

TECHNICAL NOTE

IBIS BEHAVIORAL MODELS

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INTRODUCTION

A new standard for formatting analog models of digital integrated circuit I/O characteristics is beginning to emerge and promises to provide fast, accurate simulations for transmission line and signal integrity analysis. This standard is rapidly being adopted by semiconductor manufacturers and electronic design automation vendors to assist system designers in efforts to increase bus speeds with greater confidence.

The I/O-buffer information specification (IBIS) was developed at Intel as a way of supporting designs for the Pentium® system. The IBIS specification provides a standard parsed file format of current/voltage (I/V) characteristics, device package parasitics and ESD protection device characteristics for several types of I/O structures. Some of these structures include ECL, open source, open drain and tristate.

SPICE VS. IBIS

IBIS models obtained from manufacturers have definite advantages over SPICE models. Most IBIS behavioral data is taken from actual devices. Thus, if the IBIS data is properly taken, the resulting model data has a direct correlation to the actual device. Another advantage is that IBIS models tend to simulate much faster than SPICE models. Some sources quote as much as a 25-fold increase in the performance of IBIS over SPICE.

Why would you need IBIS-formatted models if SPICE models are available? The answer to this question is quite simple. Semiconductor manufacturers are reluctant to provide SPICE models of I/O structures to the public because the models often communicate confidential process and circuit design information or the manufacturer only has models for in-house silicon-simulation tools. When SPICE models are made available to the public, the models are often "sanitized" so that any proprietary information is masked. This can result in a model that does not accurately convey the analog behavior of the device. Whether or not the SPICE model is accurate depends on the nature of the proprietary information removed from the model and the extent to which the model made available to the public is maintained to reflect the latest process and design of the device.

STRUCTURE OF AN IBIS MODEL

The current version of IBIS is composed of five basic elements as shown in Figure 1 (Ref. 1) below. Element 1 is the pull-down structure, element 2 is the pull-up structure, element 3 contains the protection devices, element 4 is the intrinsic skew time for a rising or falling signal, and element 5 is the package parasitics. Within an IBIS file, each pin can have a different model to reflect differences in input or output structure.

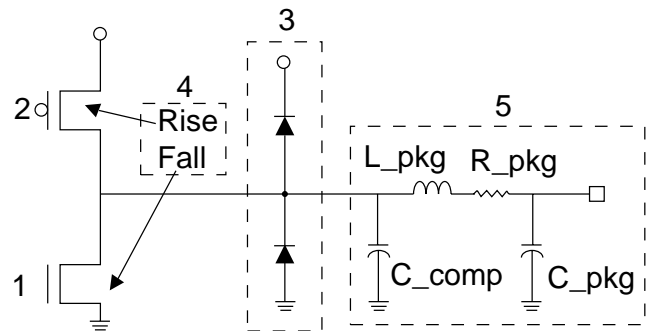


Figure 1
ELEMENTS OF AN IBIS MODEL

The following are examples of what the elements of an IBIS model look like when formatted for the IBIS file parser. Element 1 is the pull-down information that describes the I/V characteristics during pull-down. You can see that there is data for minimum and maximum current for given voltages. (These are temperature- and process-dependent specifications.)

[Pull-down]			
Voltage	I(typ)	I(min)	I(max)
-5	-177.7m	-165.8m	-189.6m
-4	-149.5m	-138.8m	-160.1m
-3	-117.5m	-108.5m	-126.5m
-2	-81.4m	-74.5m	-88.3m
data omitted			
10	139.4m	128.6m	150.2m

You may notice that the data is taken for -V_{DD} to 2V_{DD}. The main reason the voltage sweep is done over such a wide range is that this allows a behavioral model

for signal reflections caused by improper termination. Sweeping over this voltage range also allows modeling of the device for overshoot and undershoot situations when the protection diodes are forward biased. The current from the protection diodes is not included in this data. When the data is captured, the current from the protection diode is subtracted from the overall current before the current data is entered in the table. Diode current is later added by the simulator from model data when appropriate.

Element 2 contains data for the pull-up state of the buffer when the output drives high. This data is entered into the table using the formula $V_{TABLE} = V_{DD} - V_{OUTPUT}$ since the current through the pull-up device is dependent on the voltage between the output and V_{DD} .

[Pull-up]

Voltage	I(typ)	I(min)	I(max)
-5	-223.0m	-204.0m	-242.0m
-4	-197.4m	-190.7m	-204.0m
-3	-161.8m	-156.6m	-167.0m
-2	-125.3m	-118.6m	-132.0m
data omitted. . . .			
10	0.0	0.0	0.0

The minimum and maximum values are determined by the minimum and maximum operating temperatures, supply voltages and process variations. With the minimum and maximum values for data points, a worst-case and best-case model can be assembled. By combining the highest current values with the fastest ramp time and minimum package characteristics, a fast model can be derived. A slow model can be derived by combining the lowest current with the slowest ramp time and maximum package characteristics.

Notice the keyword surrounded by square brackets before each element of the model. This keyword indicates the nature of the data that follows so that the simulator can either use the data from the parsed ASCII file directly or translate the data into a format used by the simulation software.

Element 3 contains data describing the ground and power clamp diodes.

[GND_clamp]

Voltage	I(typ)	I(min)	I(max)
-5	-188.3m	NA	NA
-4	-144.9m	NA	NA
-3	-109.3m	NA	NA
-2	-58.9m	NA	NA
data omitted. . . .			

Voltage	I(typ)	I(min)	I(max)
10	0.1u	NA	NA
[POWER_clamp]			
-5	18.4m	NA	NA
-4	11.6m	NA	NA
-3	3.5m	NA	NA
-2	0.8m	NA	NA
data omitted. . . .			
10	0.1u	NA	NA

The power and ground clamp diodes are modeled in parallel with the driver information in the first two elements to ensure that the diode characteristics are present even when the output buffer is in tristate. Data for the diodes is taken with the output tristated (if possible) and is done using the same methods described above for the pull-up and pull-down structures.

Element 4 contains the ramp time for the pull-up and pull-down devices. This information is indicated by the keyword [Ramp] and is provided to ensure proper AC operation of the model.

[Ramp]

	typ	min	max
dV/dt_f	1.98/58p	1.87/60.5p	2.09/56.9p
dV/dt_r	1.55/158p	1.46/160p	1.64/177p

The min and max columns represent the minimum and maximum slew rates for the buffers. These values are very small since they represent the intrinsic values of the transistors with all package parasitics and external loads removed.

Element 5 adds the component and package parasitics. C_{comp} is the capacitance of the die itself, excluding the package capacitance. The package characteristic resistance, inductance and capacitance are added by R_{pkg} , L_{pkg} , and C_{pkg} , respectively.

[Package]

	typ	min	max
R_{pkg}	52mohm	51mohm	53mohm
L_{pkg}	6.425nH	3.33nH	9.52nH
C_{pkg}	0.875pF	0.4pF	1.35pF
• data omitted. . . .			
•			
	typ	min	max
C_{comp}	2.33p	2.17p	3.14p

Many of the capabilities of the IBIS model to simulate “real world” situations are actually dependent on the capabilities of the simulation software. The latest

version of the IBIS format (Version 3.0) contains more keyword areas that provide necessary data to model such things as ground bounce, simultaneous switching output events, gradual turn on (slew rate controlled) outputs, etc. IBIS models cannot be used to measure propagation delays or provide timing information. The main purpose of IBIS data is to simulate transmission lines and analyze signal integrity issues.

IBIS OPEN FORUM

Analog simulator vendors, computer manufacturers and IC vendors have formed a group known as the IBIS Open Forum. This group is an open, voluntary association of companies that have worked to develop the IBIS standard in its present form. At the time of this writing, the group has managed to become part of the Electronics Industries Association and is working to get IBIS accepted as an EIA standard. This group has also assembled documentation (cookbook) outlining suggested methods for data extraction. Using the methods outlined in the "IBIS Cookbook," a model with the five elements shown in Figure 1 can be assembled.

There is a program available from the IBIS forum called the IBIS Golden Parser that checks an IBIS-compatible model for proper syntax. An IBIS model that follows the proper syntax can be used either directly by a simulator or translated into a format that can be used by a simulator. This program is available on several platforms and is offered at no charge by the IBIS forum. The source code is available for a nominal fee.

Not only can the data be extracted from empirical data, but a program developed at North Carolina State University translates SPICE to IBIS. The program works with Berkeley SPICE 2 and 3, PSPICE and HSPICE. This translator produces IBIS-formatted output from actual simulation results. The program is available in the public domain for semiconductor manufacturers and end users to use to generate IBIS models from SPICE models.

FUTURE VERSIONS OF IBIS

The process of proposing changes to the IBIS format is through a buffer issue resolution document (BIRD).

Through this process, a majority vote of the forum ratifies proposed changes.

The latest IBIS version as of this writing is version 3.0. All versions (future and present) are backwards compatible with previous versions. Version 3.0 has been ratified as an EIA standard.

The IBIS committee is constantly working to improve the quality and quantity of information provided in IBIS standard files. New versions of the standard file format are constantly under review.

SOFTWARE VENDOR SUPPORT OF IBIS

As of this writing, there are 33 companies and organizations that have either participated in creating the IBIS specification or are creating/distributing/using IBIS models. As more models are made available and the IBIS format becomes more widely known, the number of software vendors supporting IBIS will increase.

MICRON SUPPORT OF IBIS

Micron has already produced IBIS models for several DRAM and SRAM devices; IBIS models for Flash devices are available upon request. Future support of IBIS will continue as long as we continue to receive customer requests for this type of assistance.

MORE INFORMATION

More information about IBIS and the IBIS Open Forum is available through the Internet. To subscribe to the IBIS Forum reflector, send your e-mail address to ibis-request@vhdl.org. The domain is 198.31.14.3. For more information, visit their Web site at www.eia.org/eia/ibis/ibis.html.

Information is also available through anonymous ftp at vhdl.org or by calling the VHDL International BBS (414) 335-0110. You will find documentation, IBIS Cookbook, recent press releases, Golden Parser, etc., residing in the pub/ibis directory.

REFERENCES

Duehren, D., W. Hobbs, A. Muranyi, and R. Rosenbaum. 1995. "I/O-buffer Modeling Spec Simplifies Simulation for High-speed Systems," *EDN*. March 16, 1995: 65-70.



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