System Coverage

This signal integrity report is generated as simulations are created for various high speed signals on the board. Some of this data may be generated with models that are not final or models from other families if the proper ones are not available. Suggested drive strengths should be conformed to as much as possible because other drive strengths may not produce desirable results.

Interfaces covered in this document

Interface Name	Structure	Topology	Constraints	Progress
PCIe X4	4 XCVR channels + clocks and sideband	Transceivers to 6Gbps	Parallelism and Cutouts	Post-Layout
HSMA	Transceivers and LVDS	XCVRs to XGbps, LVDS to Xbps	Parallelism and Cutouts	Post-Layout
HSMB	Transceivers and DQ/DQS x32 data	XCVRs to XGbps, DDR topology	Parallelism and Cutouts	Post-Layout
DDR3 HMC X40	DQ/DQS X40 data Hard Memory Cntl	DDR SSTL, 400Mhz	Topology and Parallelism	Post-Layout
DDR3 SMC X64	DQ/DQS X64 data Soft Memory Cntl	DDR SSTL, 400Mhz	Topology and Parallelism	Post-Layout
SMA Clocks	LVDS	LVDS Pairs	Parallelism and Cutouts	Post-Layout
Ethernet Interface	RGMII and XCVR	Single Ended and Channel	Parallelism and Cutouts	Post-Layout
SDI Interface	XCVR to PHY then PHY to Connector	XCVRs to XGbps, 75 Ohm to SMB	Parallelism and Cutouts	Post-Layout

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Parallelism Results

Differential Pair Edge to Edge separation in mils

Speeds						
	DDR	SMA Clks	840Mbps	875Mbps	1.25Gbps	6.5Gbps
MICROSTRIP	400MHz	550MHz	420MHz	438Mhz	625Mhz	3.25MHz
6 inch	3	4	3	3	4	23
5 inch	2	2	2	2	3	21
4 inch	2	2	2	2	2	18
3 inch	2	2	2	2	2	14
2 inch	2	2	2	2	2	10
1 inch	2	2	2	2	2	4
100 mils	2	2	2	2	2	2

Differential Coplanar edge to edge

STRIPLINE	400MHz	550MHz	420MHz	438Mhz	625Mhz	3.25MHz
6 inch	2	2	2	2	2	2
5 inch	2	2	2	2	2	2
4 inch	2	2	2	2	2	2
3 inch	2	2	2	2	2	2
2 inch	2	2	2	2	2	2
1 inch	2	2	2	2	2	2
100 mils	2	2	2	2	2	2

Differential Broadside edge to edge

STRIPLINE	400MHz	550MHz	420MHz	438Mhz	625Mhz	3.25MHz
6 inch	2	2	2	2	2	2
5 inch	2	2	2	2	2	2
4 inch	2	2	2	2	2	2
3 inch	2	2	2	2	2	2
2 inch	2	2	2	2	2	2
1 inch	2	2	2	2	2	2
100 mils	2	2	2	2	2	2

Single Edge to Edge separation in mils

Speed	
	DDR
MICROSTRIP	400MHz
6 inch	5
5 inch	2

Dual Stripline, Single ended, Coplanar edge to edge

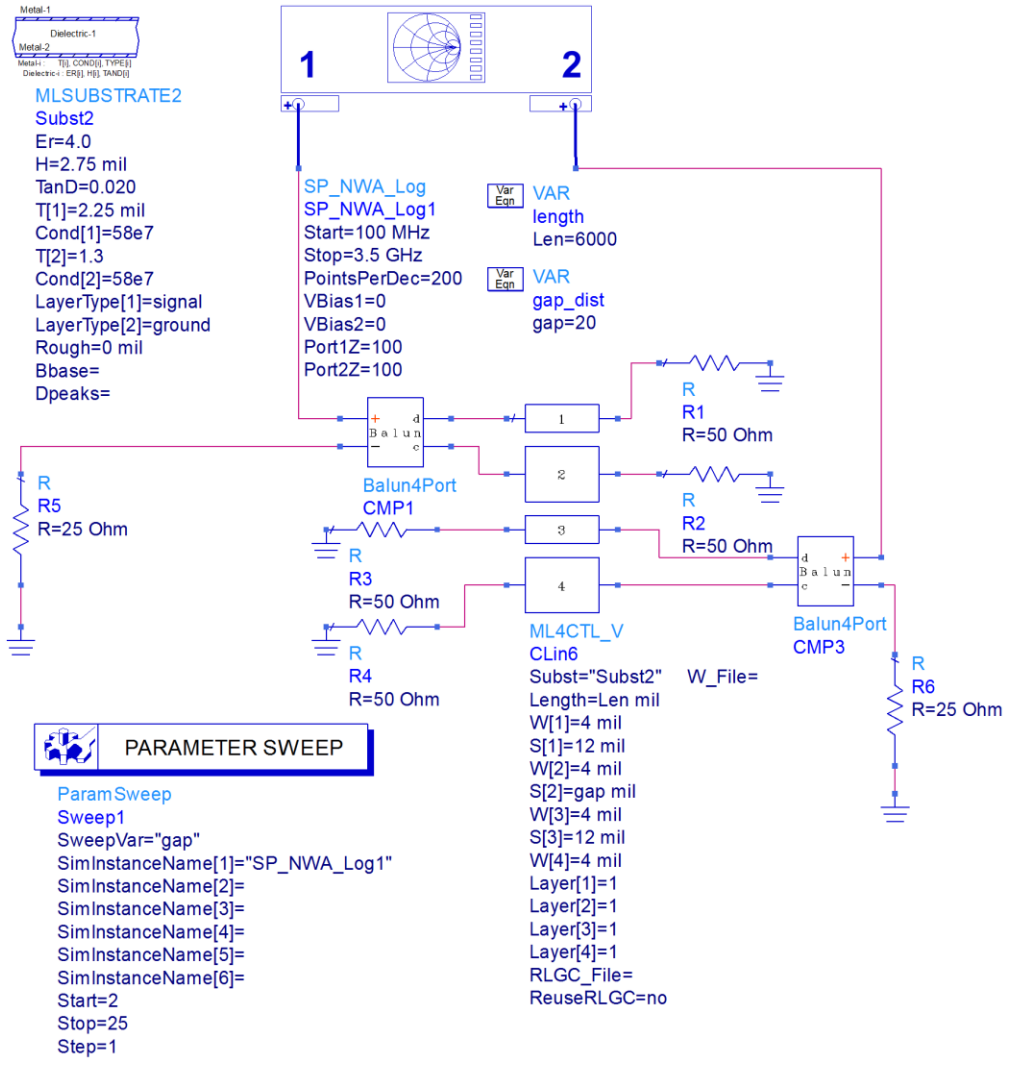
STRIPLINE	400MHz
6 inch	2

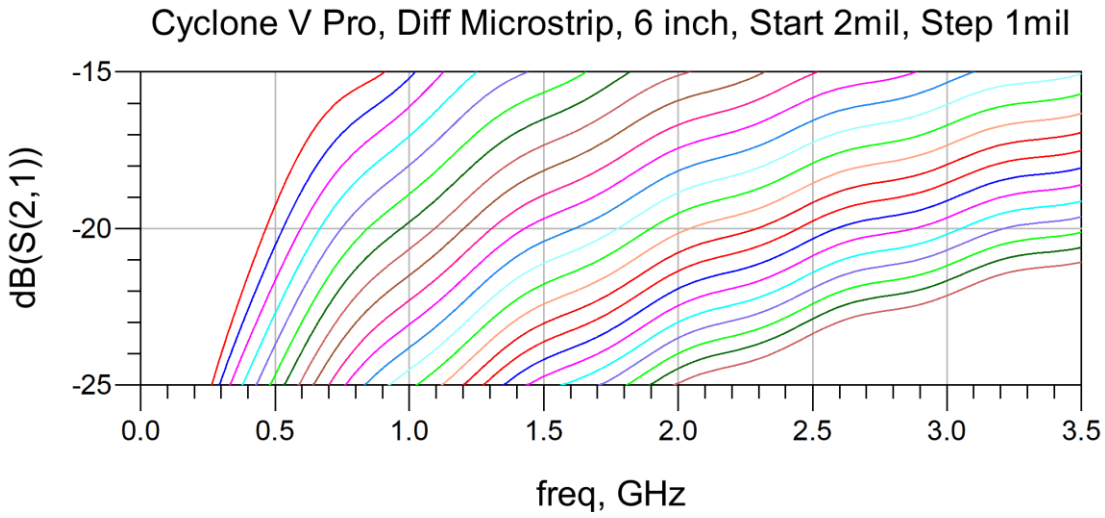
Dual Stripline, Single Ended, Broadside edge to edge

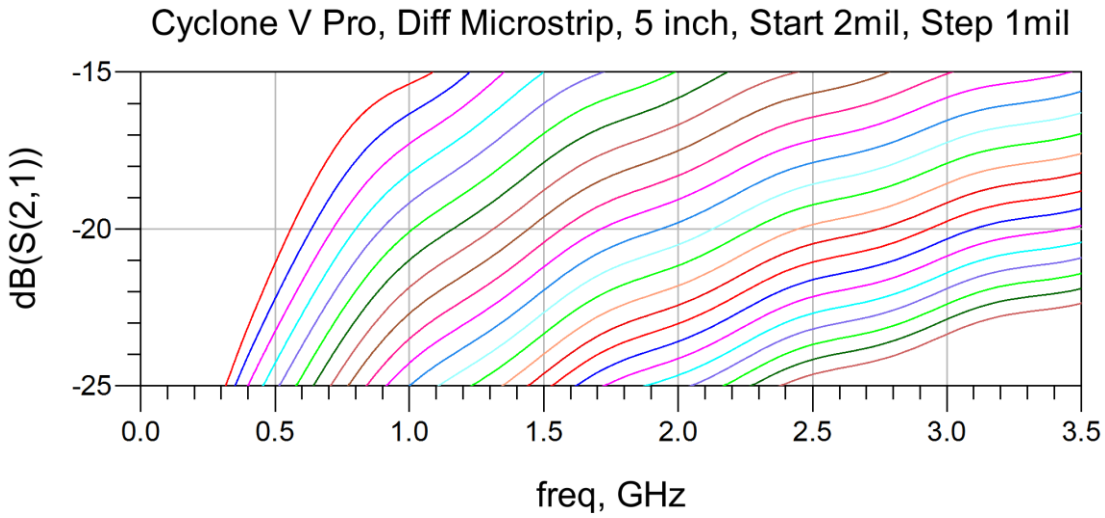
STRIPLINE	400MHz
6 inch	3.9

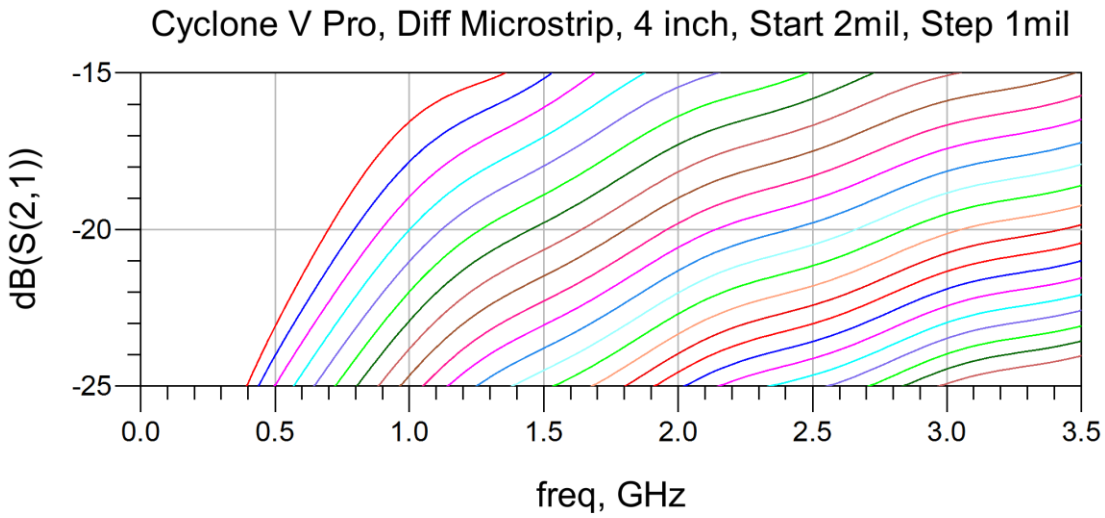
Parallelism Rule Simulations

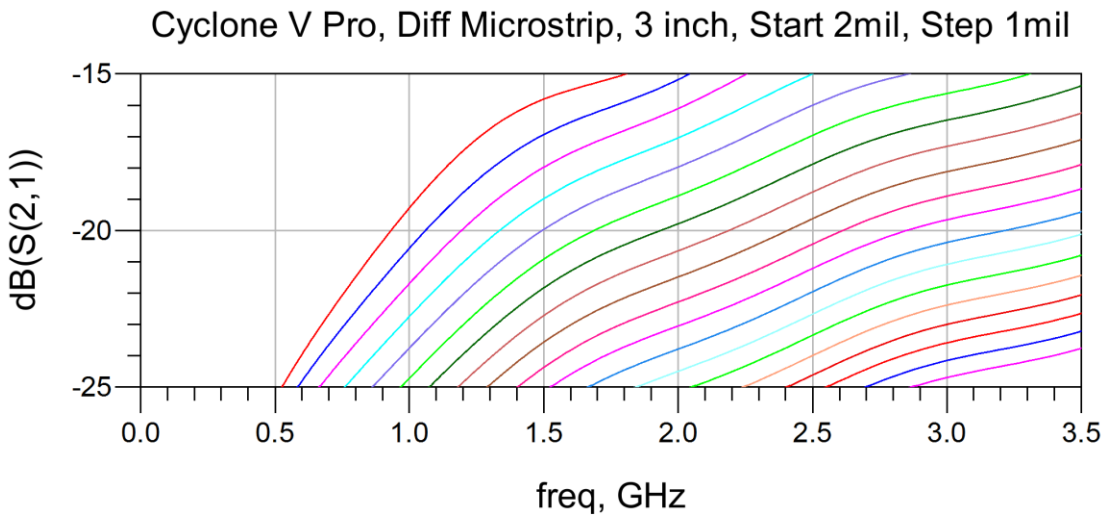
Differential Microstrip

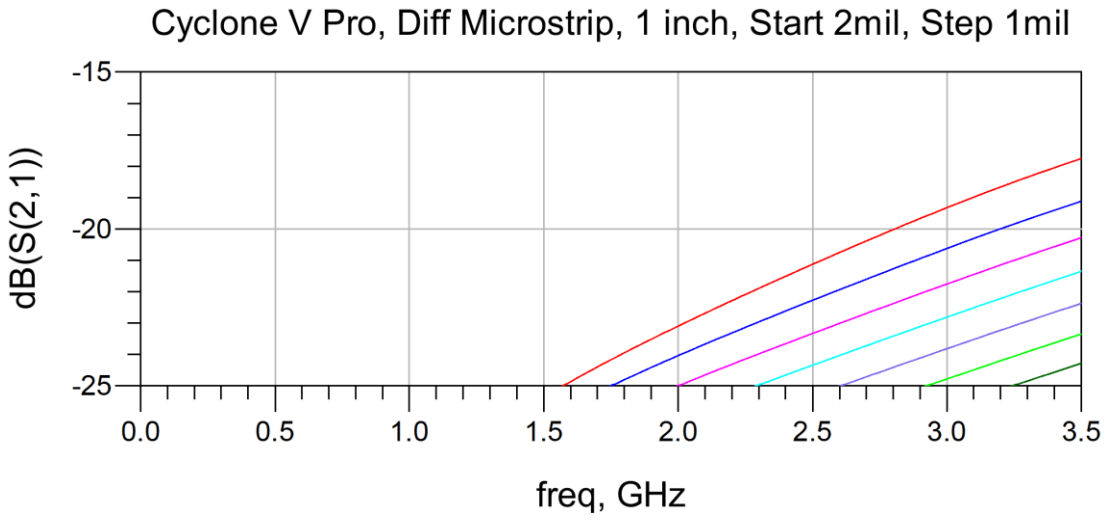



Cyclone V Pro, Diff Microstrip, 6 inch, Start 2mil, Step 1mil
dB(S(2,1))
-15
-20
-25
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz

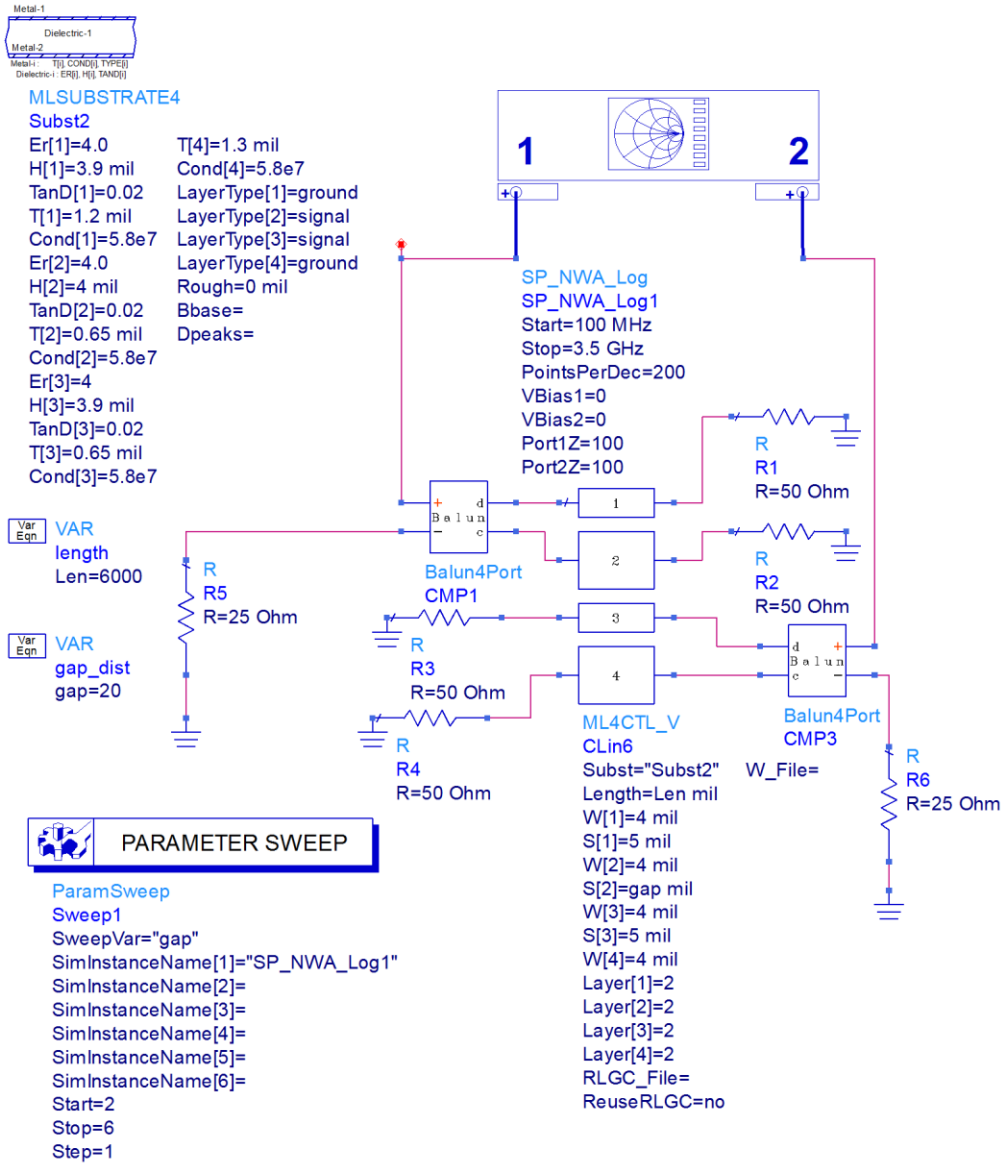

Cyclone V Pro, Diff Microstrip, 5 inch, Start 2mil, Step 1mil
dB(S(2,1))
-15
-20
-25
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz

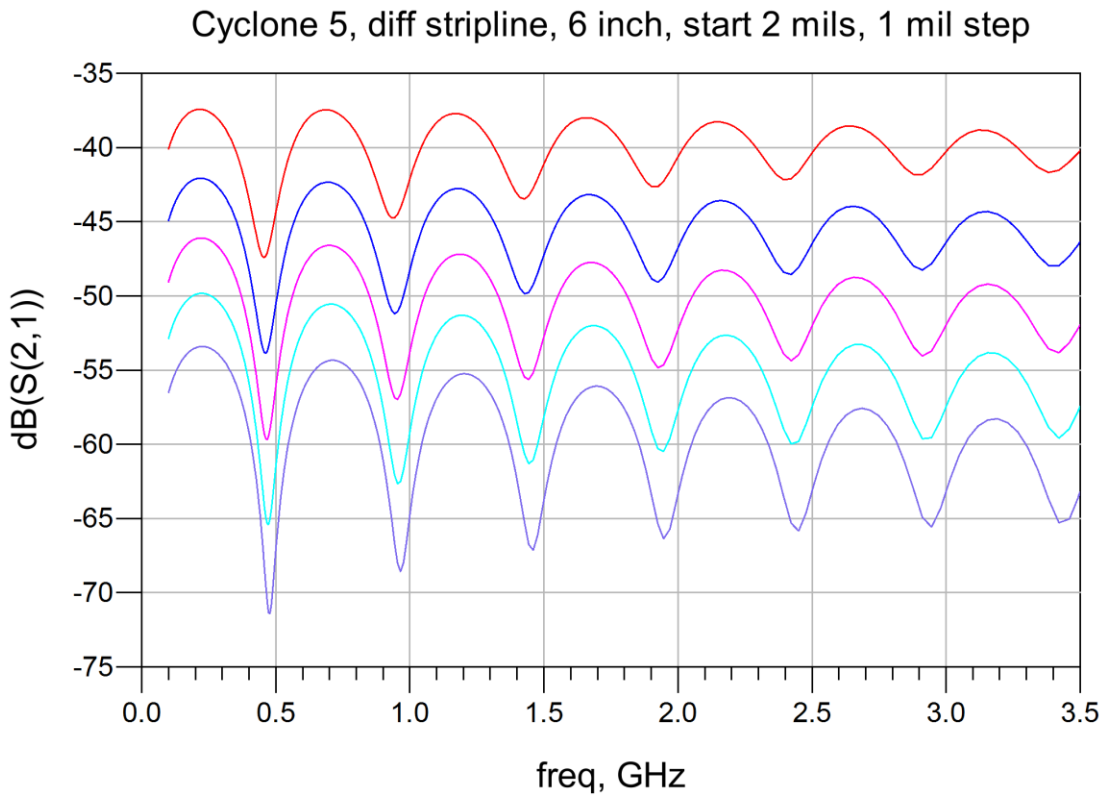

Cyclone V Pro, Diff Microstrip, 4 inch, Start 2mil, Step 1mil
dB(S(2,1))
-15
-20
-25
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz


Cyclone V Pro, Diff Microstrip, 3 inch, Start 2mil, Step 1mil
dB(S(2,1))
-15
-20
-25
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz

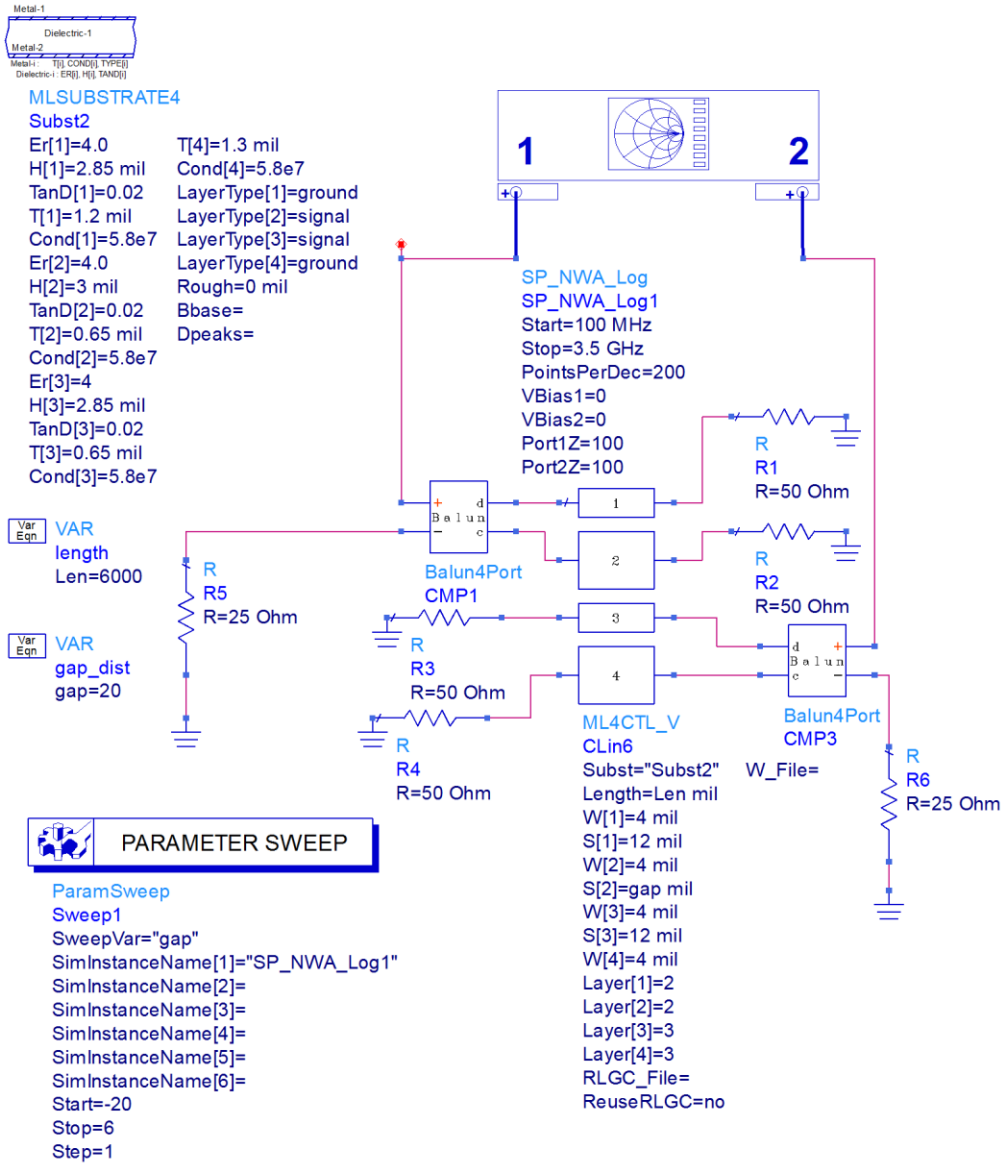

Cyclone V Pro, Diff Microstrip, 1 inch, Start 2mil, Step 1mil
dB(S(2,1))
-15
-20
-25
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz

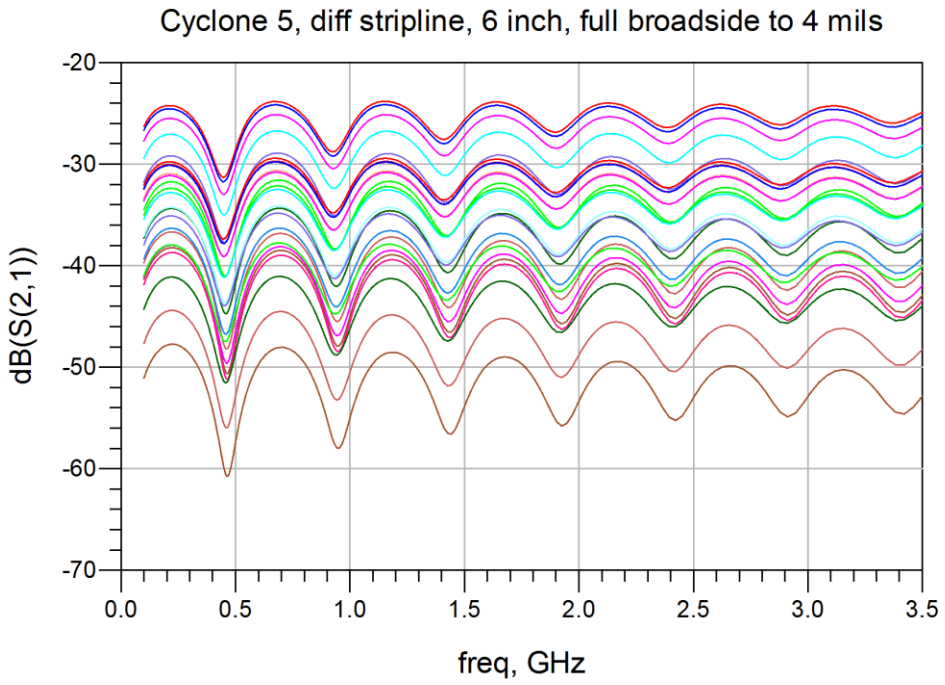
Differential Coplanar Stripline



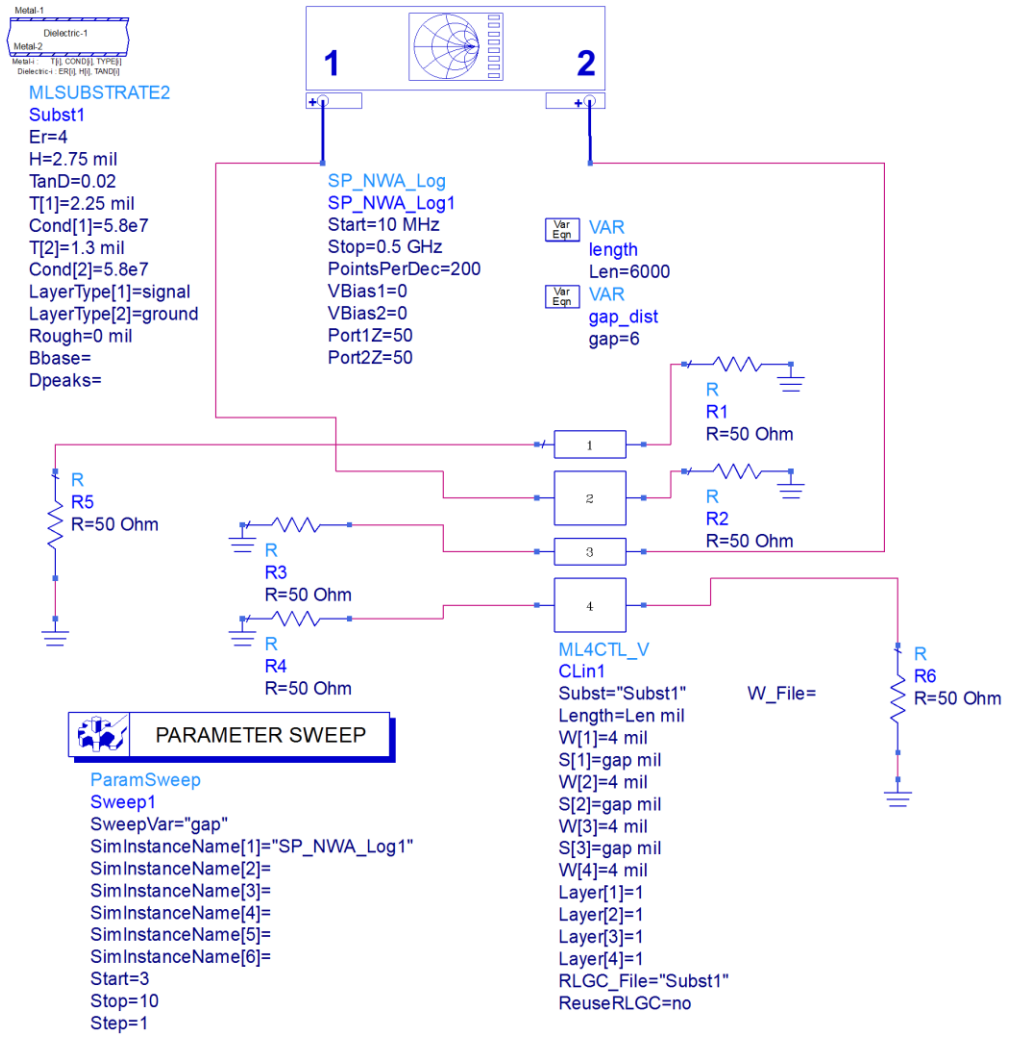

Cyclone 5, diff stripline, 6 inch, start 2 mils, 1 mil step
dB(S(2,1))
-35
-40
-45
-50
-55
-60
-65
-70
-75
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz

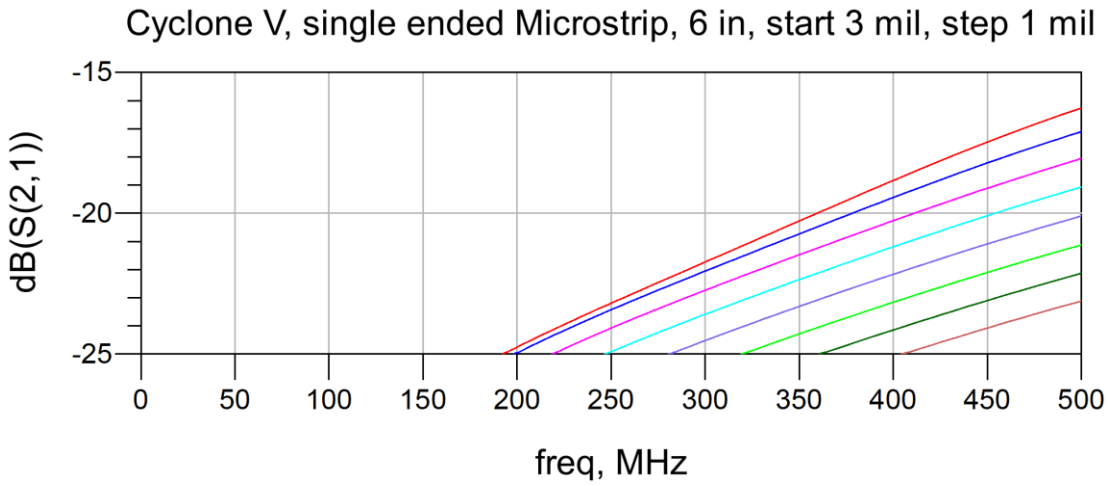
Differential Broadside Stripline

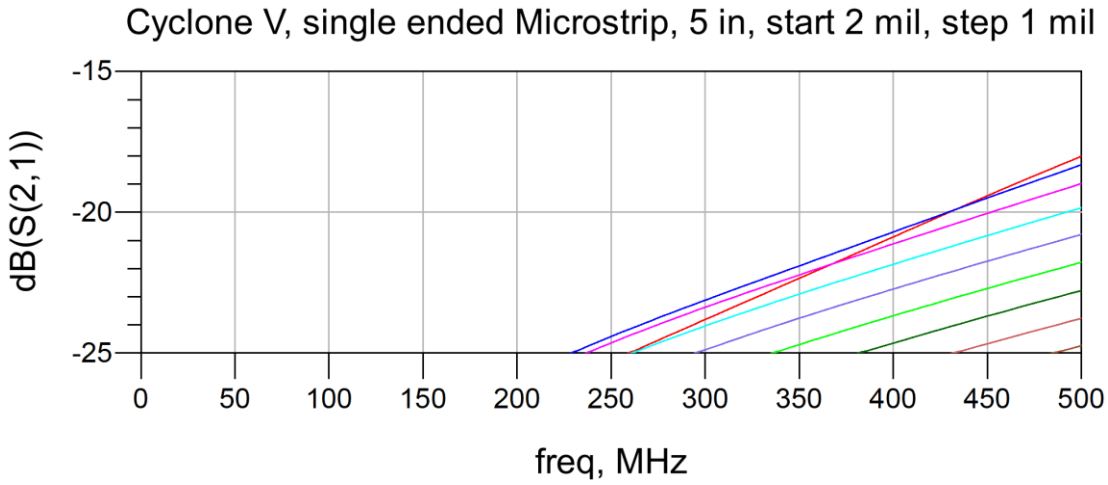



Cyclone 5, diff stripline, 6 inch, full broadside to 4 mils
dB(S(2,1))
-20
-30
-40
-50
-60
-70
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
freq, GHz

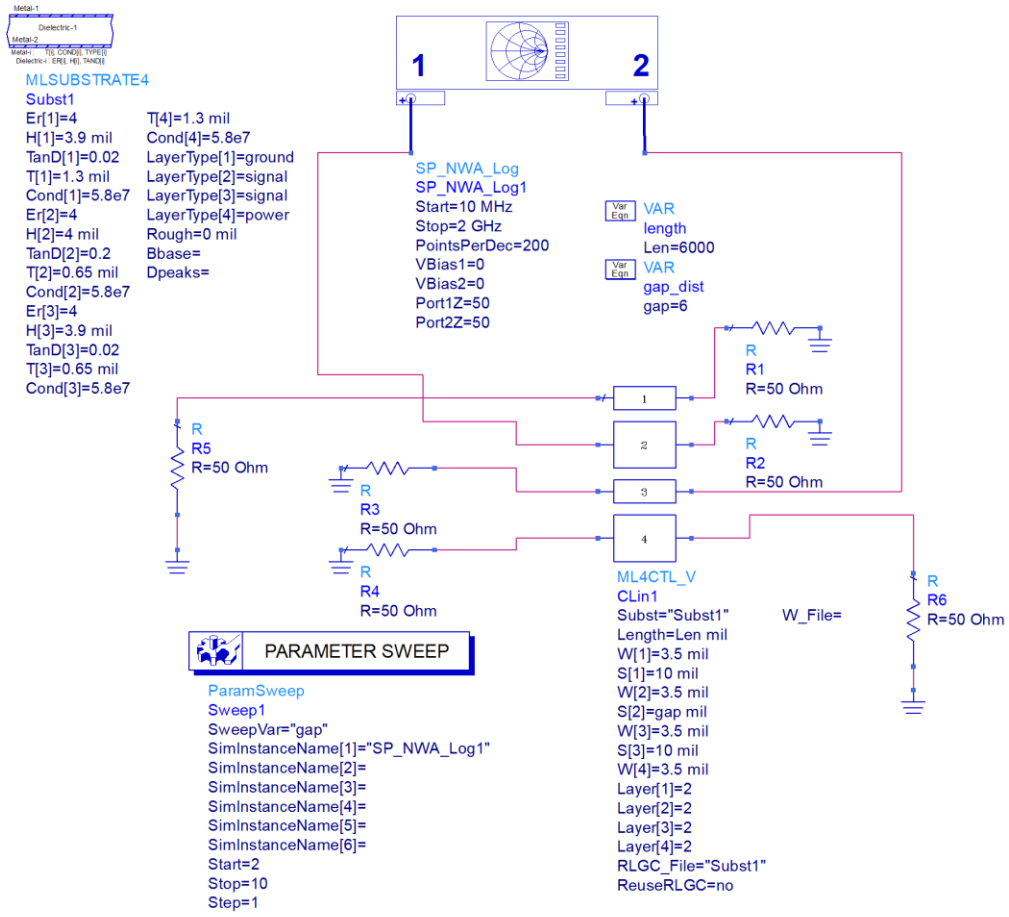
Single ended Microstrip

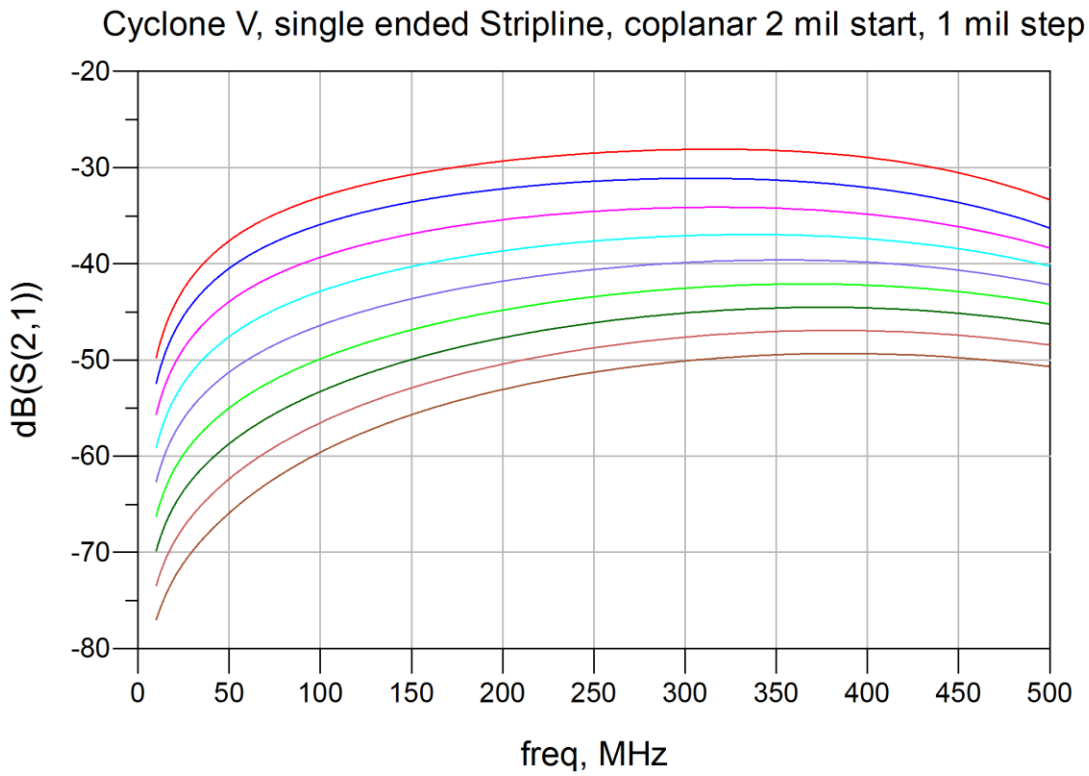



Cyclone V, single ended Microstrip, 6 in, start 3 mil, step 1 mil
dB(S(2,1))
-15
-20
-25
0
50
100
150
200
250
300
350
400
450
500
freq, MHz

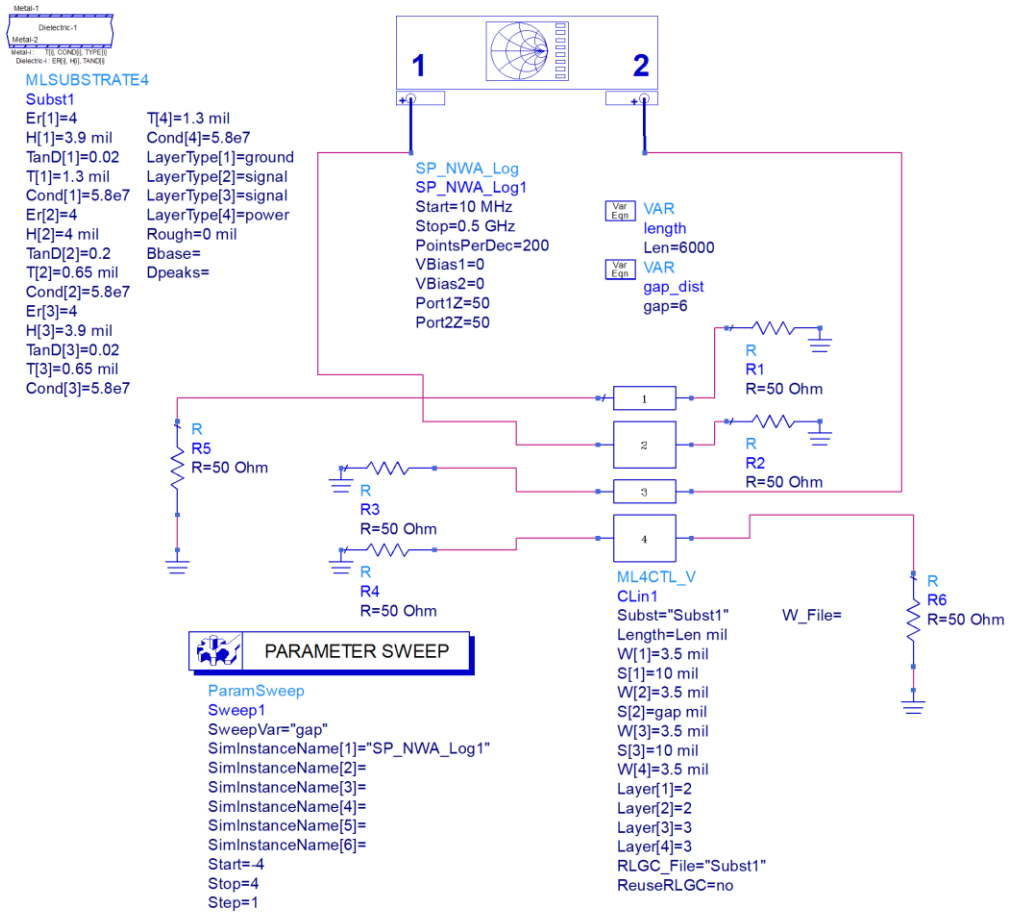

Cyclone V, single ended Microstrip, 5 in, start 2 mil, step 1 mil
dB(S(2,1))
-15
-20
-25
0
50
100
150
200
250
300
350
400
450
500
freq, MHz

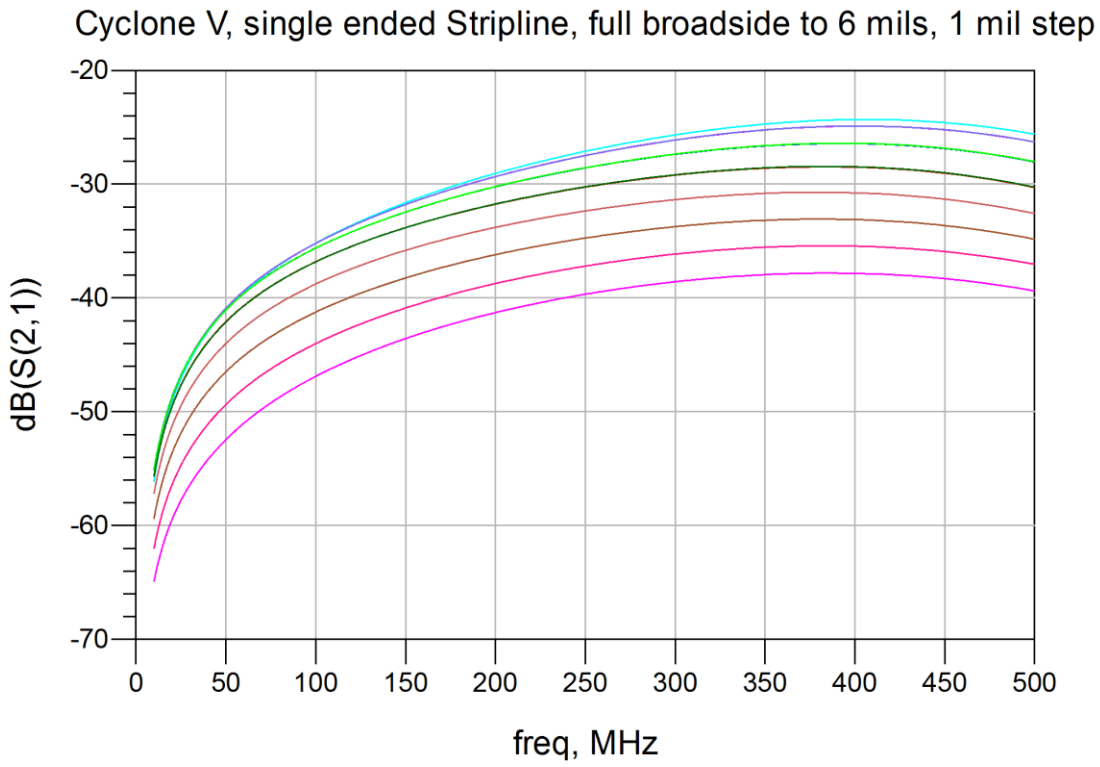
Single ended coplanar Stripline




Cyclone V, single ended Stripline, coplanar 2 mil start, 1 mil step
dB(S(2,1))
-20
-30
-40
-50
-60
-70
-80
0
50
100
150
200
250
300
350
400
450
500
freq, MHz

Single ended broadside Stripline

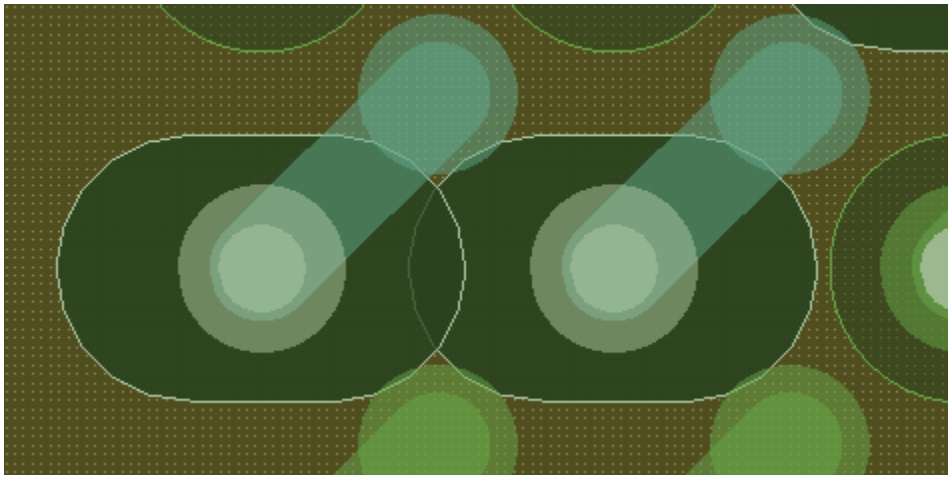




Cutouts for Discrete Components in High Speed Lines

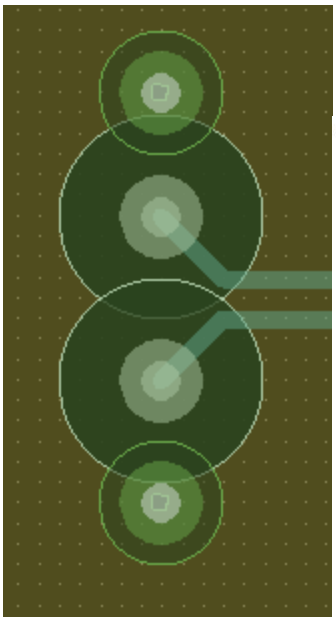
Via Structures

Via structures for high speed signals is essential. All signal vias are 8 mils.
FPGA Breakout Lines for signals <13G ellipse 30 mils by 50 mils

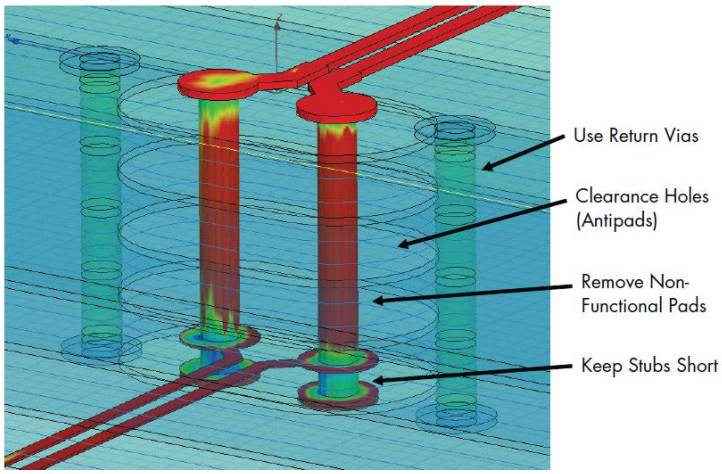


For lines >13G bring lines out on surface layer if possible to midline vias to reduce capacitance.

Midline Transceiver Vias use 8 mil drill 50 mil antipad 40 mil center to center for the signals. Ground vias 30 mils away from signal vias.



Optimal Differential Via Layout Example



For further information see "AN 529: Via Optimization Techniques for High-Speed Channel Designs" on the Altera web site.
http://www.altera.com/literature/an/an529.pdf?GSA_pos=1&WT.oss_r=1&WT.oss=AN529

Transceiver Interface Analysis

Pre-Layout

We have established a set of rules and techniques for doing transceiver channels that has worked well. Via structures and the cutout information were obtained from simulations.

Signal Layers for Transceivers

For transceivers it is preferred to use the outside layers. The ideal situation is to have all the traces on the top layer so there are no via situations to deal with. Second up is using the bottom layer for parts of the trace run. Using the whole via leaves no stubs to worry about. If the routing cannot be accomplished on the top and bottom then we use routing layers closest to the bottom of the board to minimize the stub lengths. It is not a good idea when doing really high speed channels to have stubs of any length created. Layers not close to the outer layers of the board can be used by backdrilling the via to eliminate the stub caused by the via and the pad located at the end of the via. Sometimes blind or buried vias are used but they tend to drive up the cost and complexity of the PCB.

Component Cutouts

In a lot of topologies there occur impedance discontinuities. Sometimes the ball on the package is a problem. Always DC blocking caps, termination resistors and connector pins present a discontinuity in the smooth propagation of the signal. Each one of these artifacts must be analyzed and something done to alleviate the problem. Usually an amount of material is removed from the ground and power layers below the component for

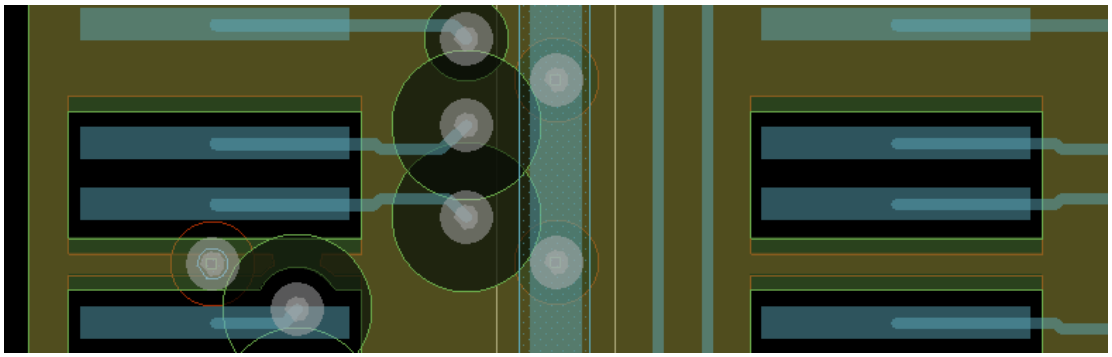
some distance to balance the impedance of the channel. The cutout size depends on the geometry of the pads associated with the component and the thickness of the dielectric layers below the component. The larger the component and pad the more capacitive coupling there is possible to the planes below. The cutout on the ground plane below a larger component pad will have a larger annular ring than that of a smaller part. Subsequent planes below the ground have larger cutouts to avoid much coupling to that plane.

Rectangular Component Cutout Summary

The units for all the distances below is mils

Board Top Layer 50 Ohm Trace Width ---------->>>	4.3	(wt)
Board Top Layer 75 Ohm Trace Width ---------->>>	4.1	(wtsdi)

Rectangular Components						
Component Type	Footprint Width	Footprint Length	First Plane cutout width	First Plane cutout length	Second Plane cutout width	Second Plane cutout length
			"=(C7+(2*(0.7*(C7-wt))))"	"=D7+2"	"=E7+10"	"=F7"
0805 smd	63	127	145	131	155	131
0603 smd	40	101	90	105	100	105
0402 smd	20	55	42	57	52	57
0201 smd	12	38	23	40	33	40
HSMC	11	90	20	92	30	92

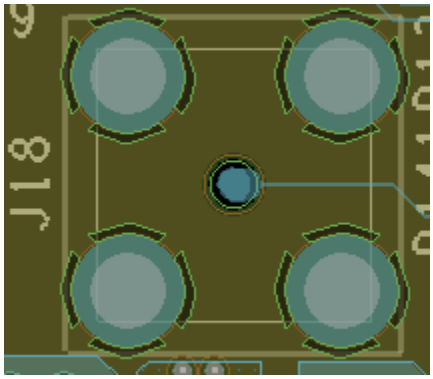


HSMC cutout example

Other components are shown in SMB section below.

SMA Connector Cutout

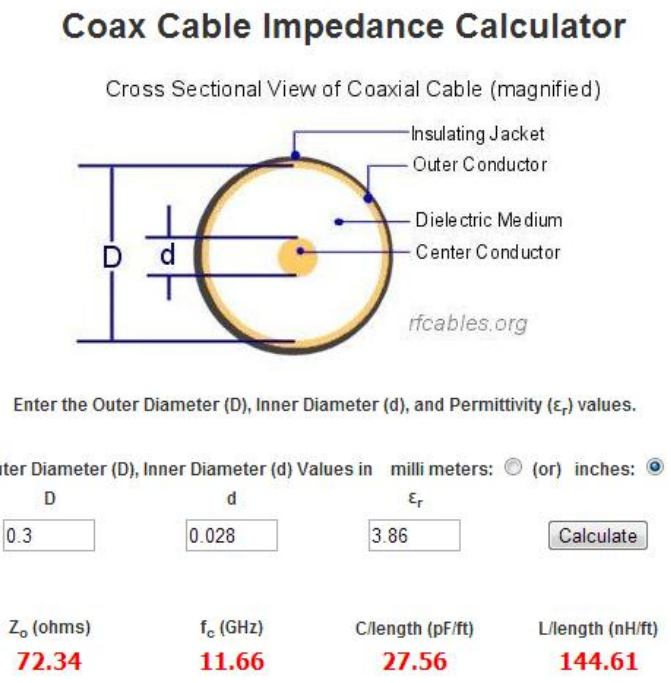
Circular Cutouts			
Component Type	Pad Diameter	First Plane Cutout Diameter	Second Plane cutout diameter
SMA smd	32	48	58



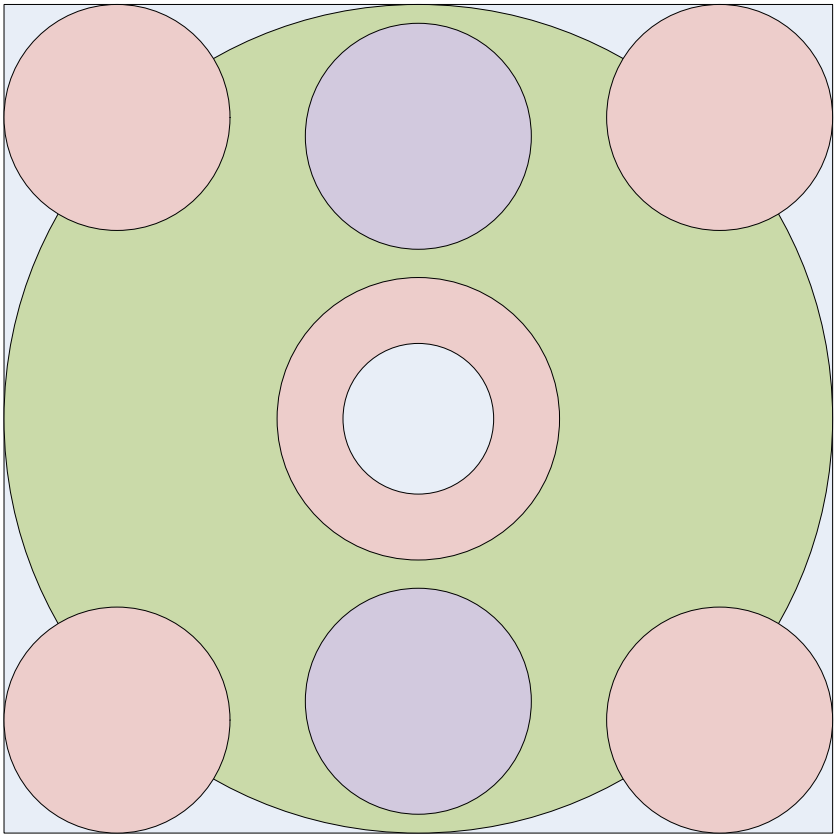
SMB Connector Cutout

The SMC connector is a through-hole part. The antipads go all the way through the board.

Using a coaxial calculator from the web:

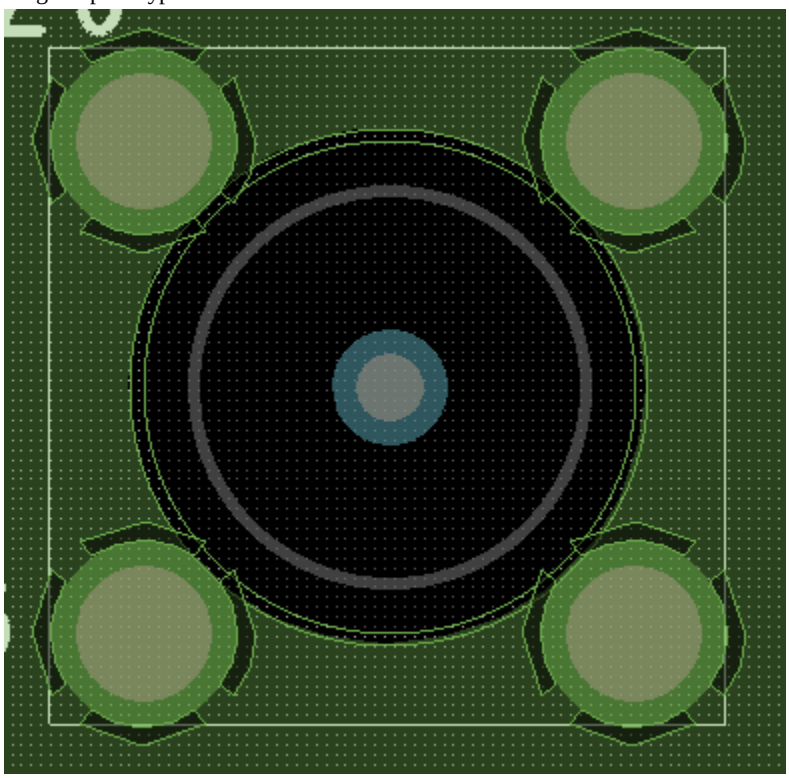


Since even that size of antipad is too large. Here is a solution



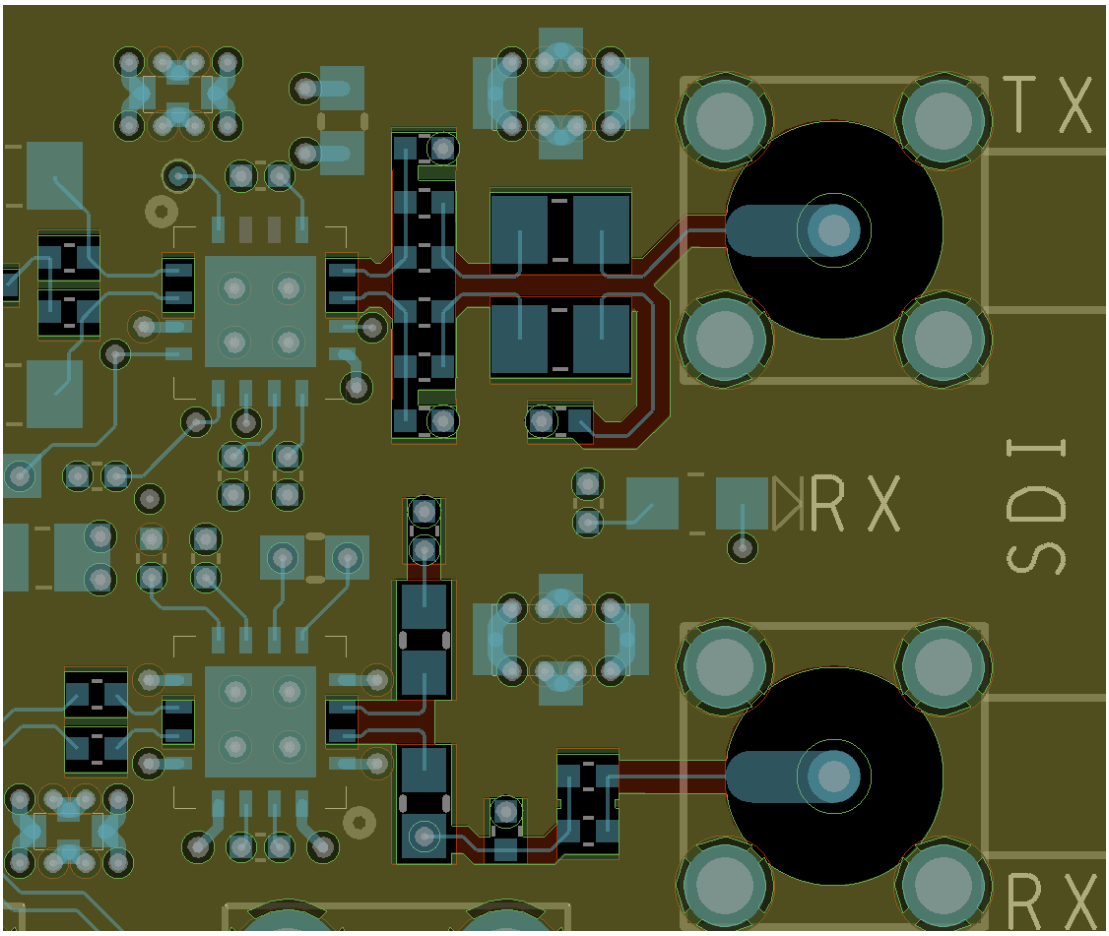
- Pink is existing pads from setup for the part
- Green is an antipad who's diameter is 275mils diameter
- Purple is a through hole drill, 75 mils in diameter, with no plating anywhere

Original prototype from Stratix V FPGA



Use this as a starting point. Increase the antipad to 275mils. Add the drills to reduce capacitance.

SDI Components and cutouts example

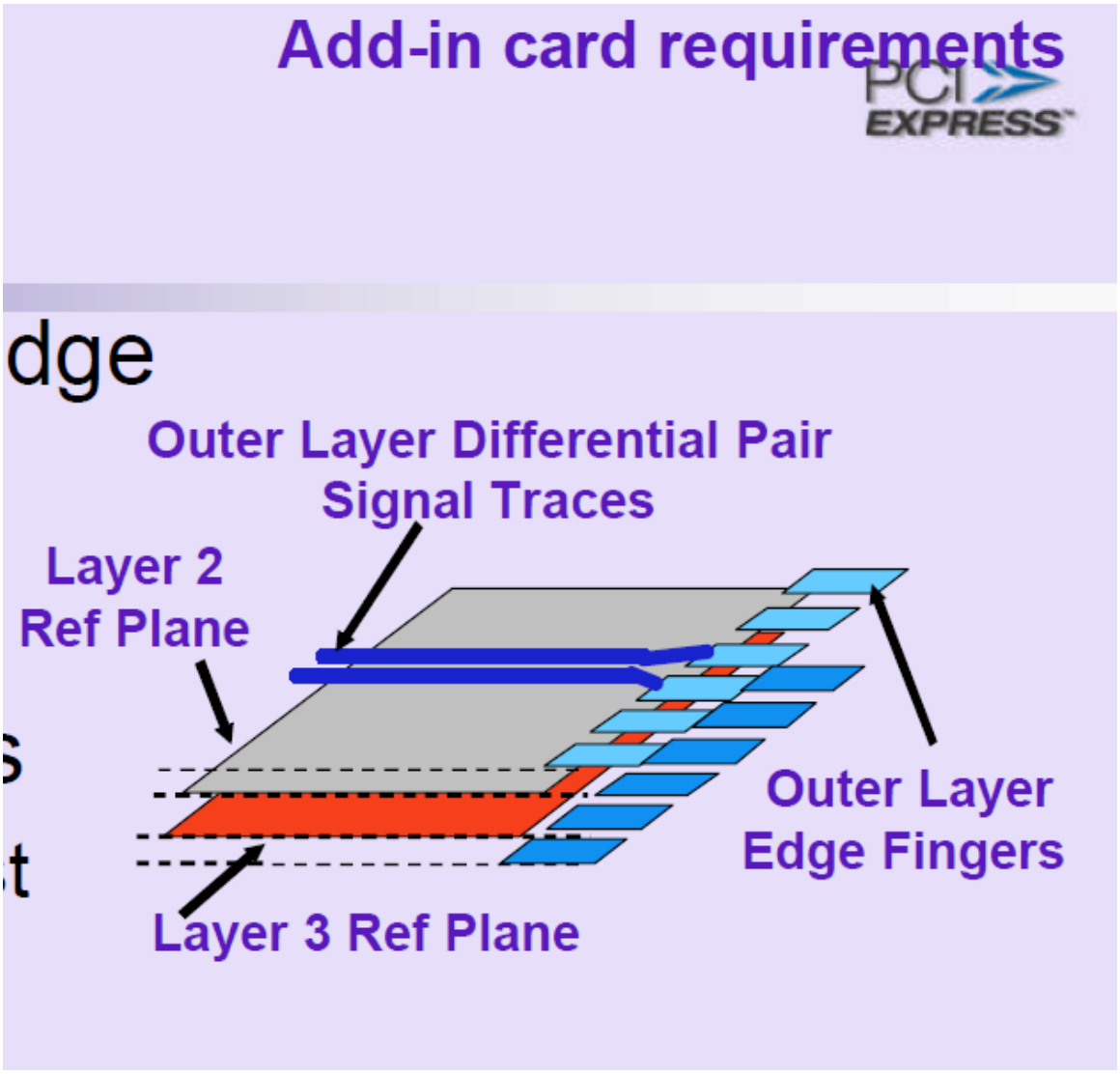


The component pins for the PHY chips are shown with cutouts. The right side of the PHY has 75 ohm traces that reference layer 3 instead of layer 2. The antipads for the larger components and the connectors are not correct in this diagram.

PCIe Interface Cutouts

Edge Connector PCIe, 28 mil width

From PCI Sig training literature:



DC Blocking caps

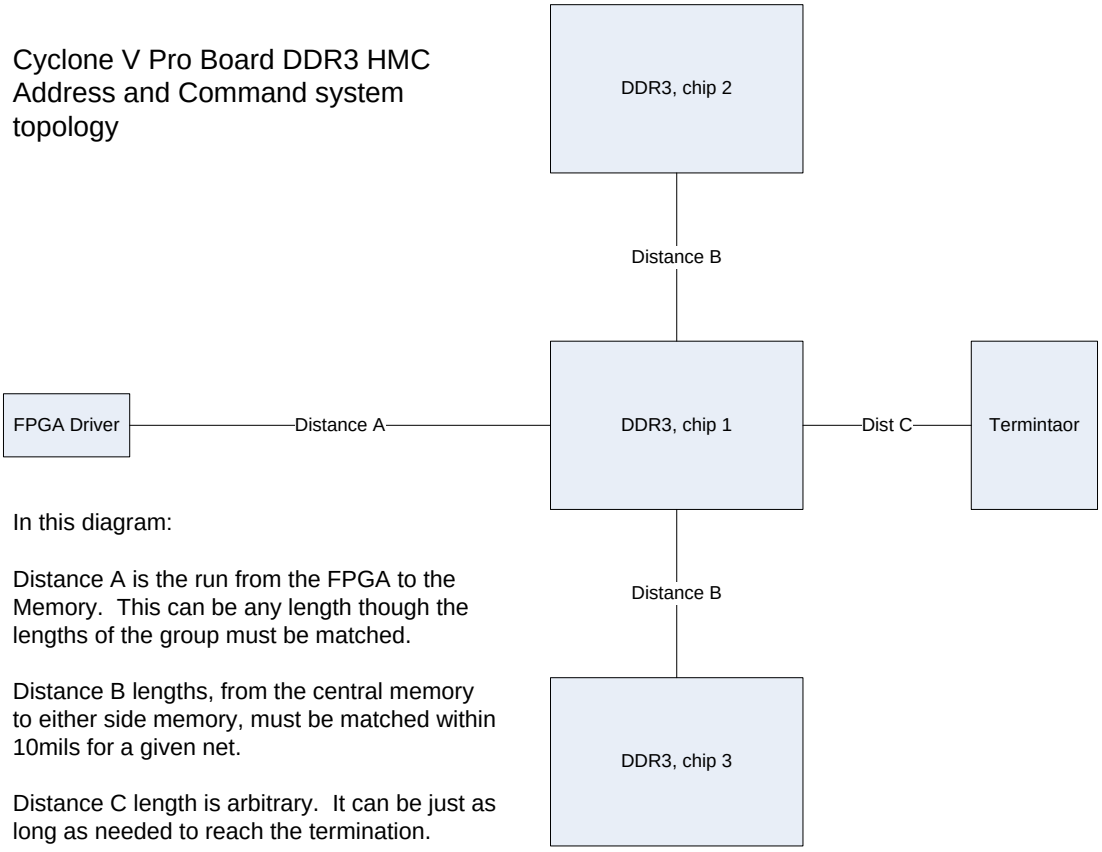
See above for 0402 cutouts in the rectangular cutout section.

DDR3A X40 Hard Memory Controller

The 40-bit data bus will comprise of three x16 devices (MT41K256M16HA-125:E) with a single address/command bus. One of the three devices will be partially used for ECC purposes only. It will use just 8 data lines and the other 8 will be terminated and not connected to HPS. This scheme is according to recommendation from Micron. This interface will connect to dedicated HMC pins for HPS I/O banks on the FPGA's top edge.

HMC Address, Command

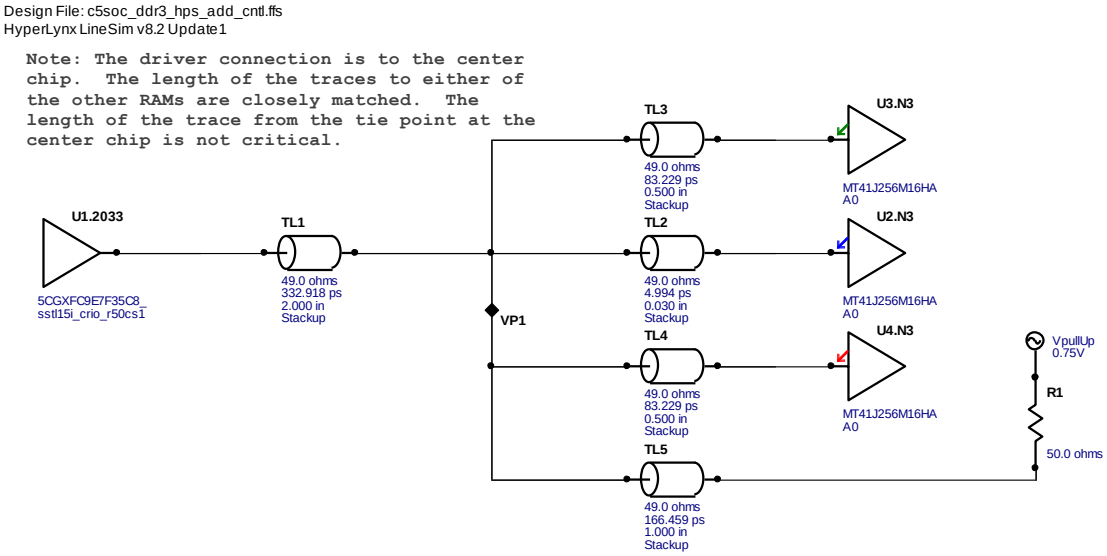
While DDR3 memory devices are designed to use a Fly-By topology for address and command signals, the Cyclone V family does not support DQ/DQS leveling. This then requires the address and command signals to be routed in a "T" or "Tree" topology. Because this interface uses three devices the balancing of the signal timing is set up as indicated below. In this topology all of the address, control signals and clocks are routed to the center chip. From this point the signals branch out to the chips on either side. The signal run to the termination is ran as short as possible to resistors above the center chip.



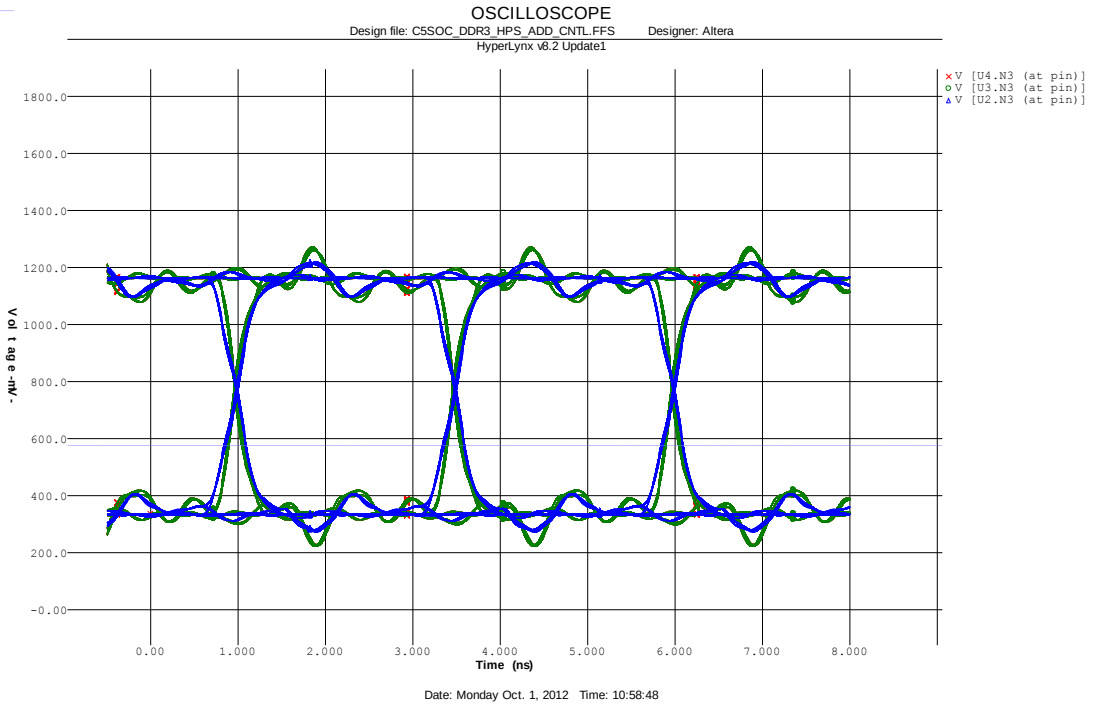
Pre-Layout Simulations for Address and Command Signals

The following simulations were made to plan the topology and determine the best drive levels.

With 50 ohm driver



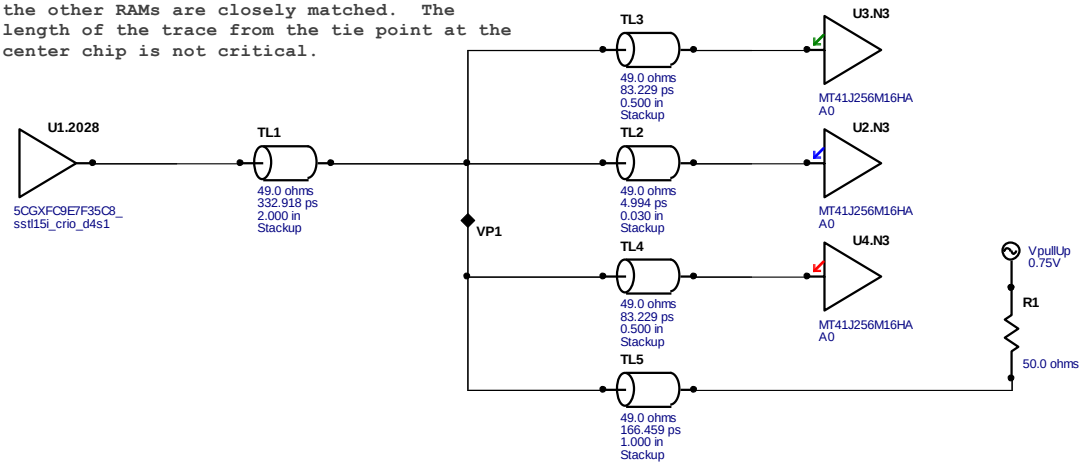
The system is driven by an 8ma output from the Cyclone Chip.

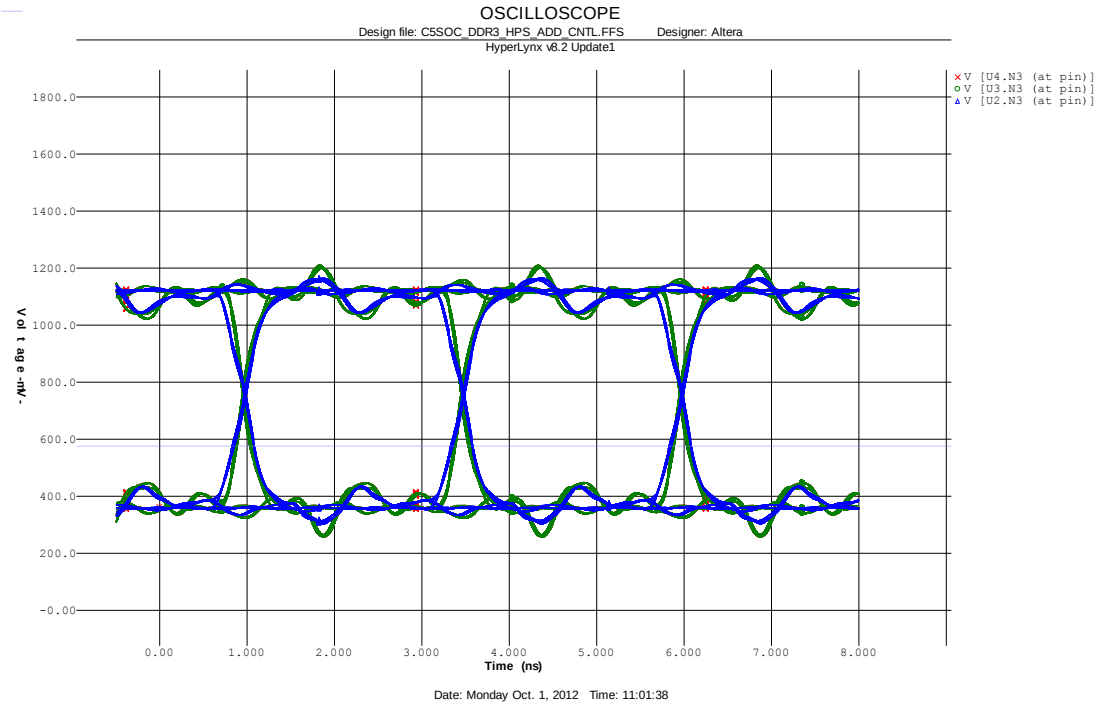


With 4ma driver using emphasis

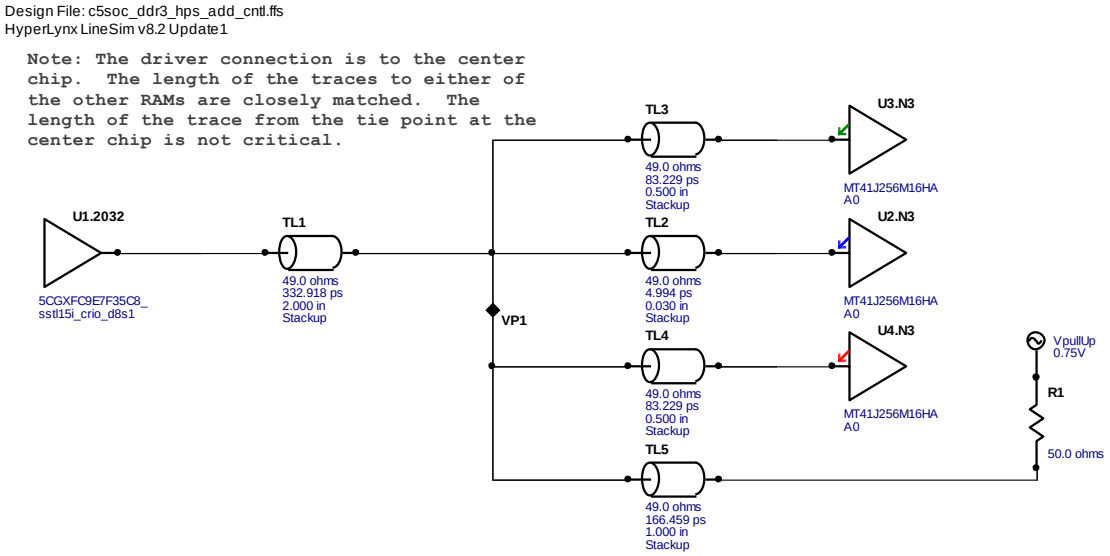
Design File: c5soc_ddr3_hps_add_cntl.ffs
HyperLynx LineSim v8.2 Update1

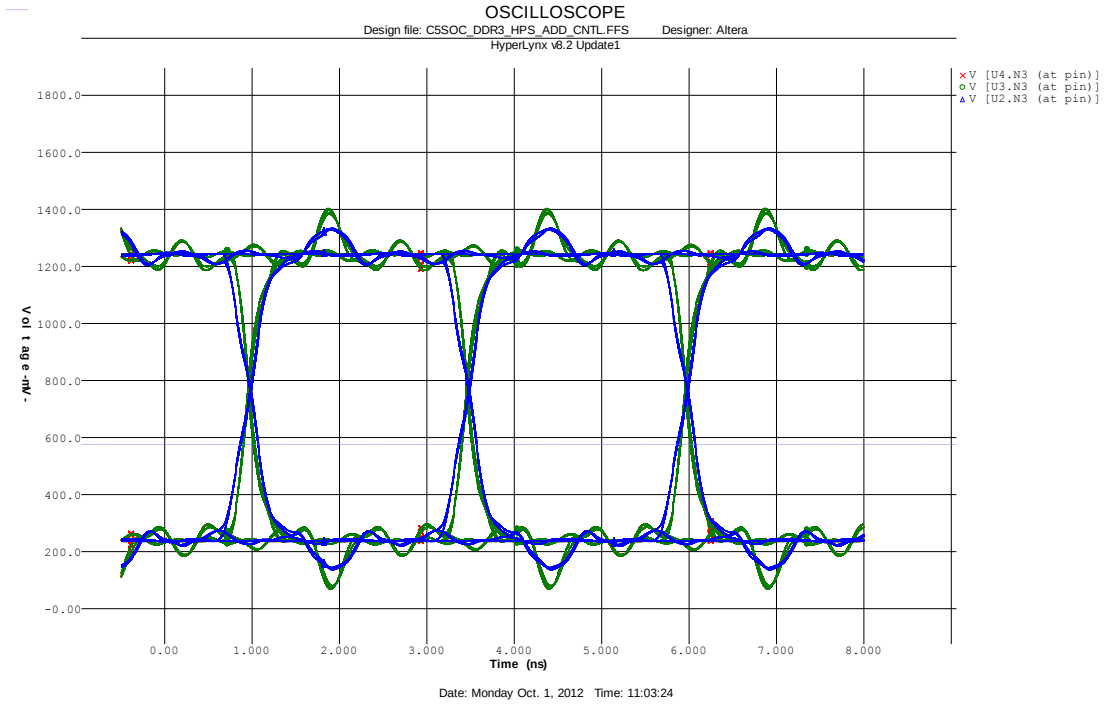
Note: The driver connection is to the center chip. The length of the traces to either of the other RAMs are closely matched. The length of the trace from the tie point at the center chip is not critical.



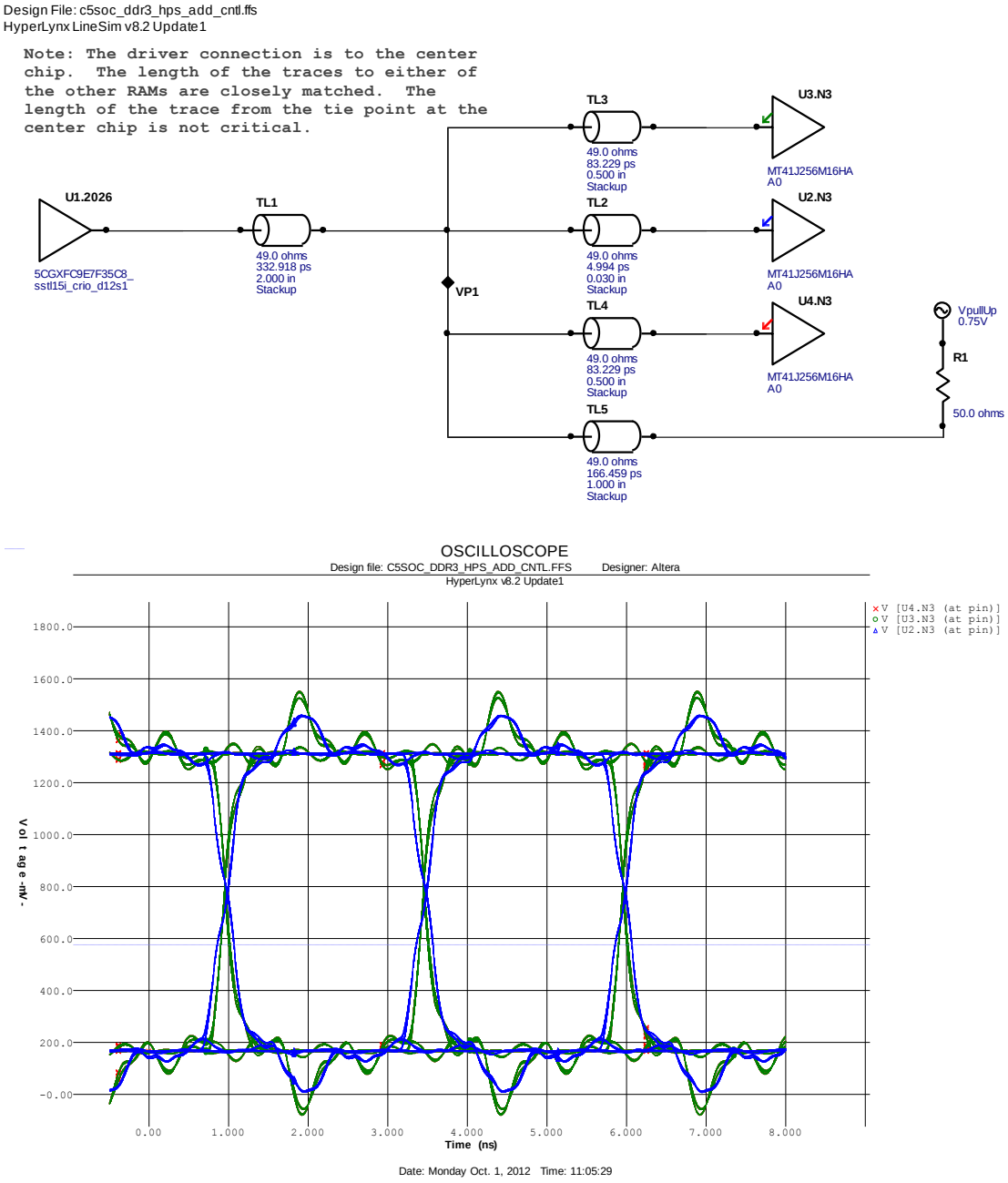


8ma drive with emphasis





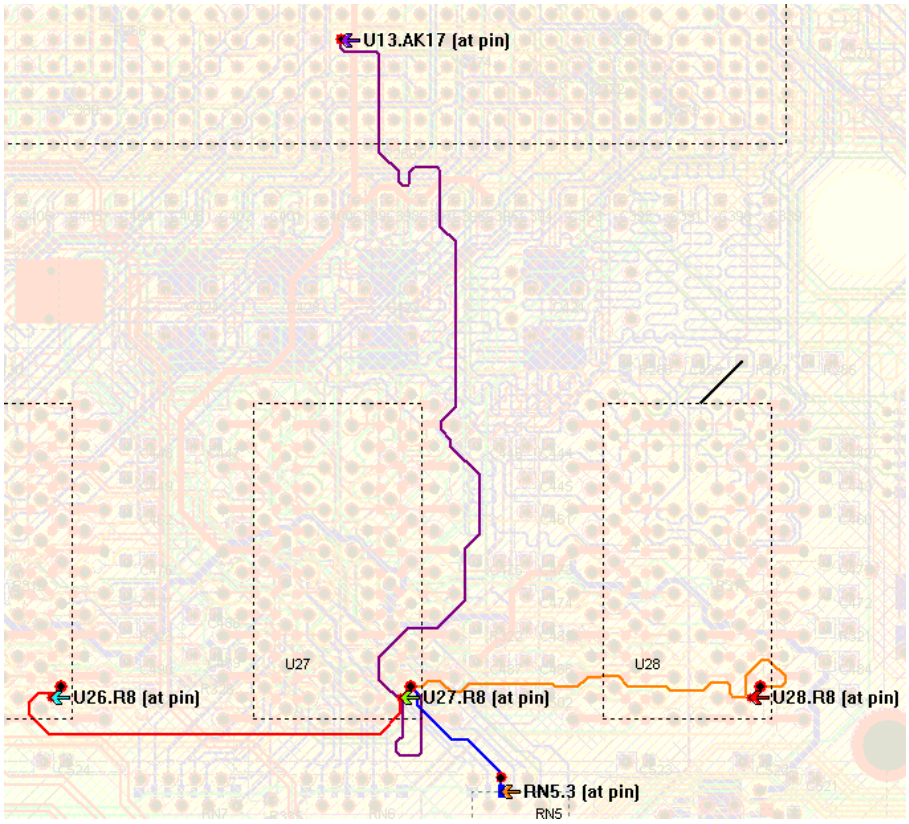
12ma driver with emphasis



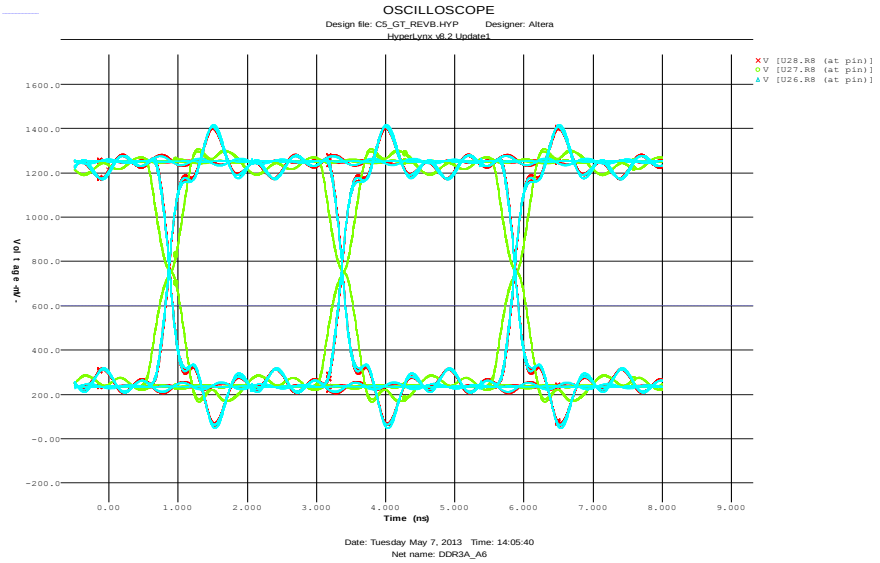
Conclusion: Using an 8ma driver with emphasis gives the best margin without overshoot.

HMC Post Layout Simulations for Address and Command Signals

The following simulations were created using the final artwork as a source for data.



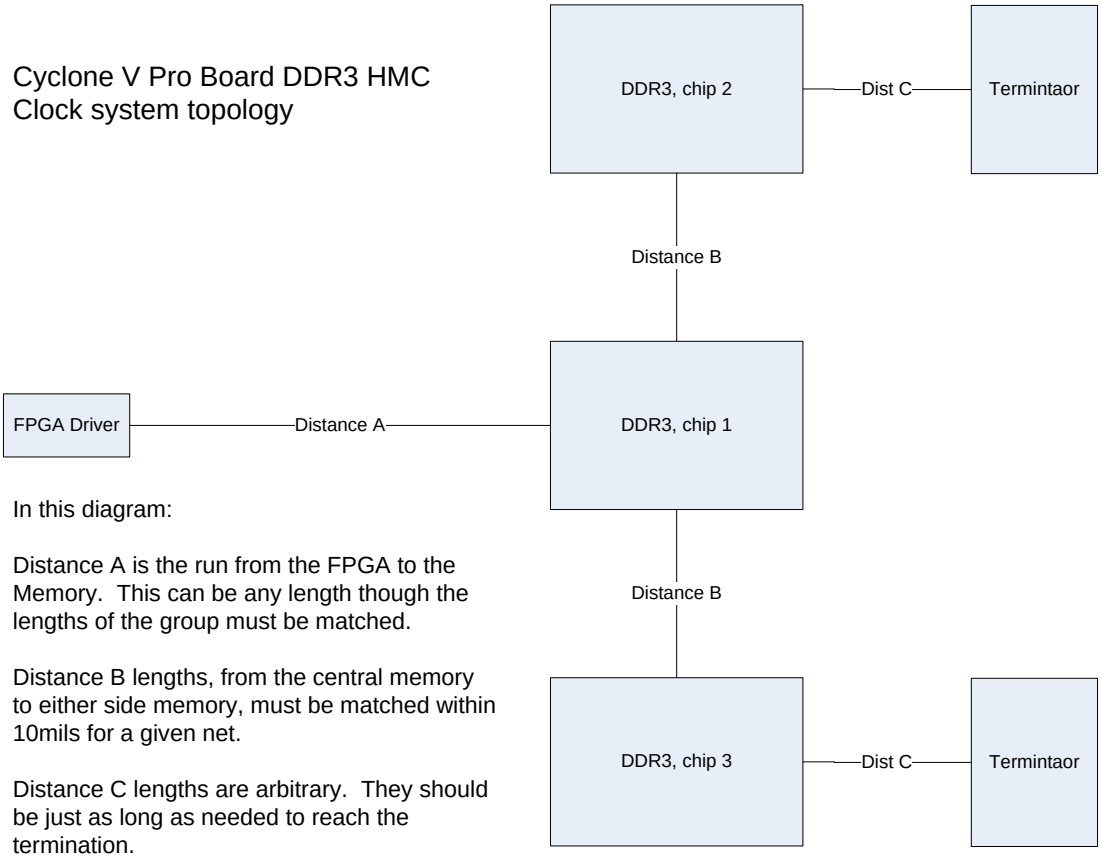
Simulation with 8ma drive



HMC Clocks

Topology Diagram

Cyclone V Pro Board DDR3 HMC Clock system topology



In this diagram:

Distance A is the run from the FPGA to the Memory. This can be any length though the lengths of the group must be matched.

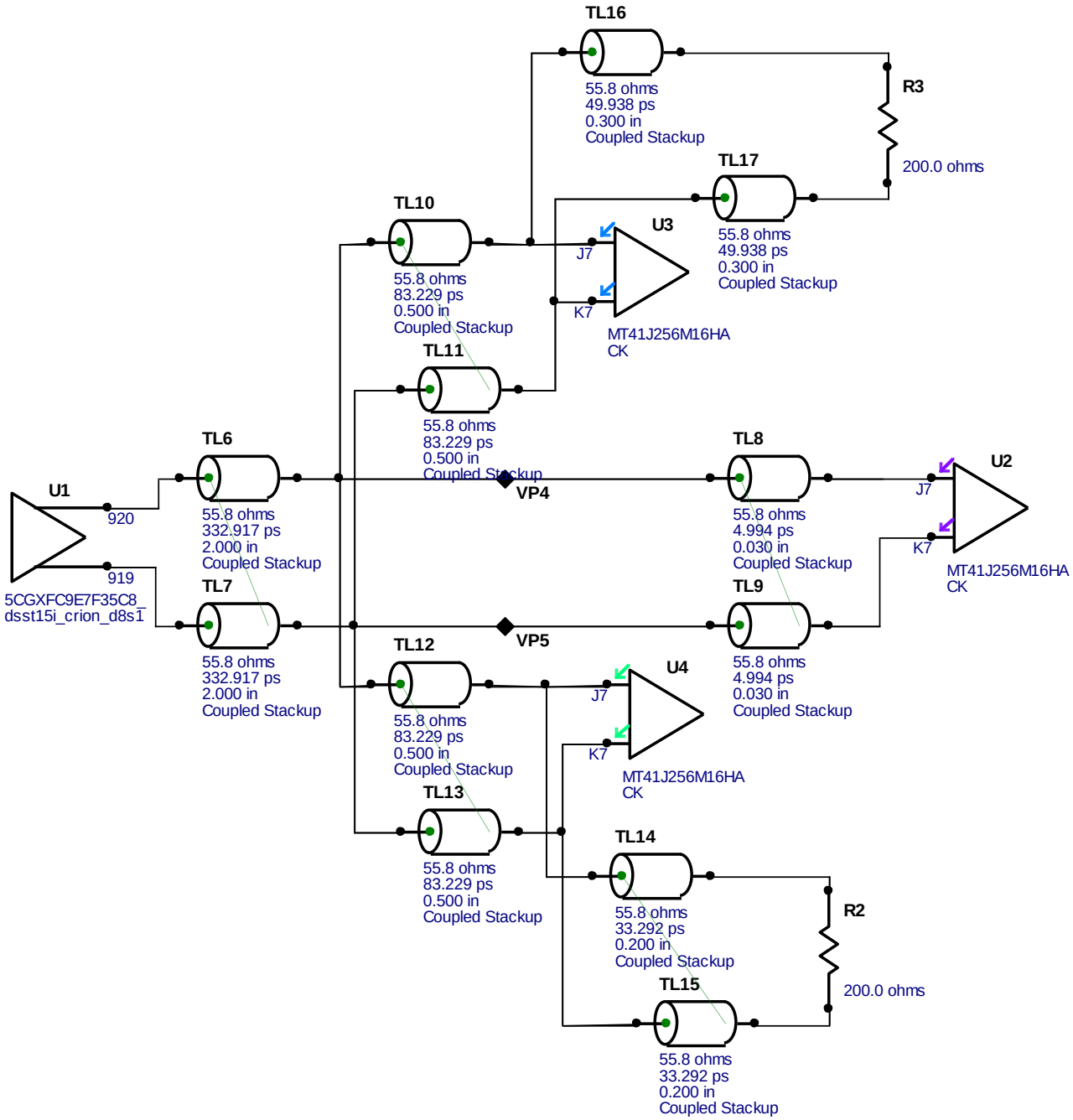
Distance B lengths, from the central memory to either side memory, must be matched within 10mils for a given net.

Distance C lengths are arbitrary. They should be just as long as needed to reach the termination.

HMC Pre-layout simulations for Clocks

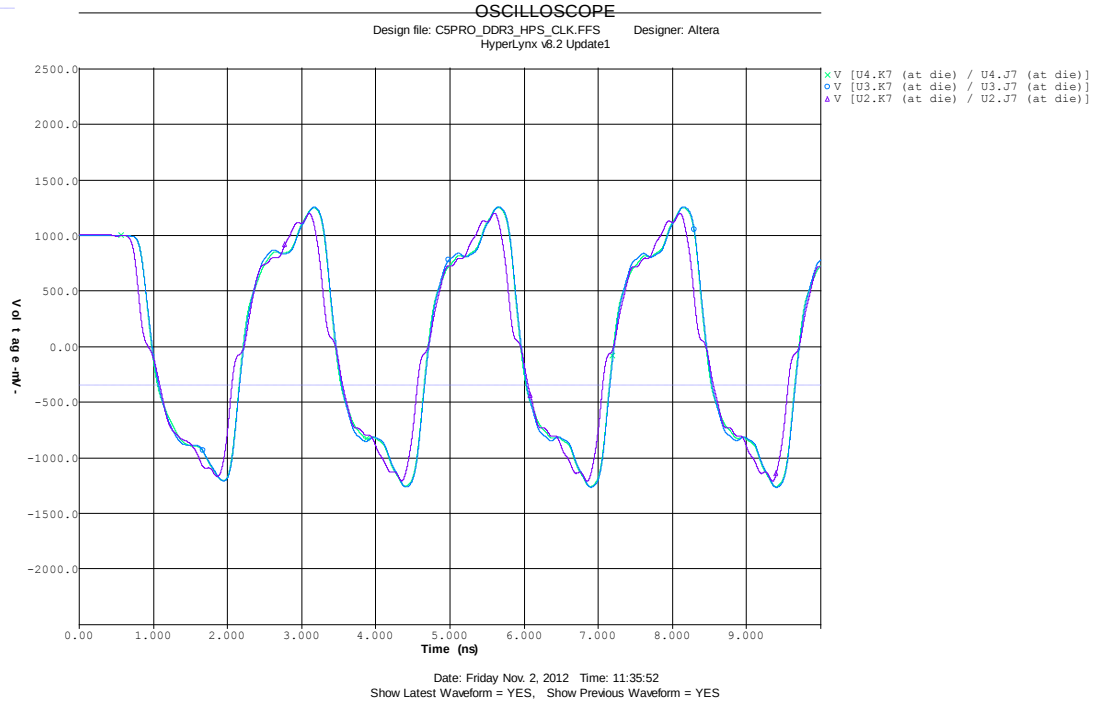
This system uses the same topology but with differential lines.

Design File: c5pro_ddr3_hps_clk.ffs
HyperLynx LineSim v8.2 Update1



Simulation using 8ma drivers

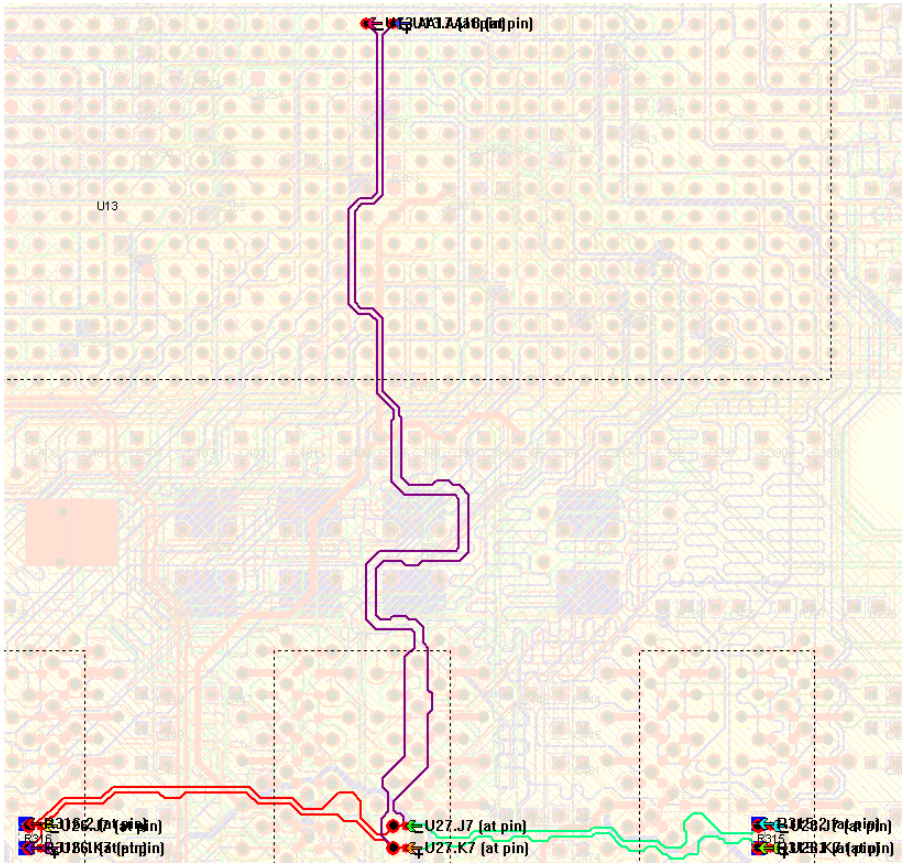
Same drive as the address and command lines



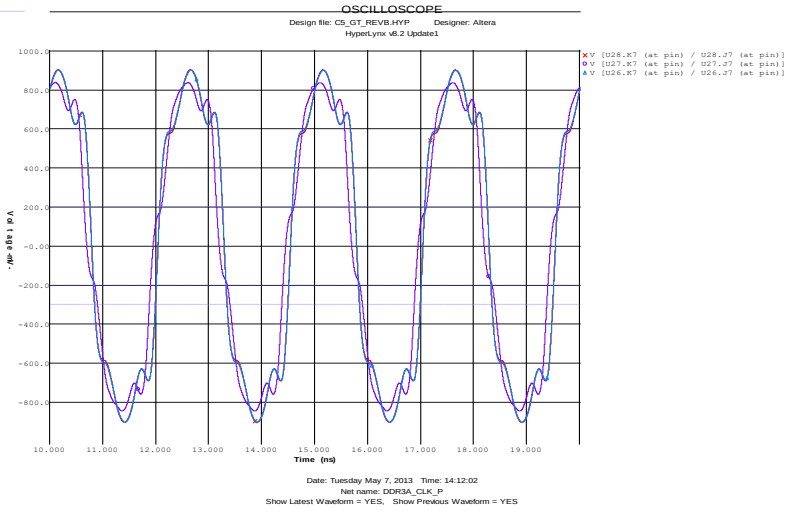
8ma is OK for this too.

HMC Post Layout Simulations for the Clock

The following simulations were created using the final artwork as a source for data.



With 8ma driver the simulation looks like this:



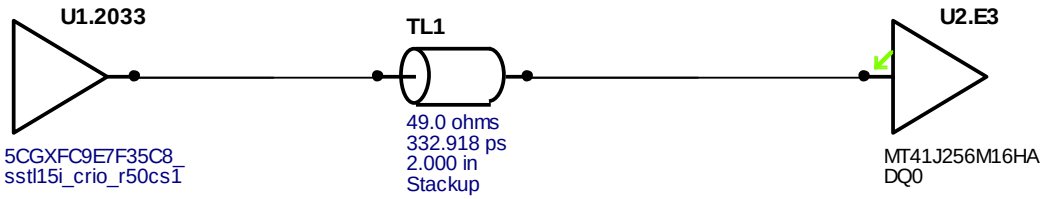
DQ and DQS Topology

The DQ and DQS signals are very unlike the Address, Command and Clock signals. They are only point to point bidirectional signals either single ended or differential. The FPGA and the DDR3 devices both can provide series terminated outputs and parallel terminated inputs depending on whether they are driving or receiving. This allows a lot of flexibility so designing can get out of hand. The best thing to do is to decide the topology to use based on whatever parameters are called out for the design. Driving the signals with series termination on the outputs and using minimal termination on the receiving end will give the lowest overall power. Series drive termination also causes the minimum amount of crosstalk.

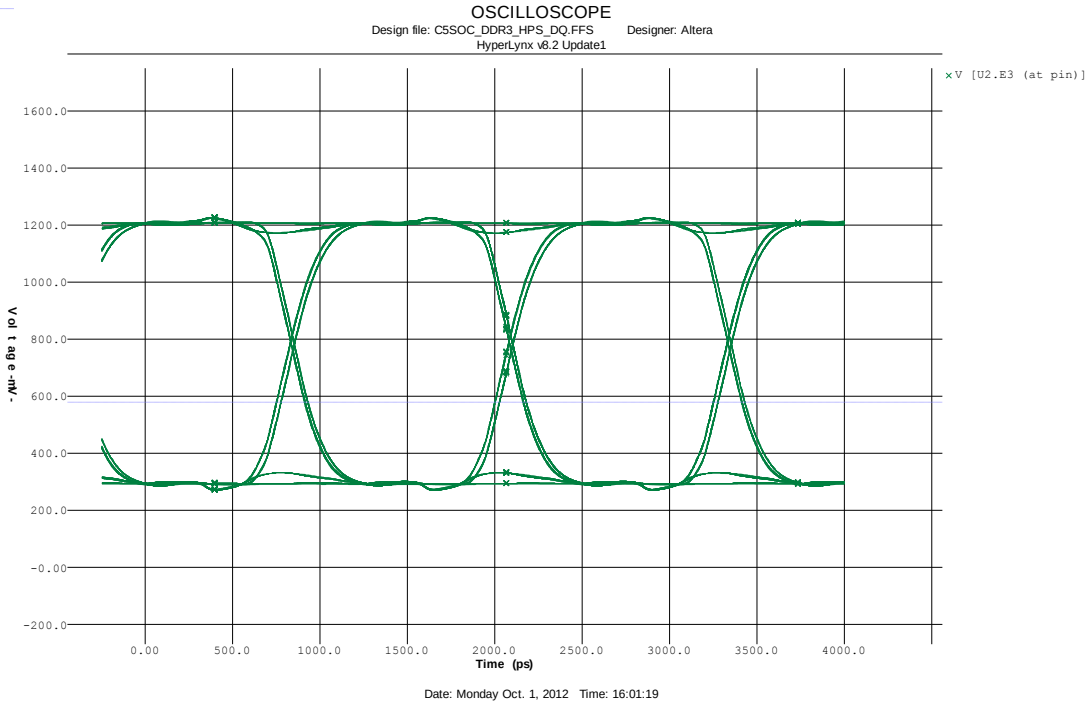
Pre-Layout Simulation for DQ systems

DQ FPGA -> Memory

Design File: c5soc_ddr3_hps_dq.ffs
HyperLynx LineSim v8.2 Update1

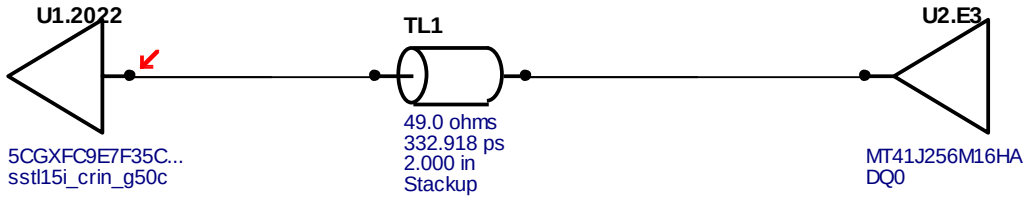


Here the driver is set for 50 Ohm series termination. The receiving end is set up for 60 Ohm ODT.

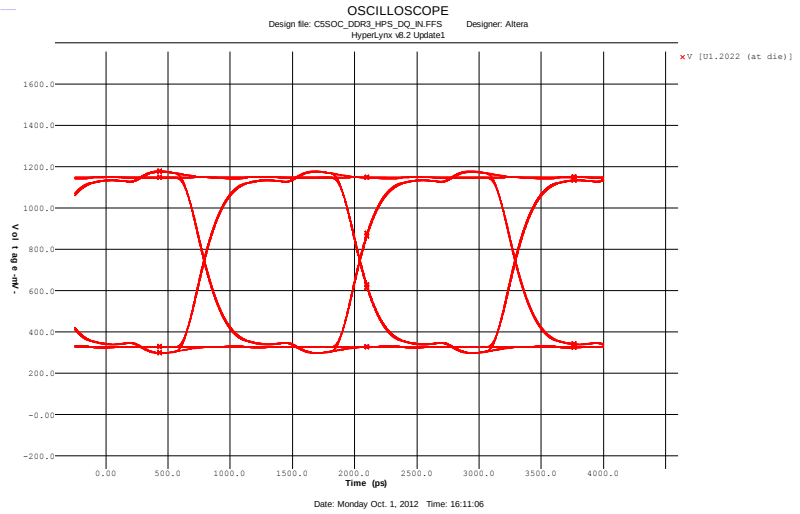


DQ Memory -> FPGA

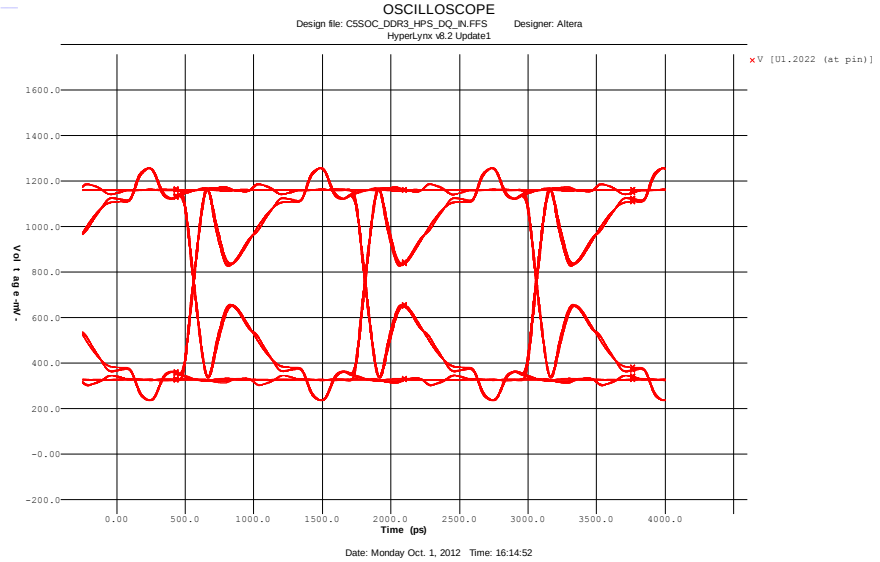
Design File: c5soc_ddr3_hps_dq_in.ffs
HyperLynx LineSim v8.2 Update1



This simulation with 40 Ohm output from the DDR chip and 50 Ohm termination on the receive end. These simulations show the signal at the die.

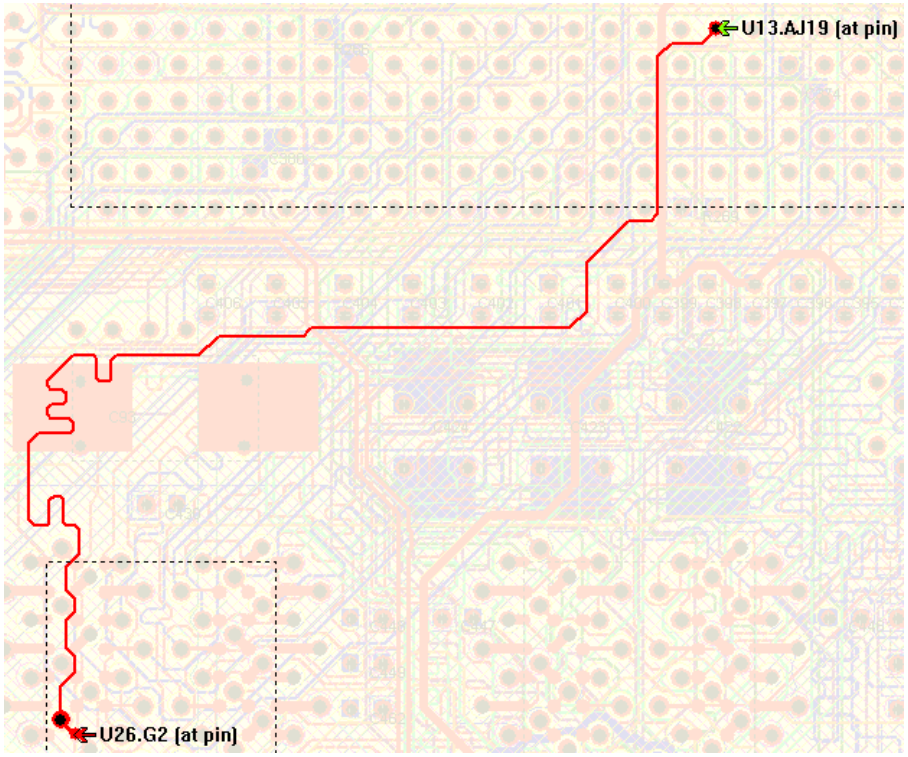


This shows the distortion of the signal at the ball of the device.

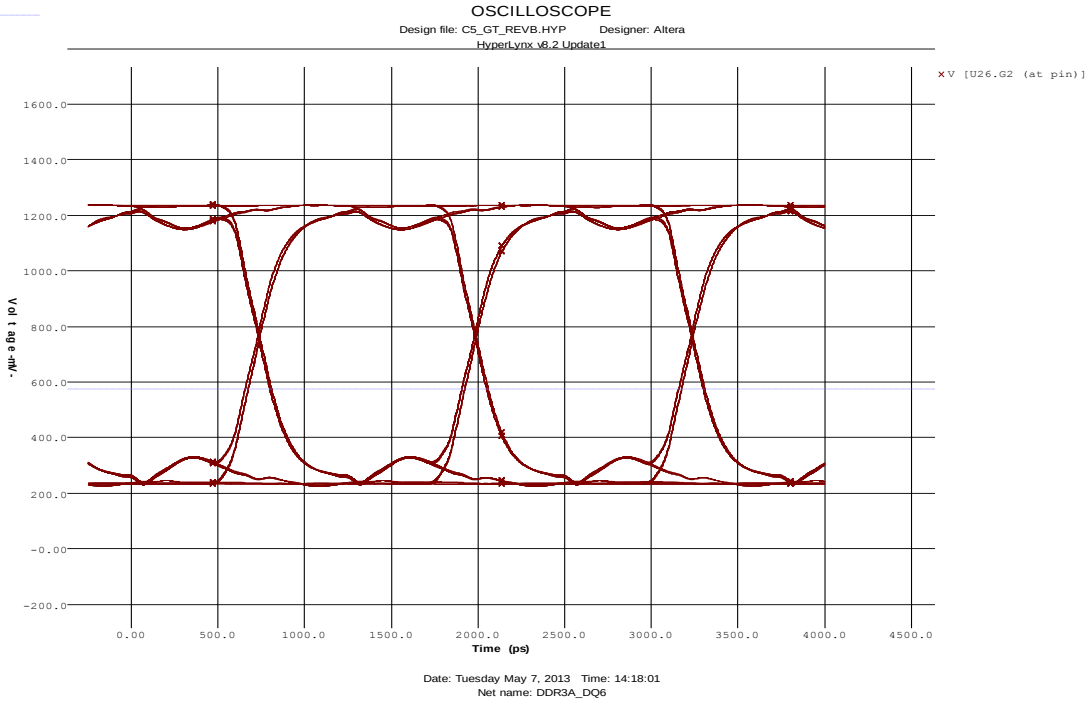


Post Layout Simulation for DQ systems

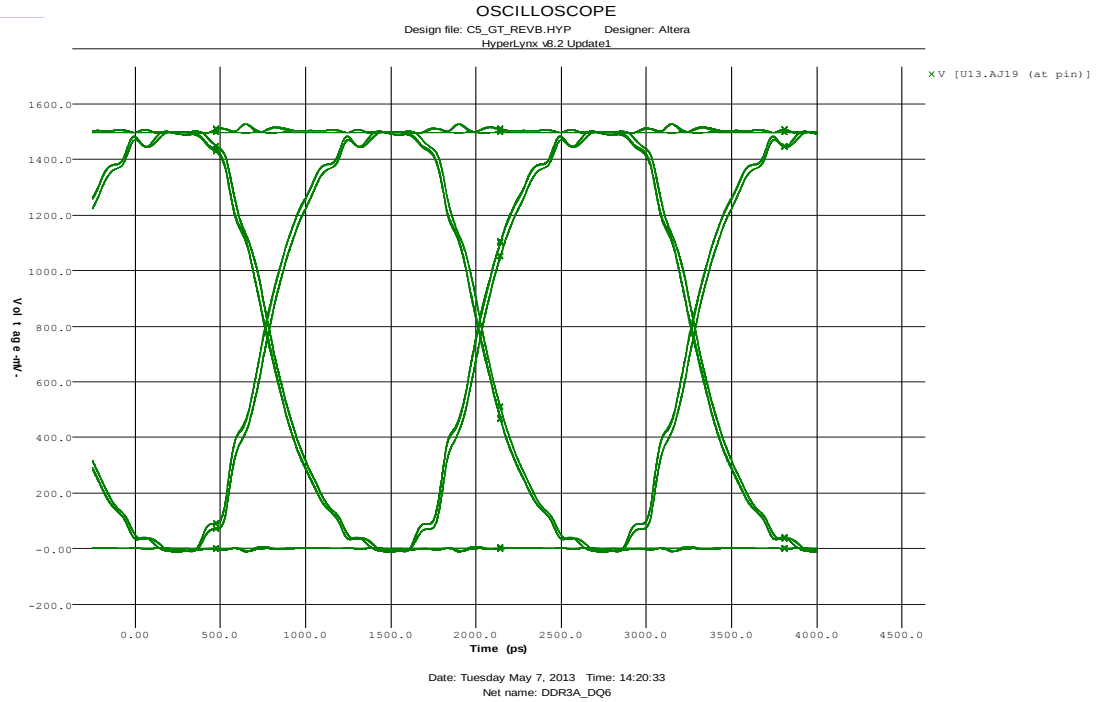
The following simulations were created using the final artwork as a source for data.



Simulation to memory with drives as above

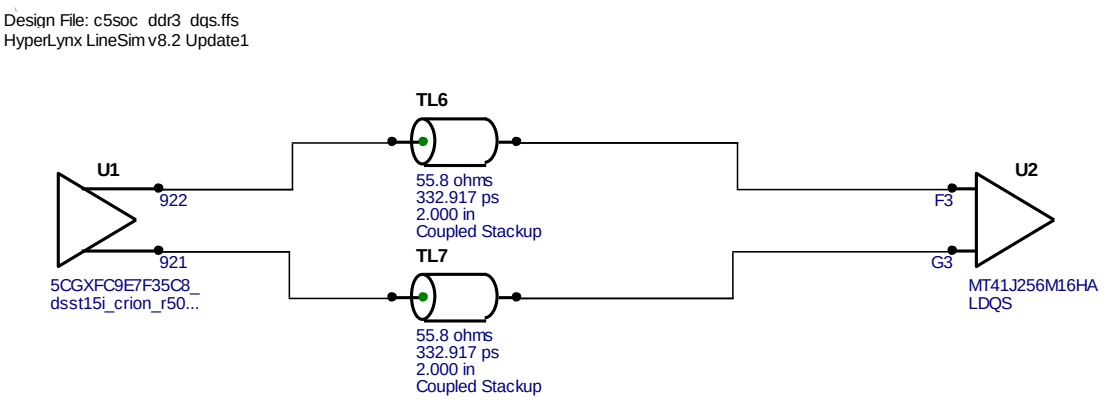


Simulation form the Memoy to the FPGA with drive as above

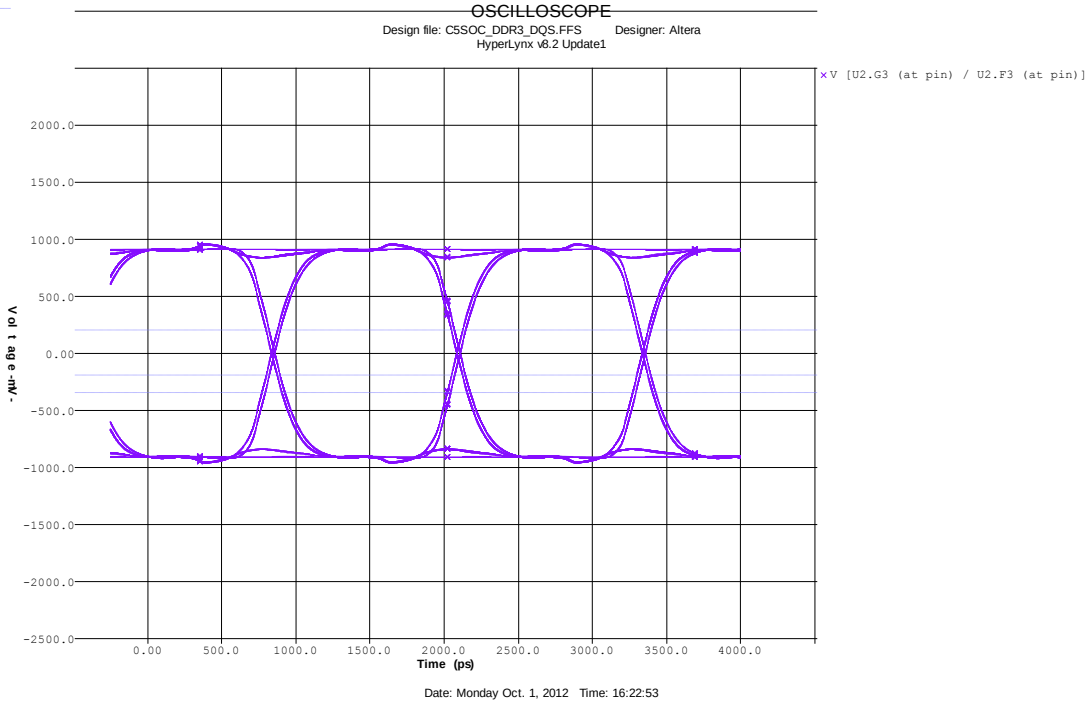


Pre-Layout Simulation for DQS systems

DQS FPGA -> Memory



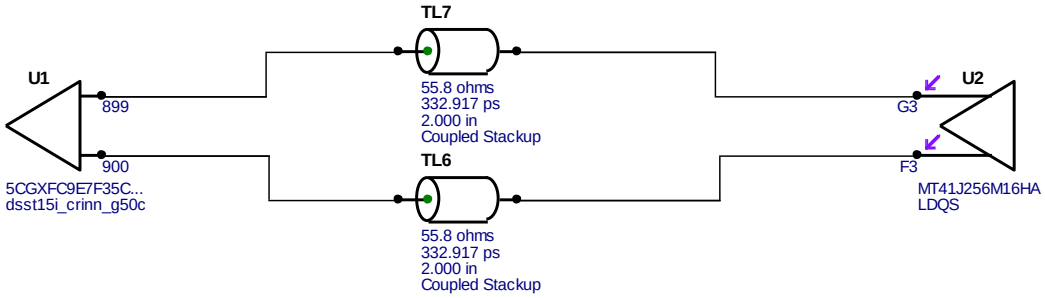
This simulation ran with 50 Ohm ODT drive from FPGA and 60 Ohm OCT termination on the Memory



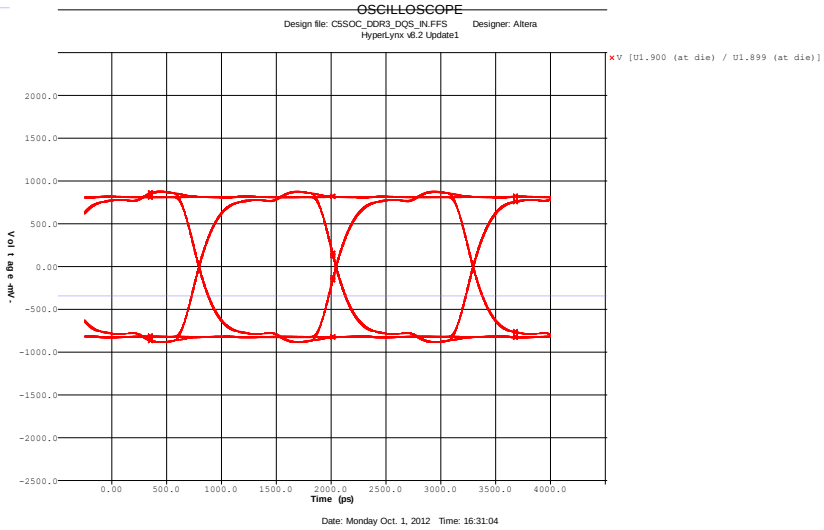
DQS Memory -> FPGA

The driver used is the same strength as the driver for the DQ system. On the receive side it is a 50 Ohm ODT.

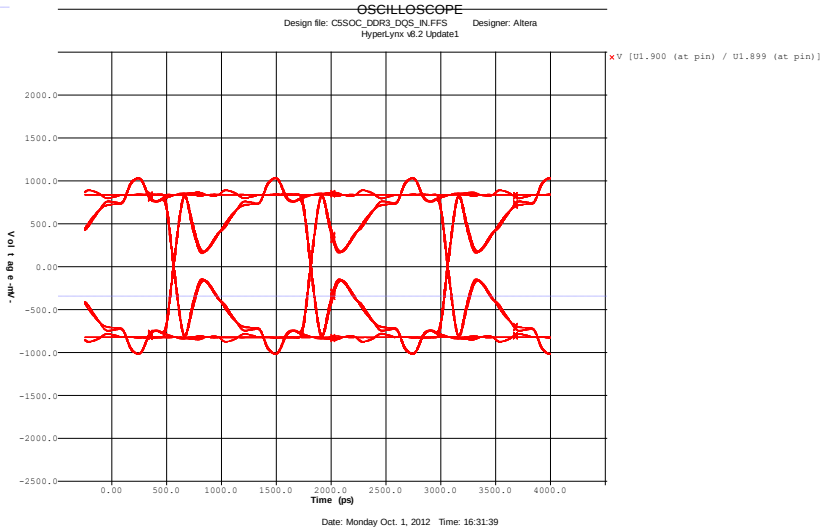
Design File: c5soc_ddr3_dqs_in.ffs
HyperLynx LineSim v8.2 Update1



At the die…



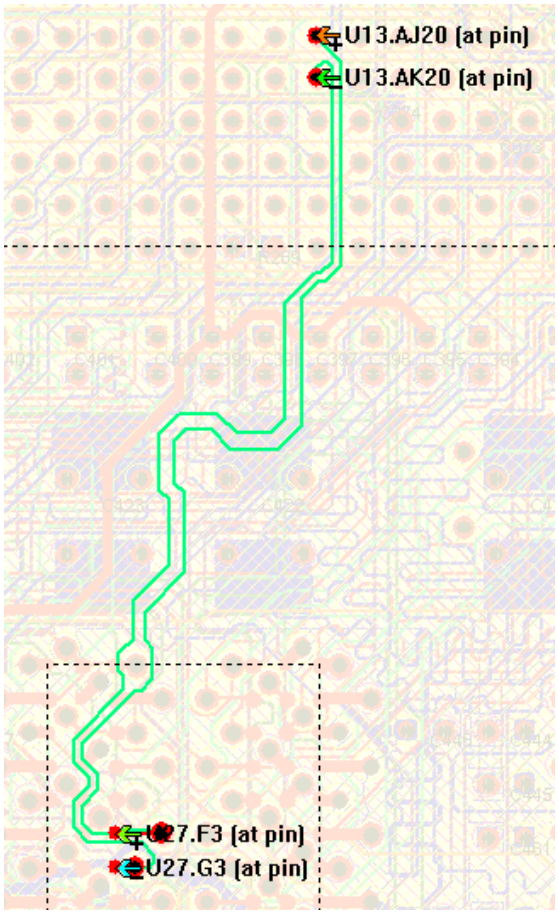
At the pin…



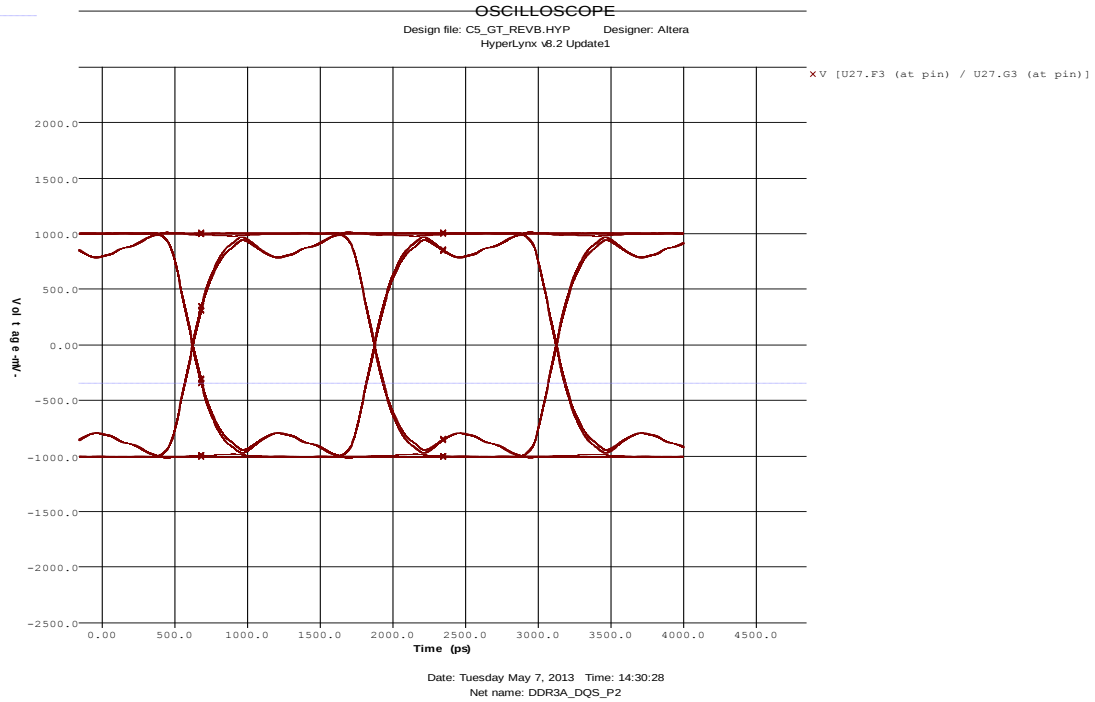
Post Layout Simulation for DQS systems

The following simulations were created using the final artwork as a source for data.

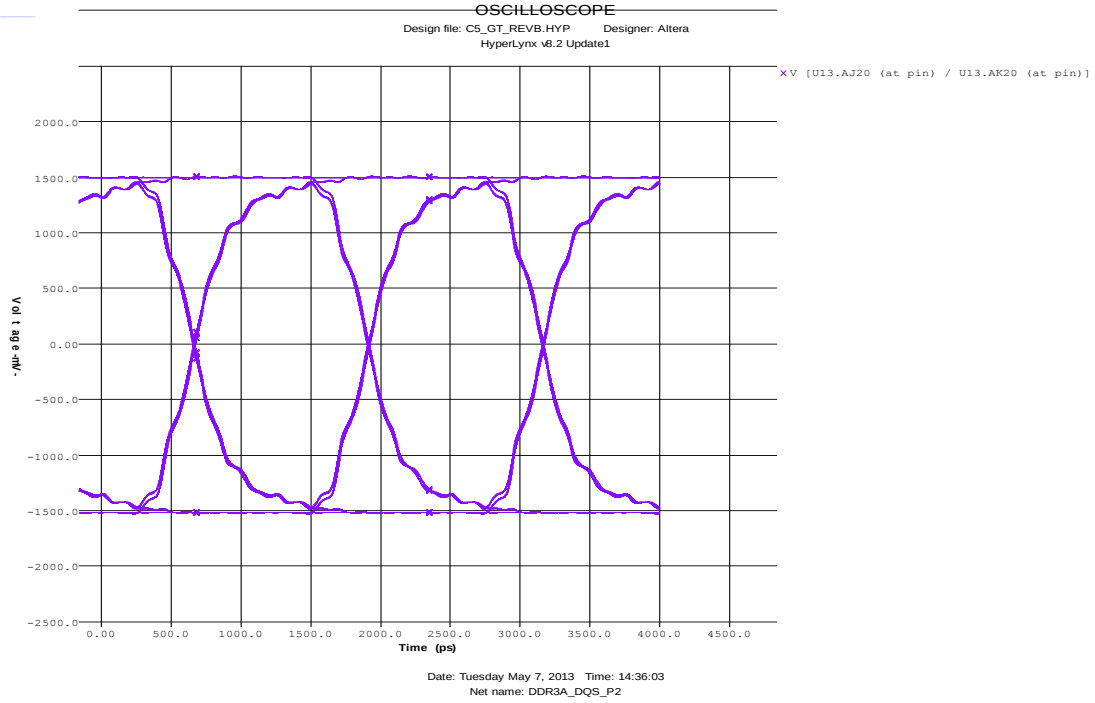
Topology



Simulation to memory from FPGA with the above settings



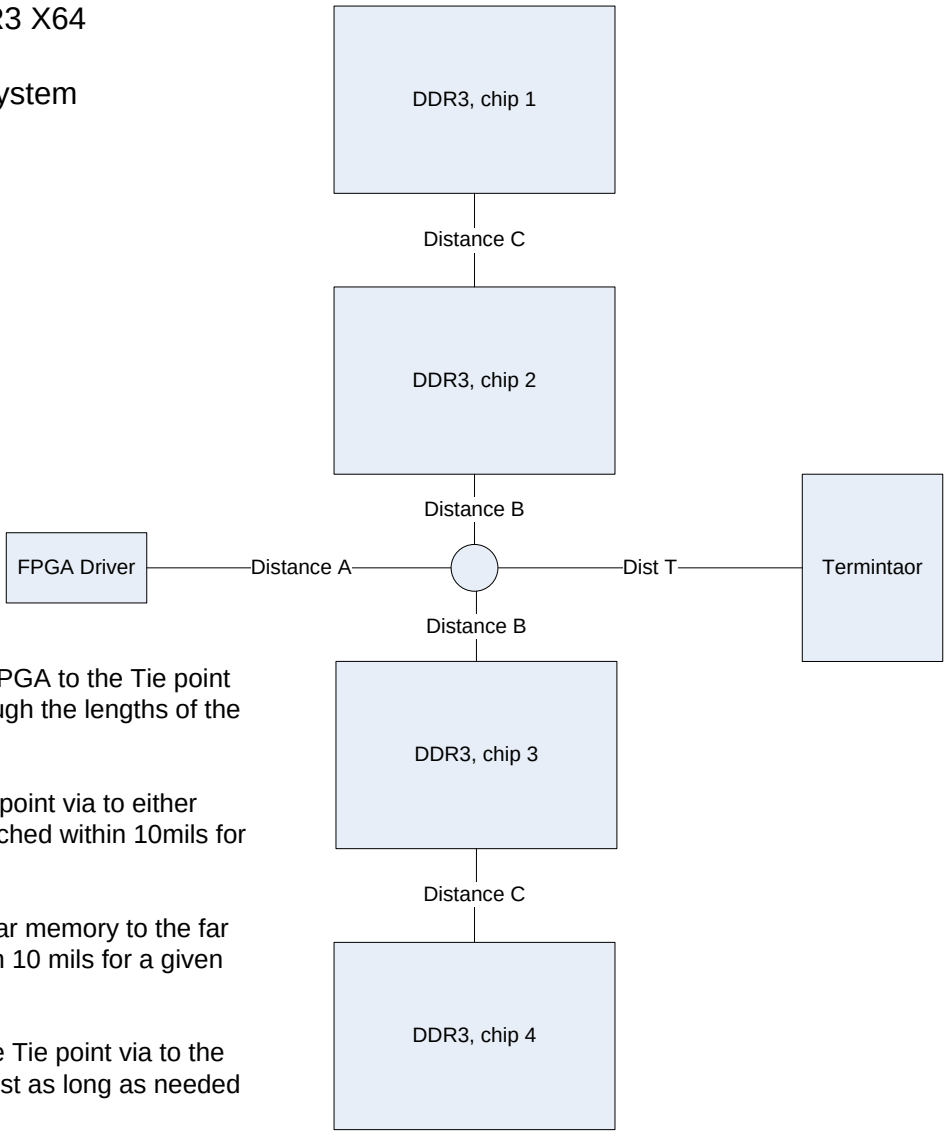
Simulation to FPGA from memory with the above settings



DDR3B X64 Soft Memory Controller Simulations

SMC Address and Command Topology

Cyclone V GT Board DDR3 X64 Soft Memory Controller Address and Command system topology



In this diagram:

Distance A is the run from the FPGA to the Tie point via. This can be any length though the lengths of the group must be matched.

Distance B lengths, from the tie point via to either near side memory, must be matched within 10mils for a given net.

Distance C lengths, from the near memory to the far memory must be matched within 10 mils for a given net.

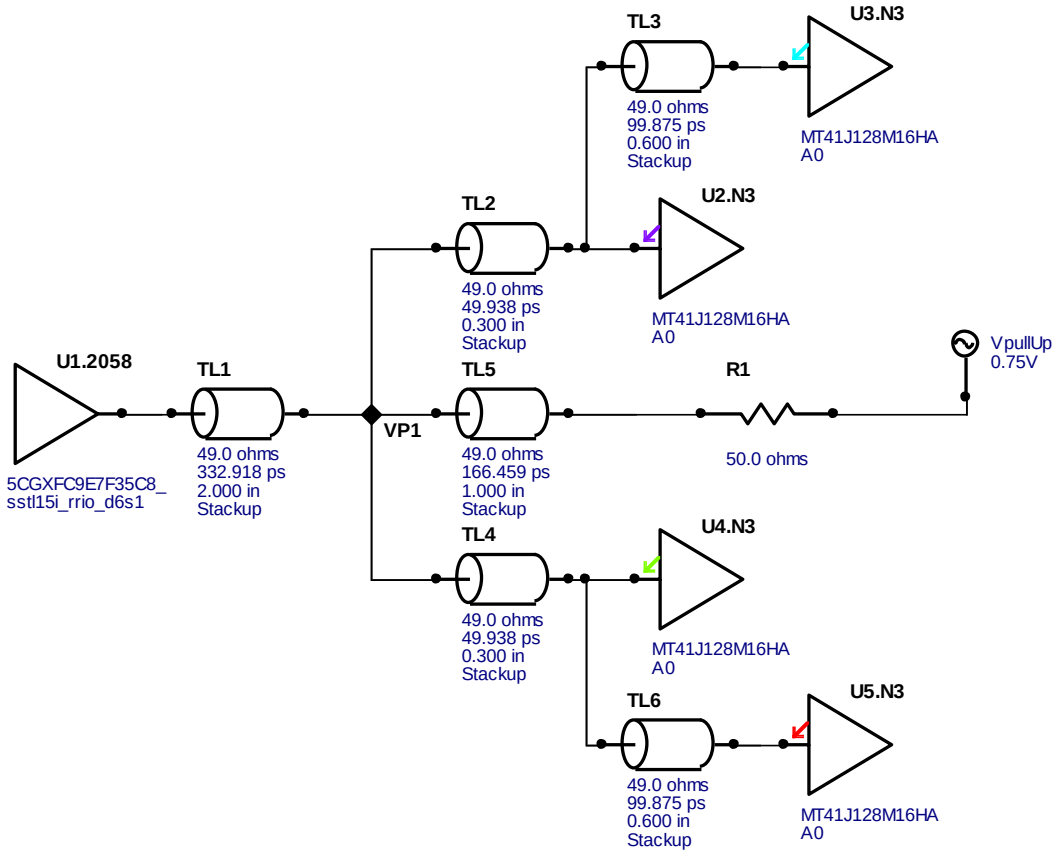
Distance T is the length from the Tie point via to the termination resistor. It can be just as long as needed to reach the termination.

Some things need to be said about this topology for clarity.

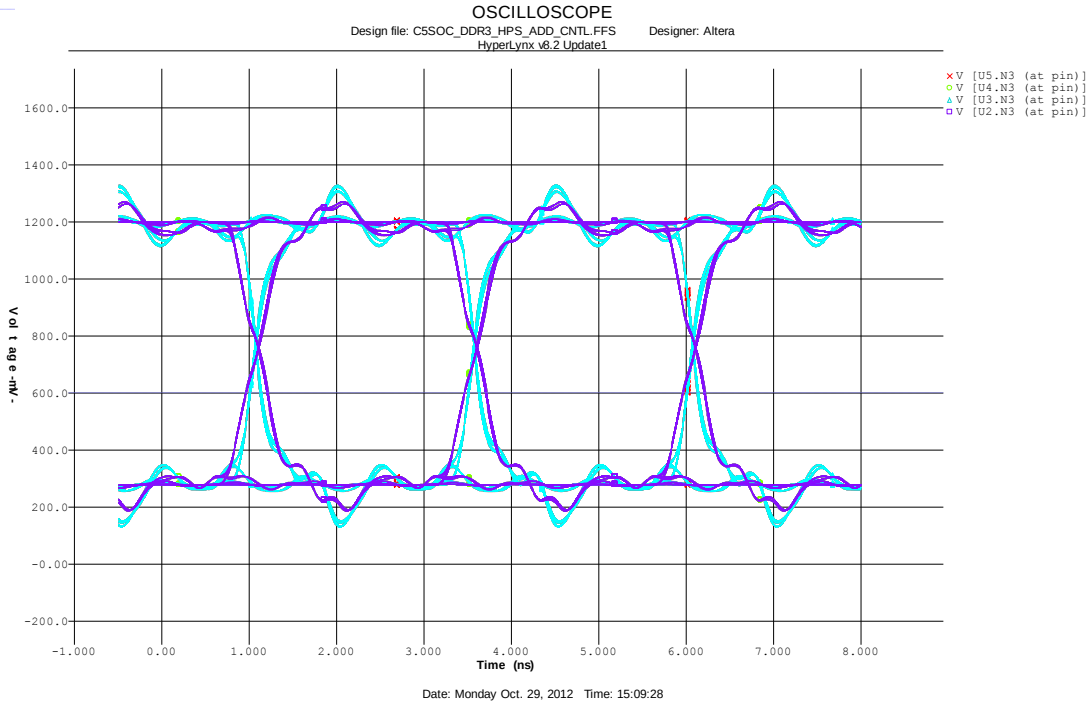
- It is critical that the sum of distances from the FPGA to DDR3 chips 2 and 3 be matched within 10 mils
- It is critical that the sum of distances from the FPGS to DDR3 chips 1 and 4 be matched within 10 mils
- The distance "T" can be any length but shorter is better match all distance "T" values within 200 mils

Simulation Schematic

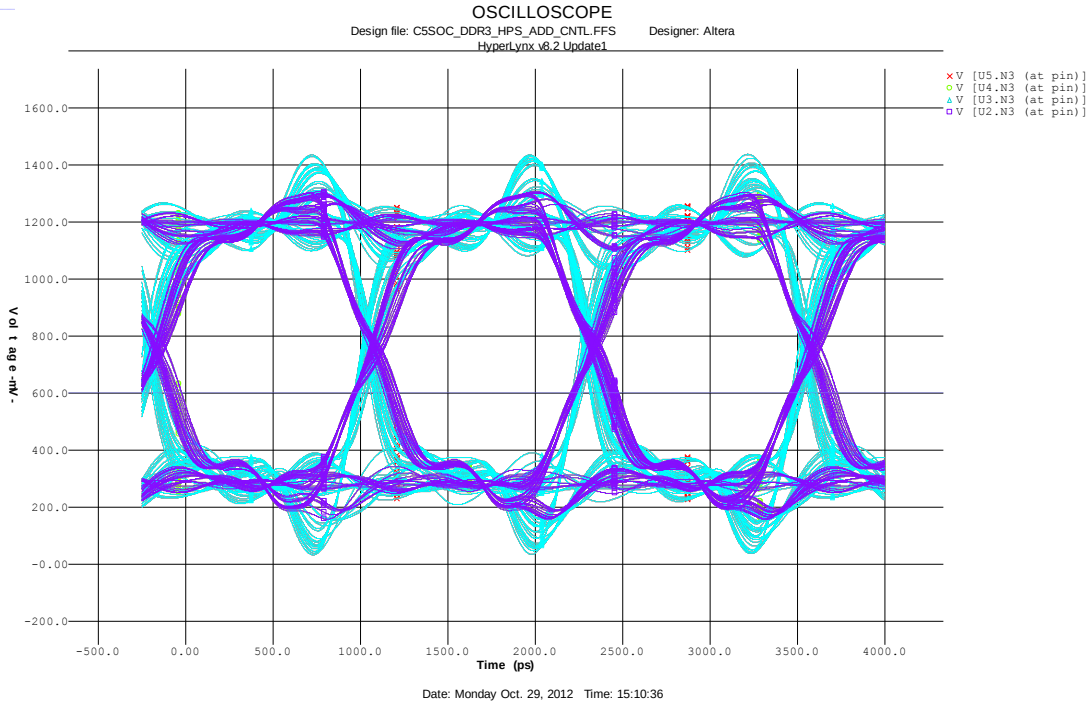
Design File: c5soc_ddr3_hps_add_cntl.ffs
HyperLynx LineSim v8.2 Update1



Results for 400MHz SDR Address and Most Control Lines

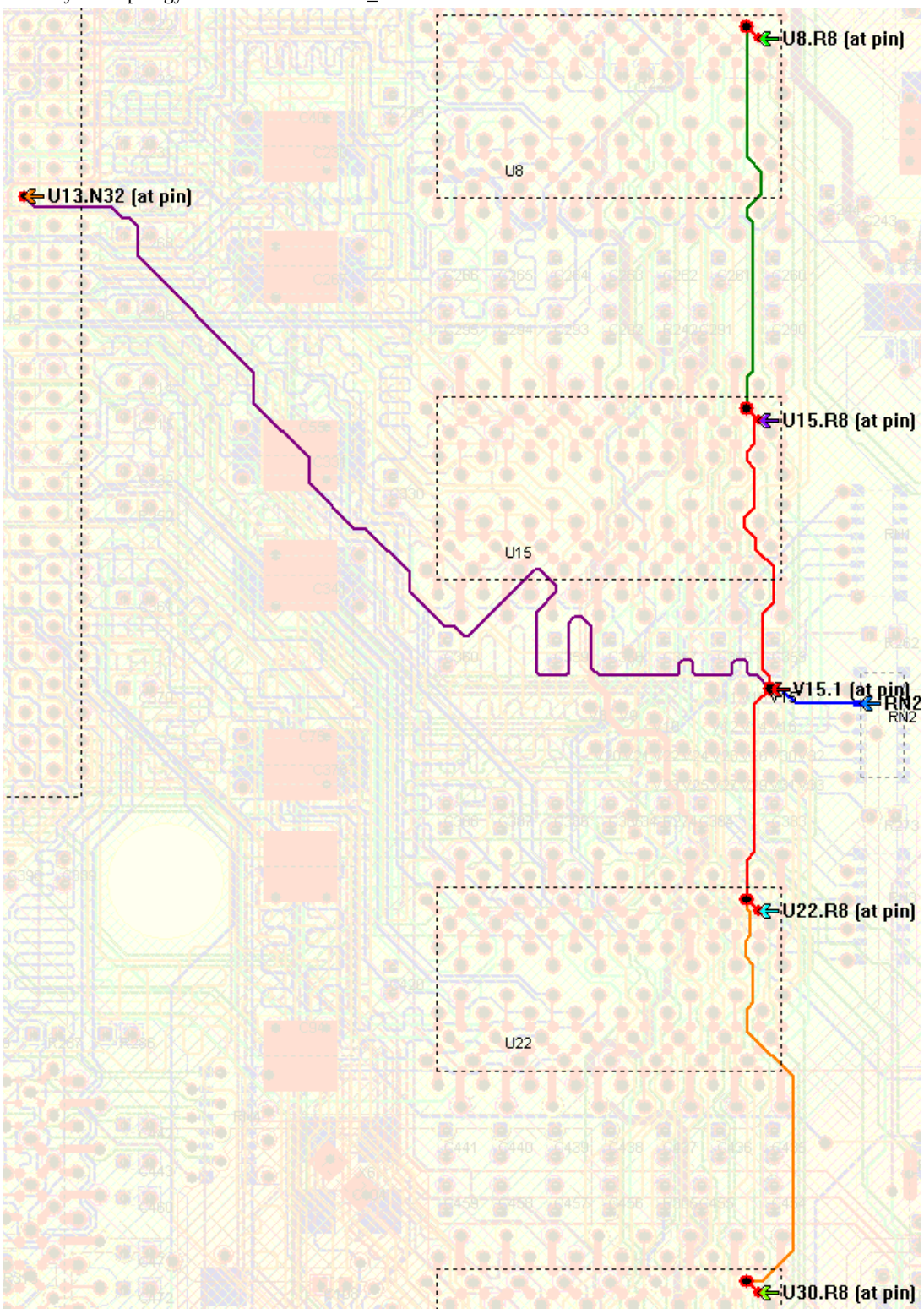


Results for 400MHz DDR control lines

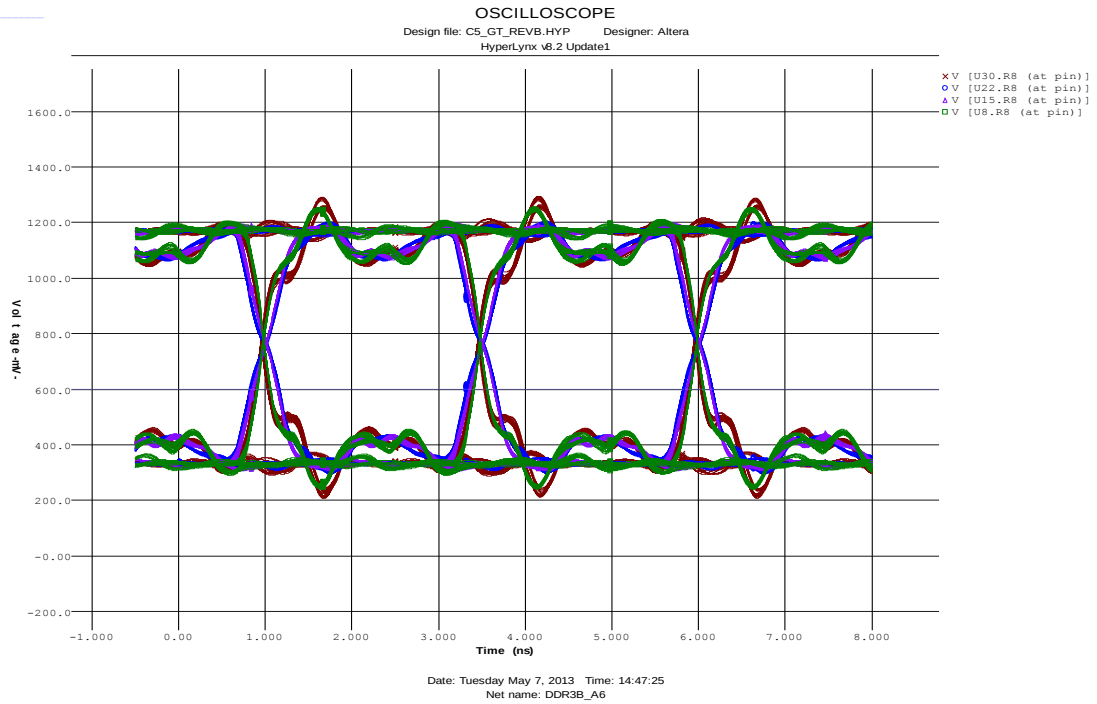


Nice eyes. Use 6ma drive for all Address and Control signals, no overshoot but good opening.

Post Layout Topology Address line DDR3B_A6

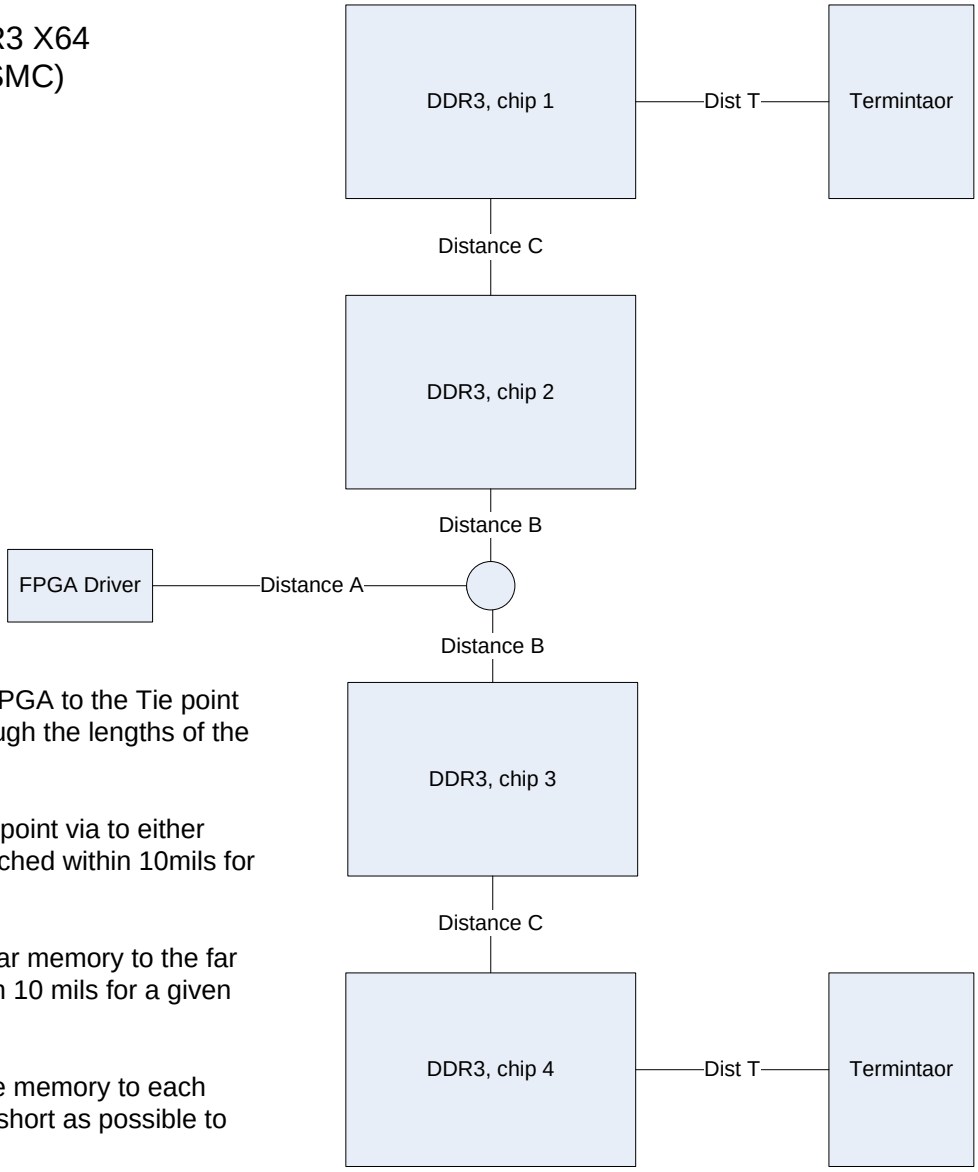


Simulation with above drive strength



SMC Clock lines out to the memory

Cyclone V GT Board DDR3 X64 Soft Memory Controller (SMC) Clock topology



In this diagram:

Distance A is the run from the FPGA to the Tie point via. This can be any length though the lengths of the group must be matched.

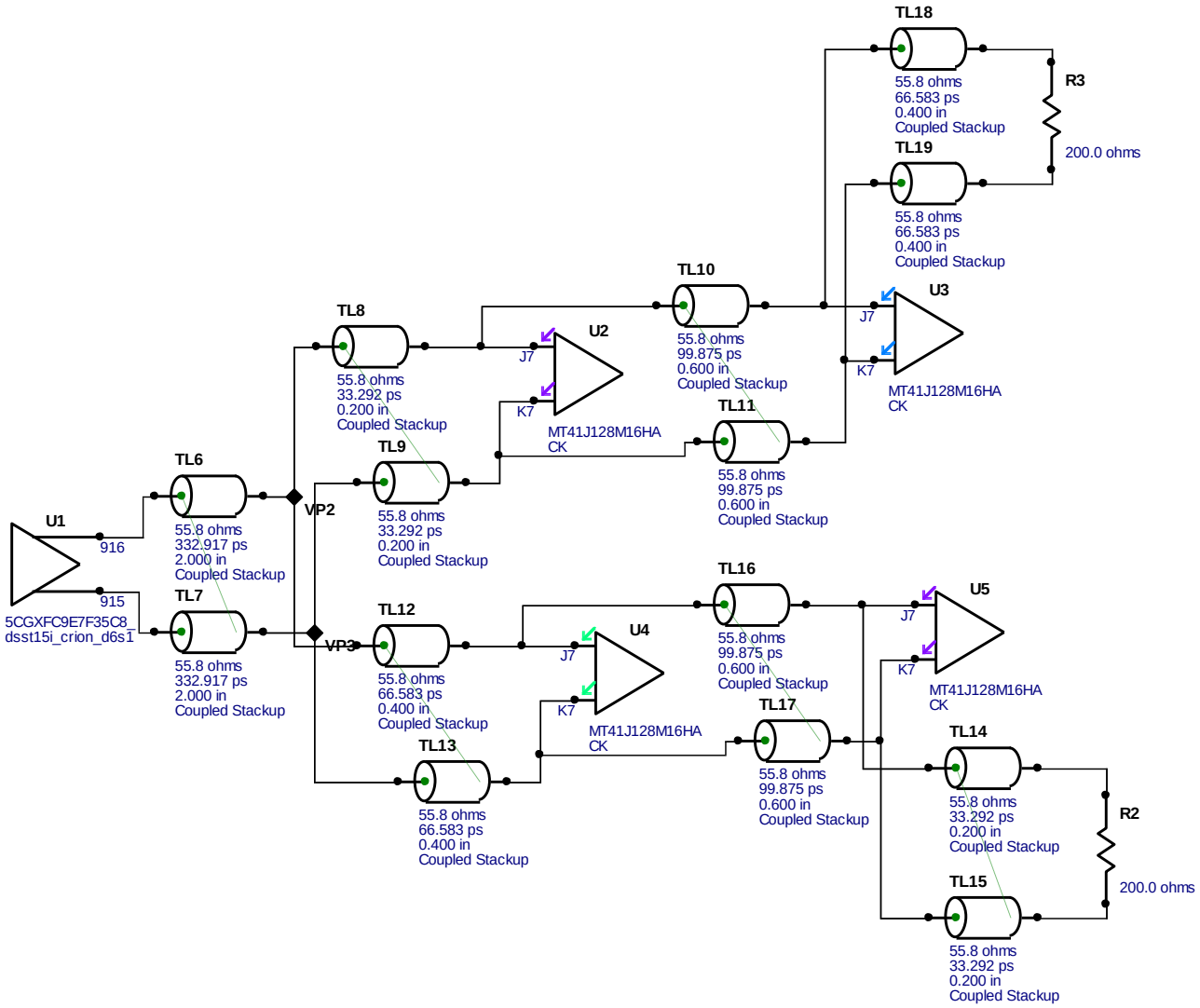
Distance B lengths, from the tie point via to either near side memory, must be matched within 10mils for a given net.

Distance C lengths, from the near memory to the far memory must be matched within 10 mils for a given net.

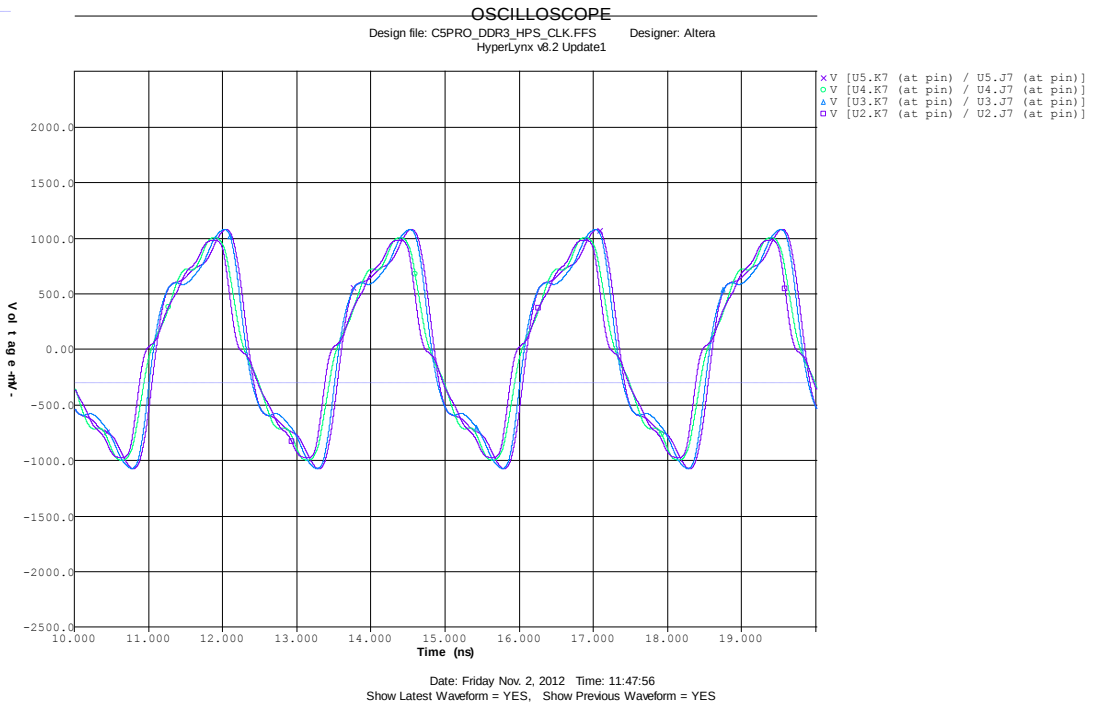
Distance T is the length from the memory to each termination resistor. It must be short as possible to reach the termination.

Simulation Schematic

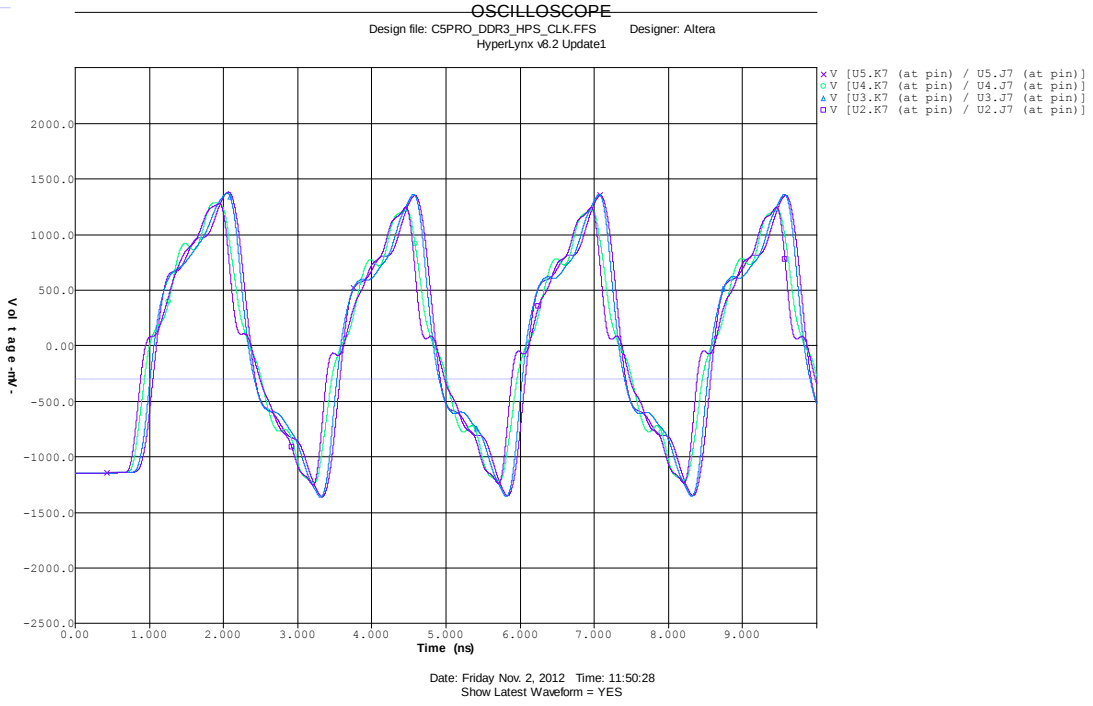
Design File: c5pro_ddr3_hps_clk.ffs
HyperLynx LineSim v8.2 Update1



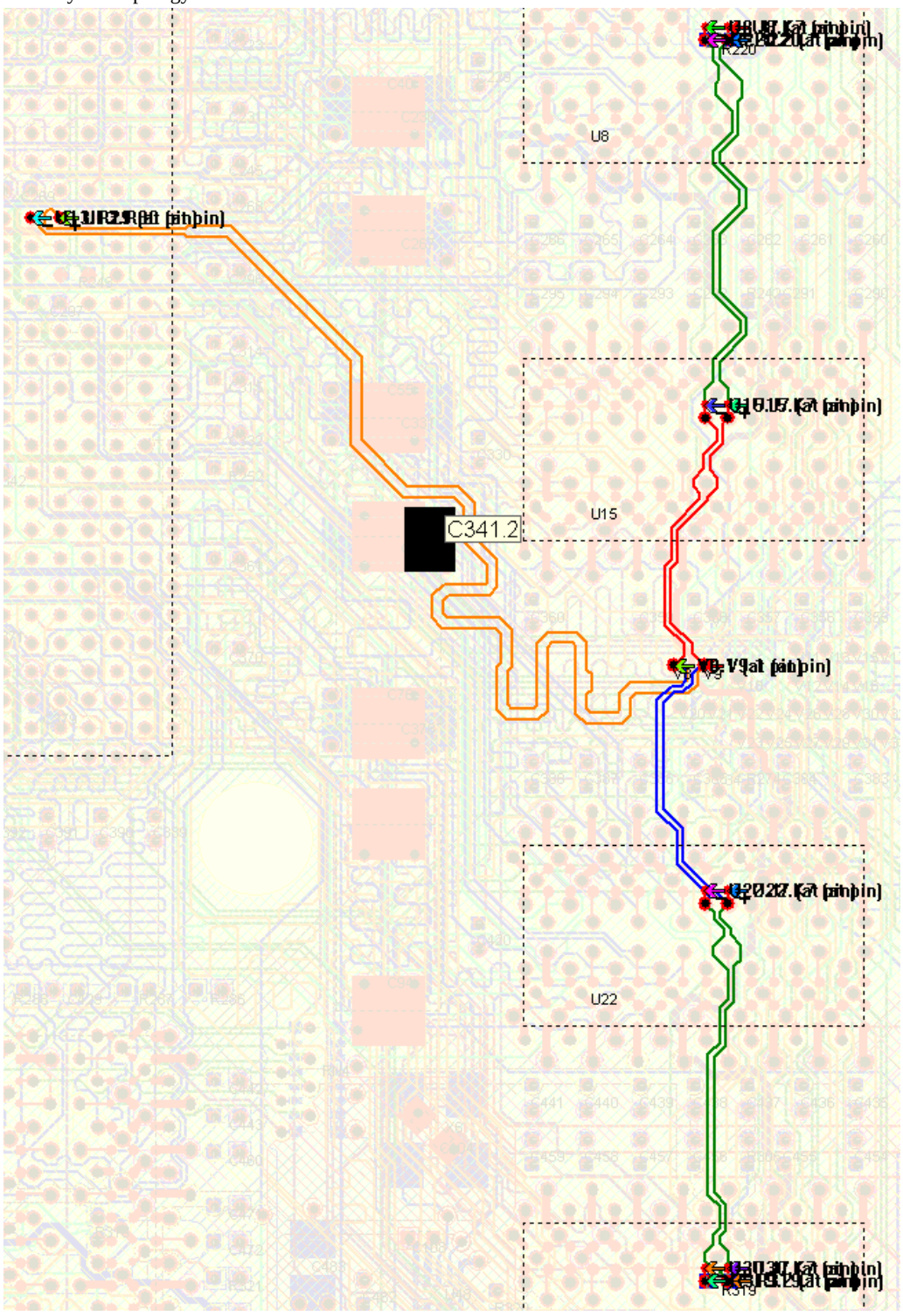
400MHz clock simulation



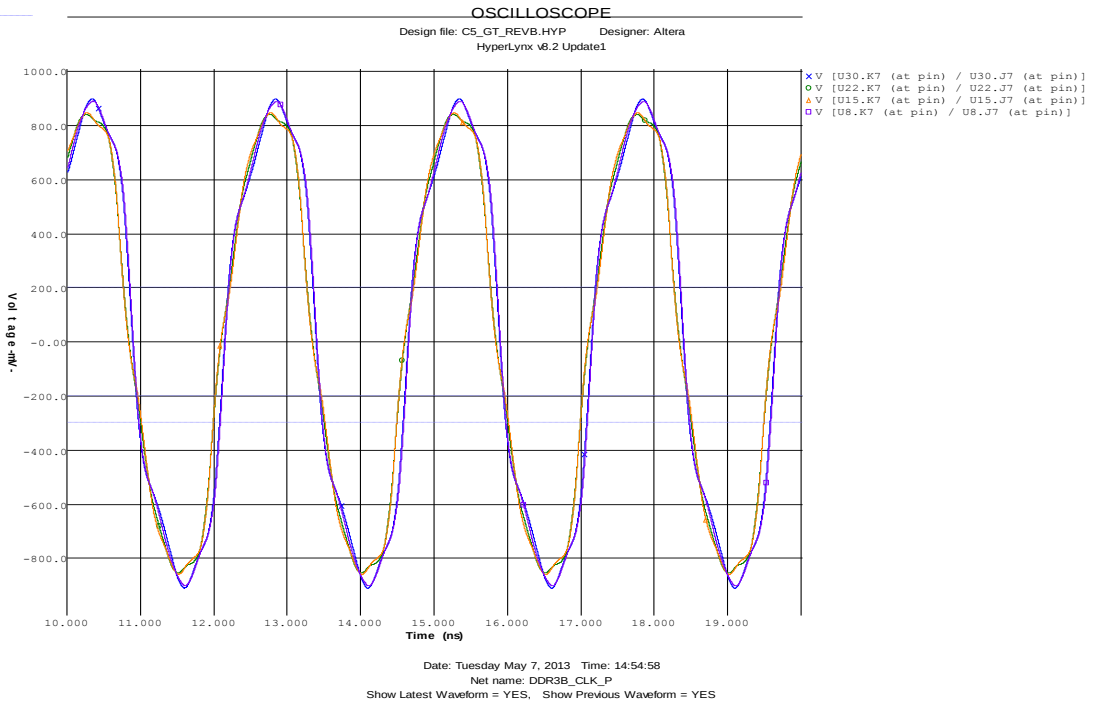
This is also good at 6ma drive strength, more current just makes it sloppy and kinky.



Post Layout Topology for clock line



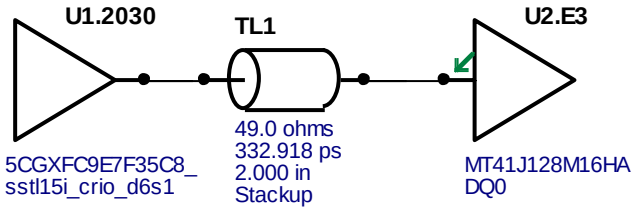
Simulation with above drive strength



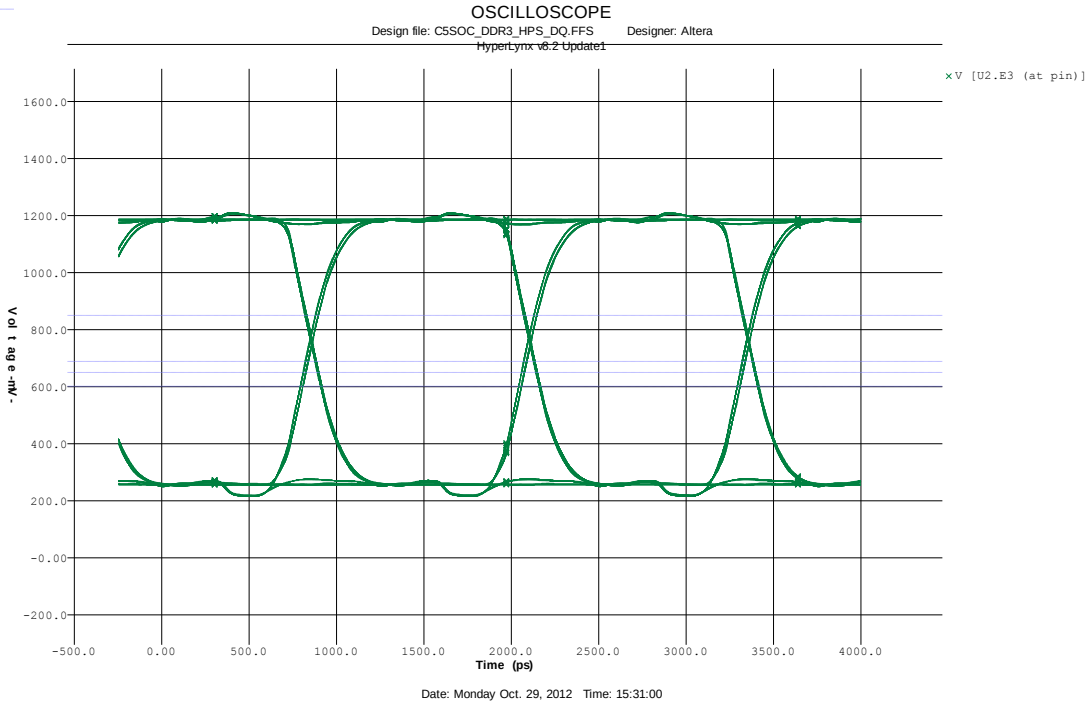
DQ System

Topology Schematic, signal out to memory.

Design File: c5soc_ddr3_hps_dq.ffs
HyperLynx LineSim v8.2 Update1

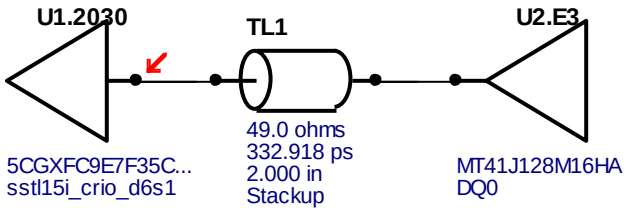


Simulation Results

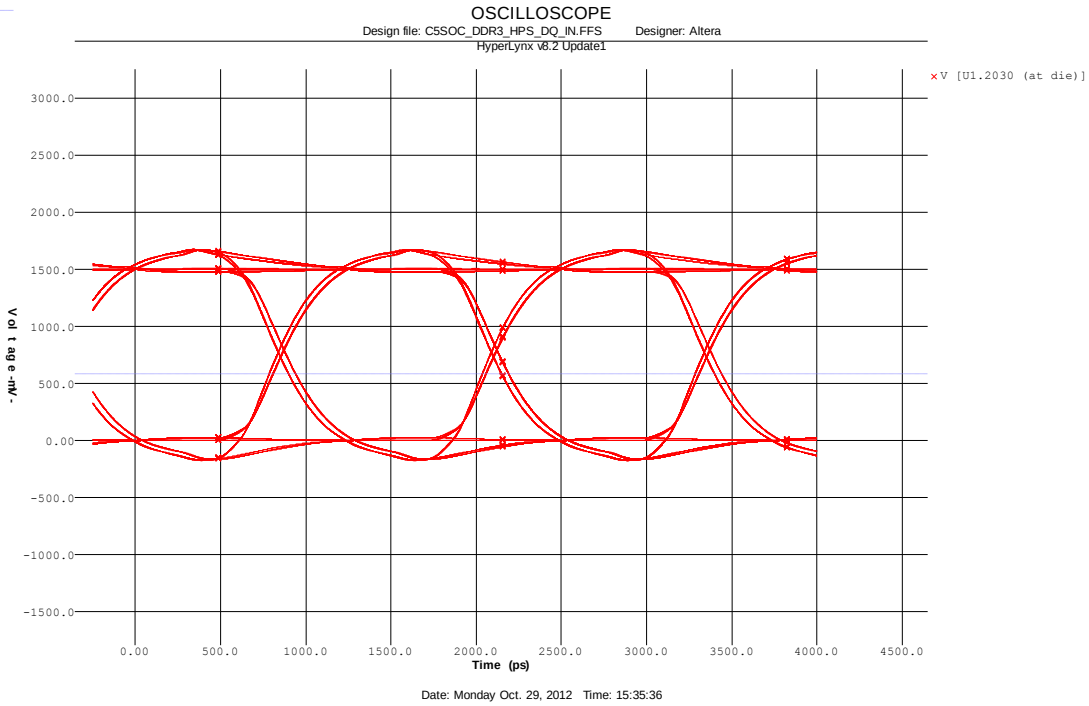


Topology Schematic, signal in from memory.

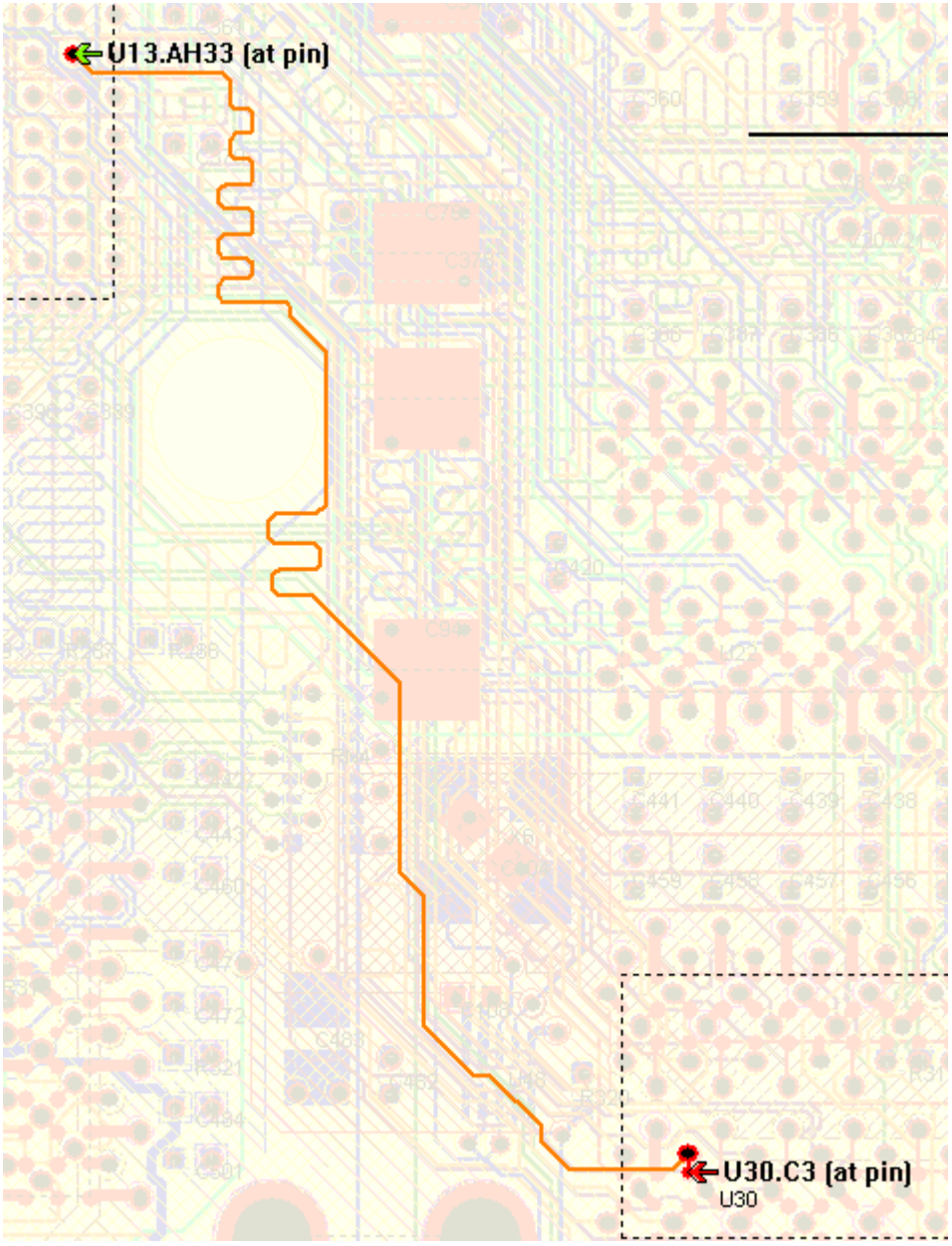
Design File: c5soc_ddr3_hps_dq_in.ffs
HyperLynx LineSim v8.2 Update1



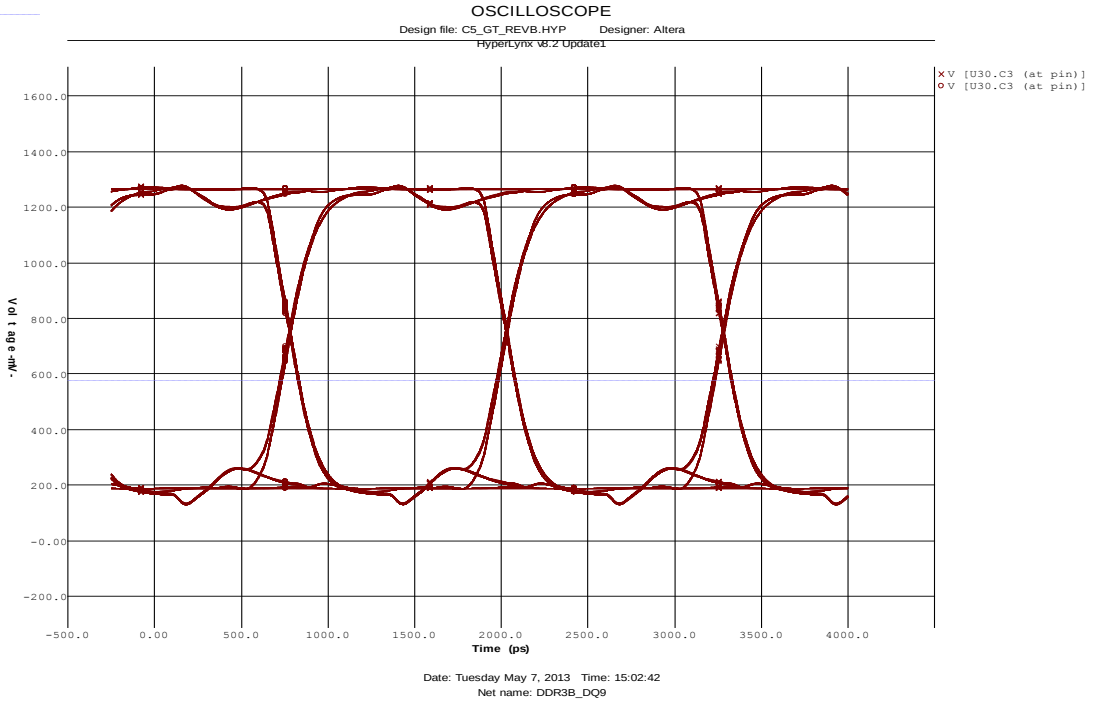
Simulation Results



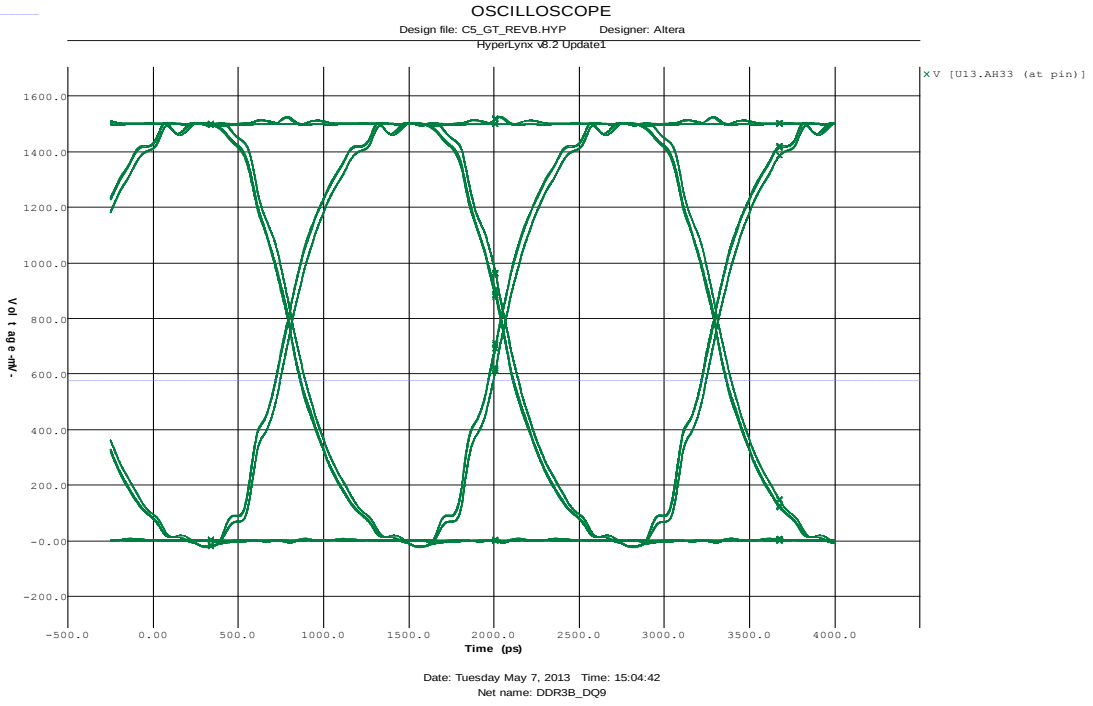
Post-layout DQ9 topology is shown here



Simulation of DDR3B_DQ9 to the memory with above drive strengths was executed to produce this graph:



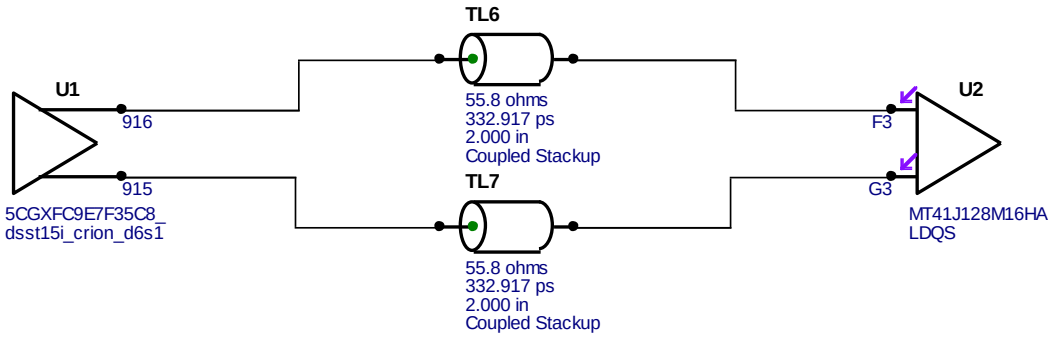
The same topology being driven by the memory device back to the FPGA



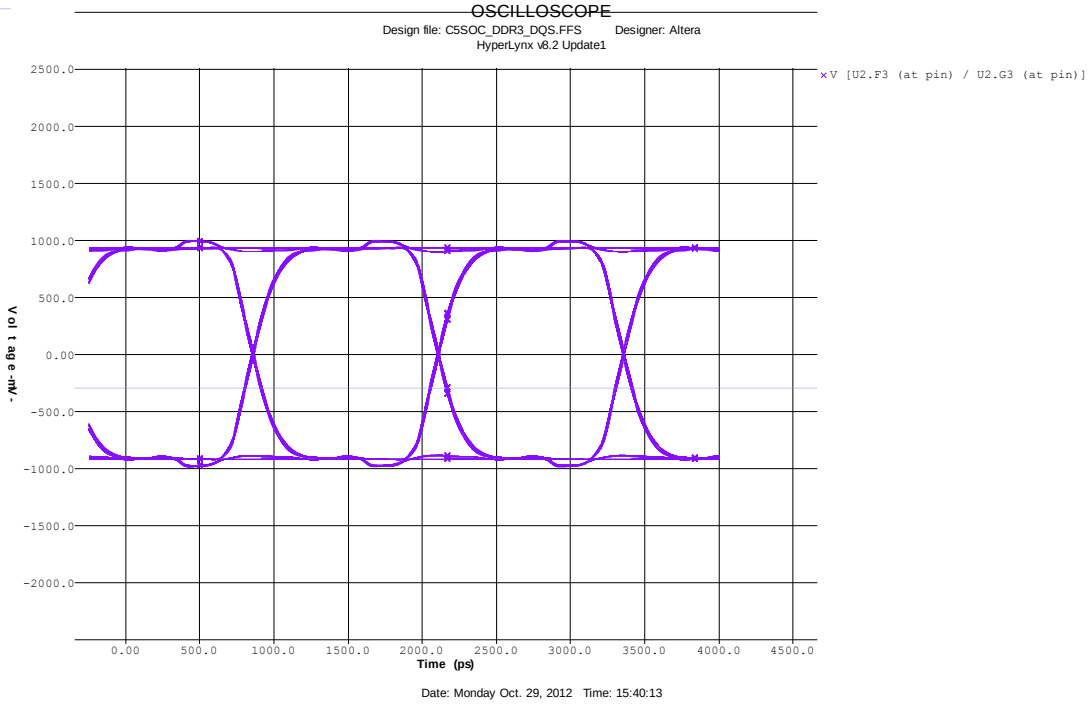
DQS System

Topology Schematic, signal out to memory.

Design File: c5soc_ddr3_dqs.ffs
HyperLynx LineSim v8.2 Update1

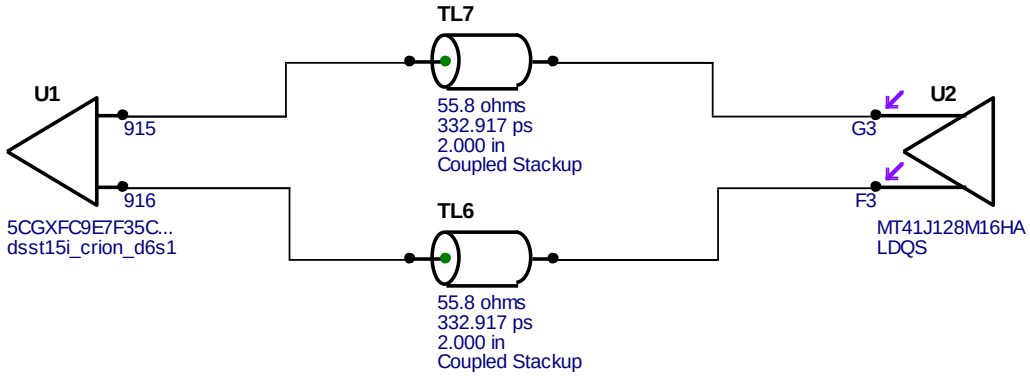


Simulation results

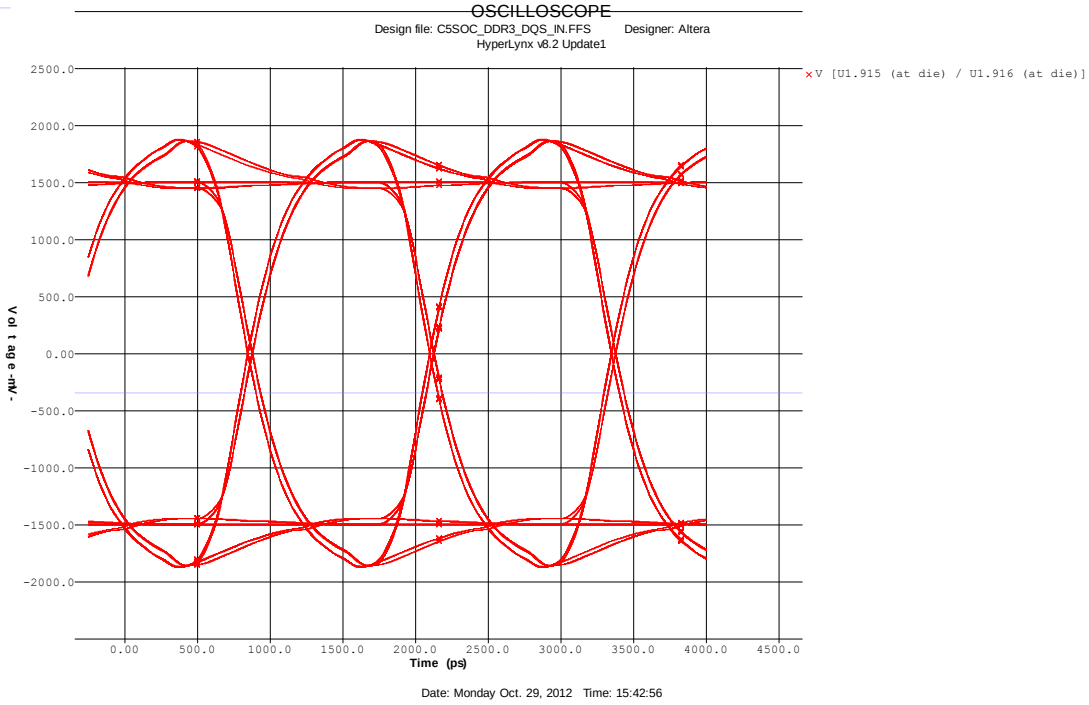


Topology Schematic signal in from memory

Design File: c5soc_ddr3_dqs_in.ffs
HyperLynx LineSim v8.2 Update1

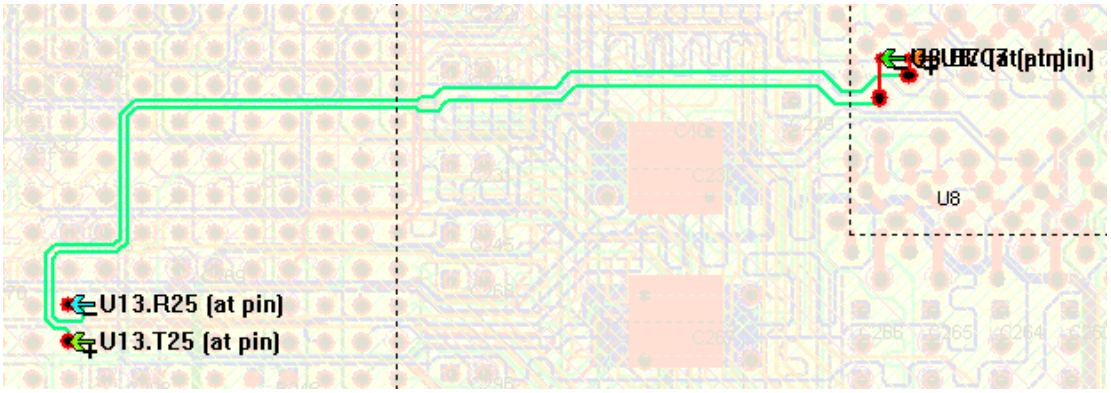


Simulation

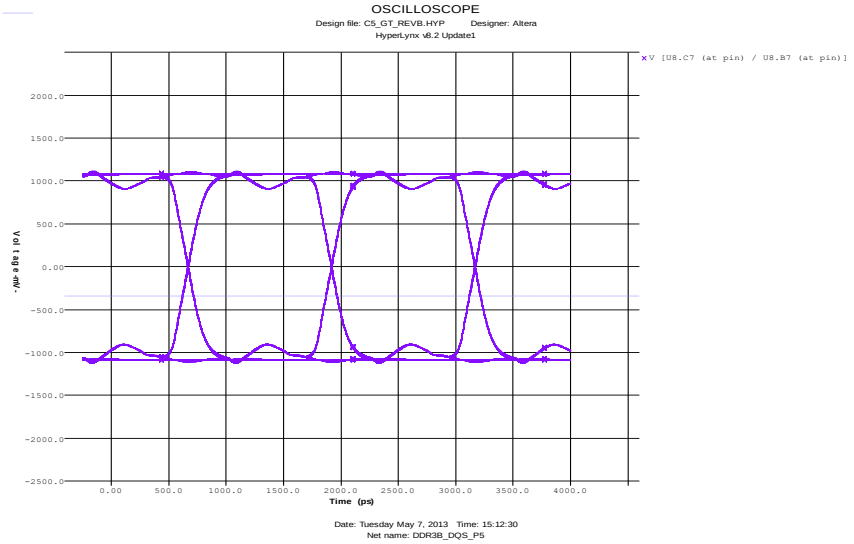


Nice, it should work well.

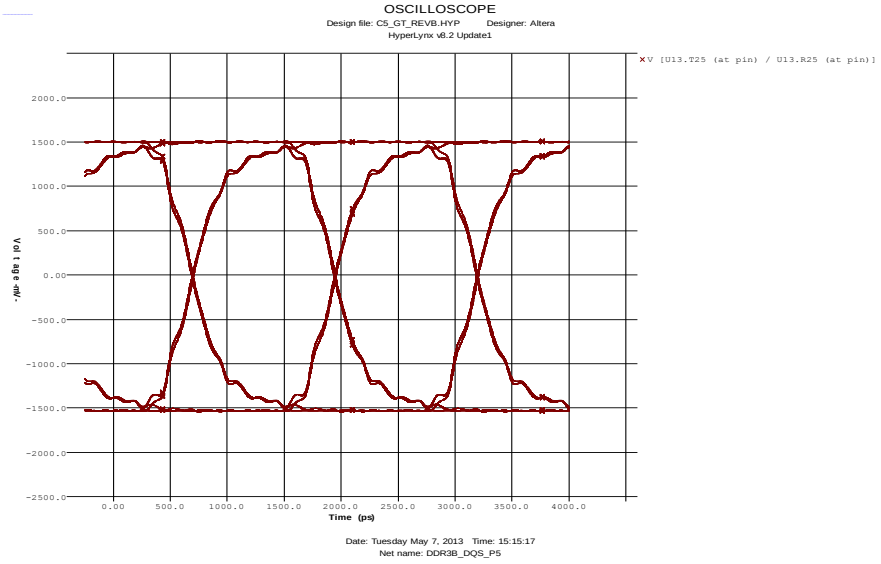
Verification by analysis of the topology using HyperLynx on the Revision B board is presented below. The topology for DDR3B_DQS5 looks like this:



Here is the simulation from the FPGA to the memory device



In turn here is the simulation for the data coming back from the memory device



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