IBIS Model Process For High-Speed LVDS Interface Products

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Overview

With high-speed system designs becoming faster and more complicated, the need to simulate designs before routing and layout is essential. In order to perform timely and accurate simulations, models representing all of the system components are required. The Input/Output Buffer Information Specification (IBIS) has emerged as the device model standard for most system designers and semiconductor vendors. Since IBIS is a behavioral model, it has the advantages over SPICE of not revealing proprietary information and shorter simulation run times. National Semiconductor recognizes the importance of providing quality IBIS models to its customers, and fully supports the IBIS standard. This paper discusses National Semiconductor's methodology for creating IBIS files for its high-speed Interface products.

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Review of IBIS Standard

IBIS is an approved standard within the Electronic Industry Alliance (EIA), and is also known as ANSI/EIA-656. IBIS is considered a behavioral model specification. An IBIS behavioral model contains I-V and V-T data of input and output buffers of a device in ASCII-text format. This data, along with keywords specified by the IBIS standard, can be used to describe the analog behavior of the device under operation. However, IBIS really isn't a "model", rather it is data that will be used by a simulator to create a behavior model of the device based upon certain algorithms. An IBIS behavioral model is sometimes referred to as an "IBIS file" or "IBIS datasheet". IBIS files are most commonly used for signal integrity simulations of high-speed boards or systems.

For more information on the history of the IBIS specification and the basic structure of model types in IBIS, refer to National Semiconductor application note AN-1111, An Introduction to IBIS (I/O Buffer Information Specification) Modeling. The IBIS Open Forum is an EIA group that is responsible for the official IBIS specification. The IBIS Open Forum website (http://www.eigroup.org/IBIS/Default.htm) contains useful information about IBIS modeling, including the current specification, training material, and various presentations by model users and developers.

Differential Technology and the IBIS Specification

Over the years, as the technology has progressed to such standards as LVDS, the IBIS specification has evolved to support these new standards. The IBIS specification supports differential I/O by providing differential pin mapping. This allows simulators using IBIS files to know which pins are a differential pair, described as inverting and non-inverting pins. However, the format of the IBIS data is for a single-ended device. To create a differential IBIS file, the IBIS data is extracted as if it was a single-ended device. This has led to discussion in the IBIS community as to what the best method is to create differential IBIS files. As a result, there are several methods that have been proposed and are used by different vendors and modeling companies. National Semiconductor recognizes that there are different methods available for creating differential IBIS files, and uses the methods described in this paper to provide the highest quality models possible. As more work is done in the area of differential modeling, National Semiconductor will continue to evaluate it's methodology process and use the best methods available to create the most accurate models.

Common Model Types in the IBIS Specification

There are different model type declarations available in the IBIS specification. Some of the model types are input, input/output, output, 3-state output, and open drain. The two most common model types used by National Semiconductor are Input and 3-State Output. These model types will be discussed in detail below.

Input Model

The Input Model can be viewed as a receiver input, control input, or driver input. When an input-to-output simulation is done using IBIS files, the output model exhibits the behavior of the device driving, and the input model exhibits the behavior of the device receiving.

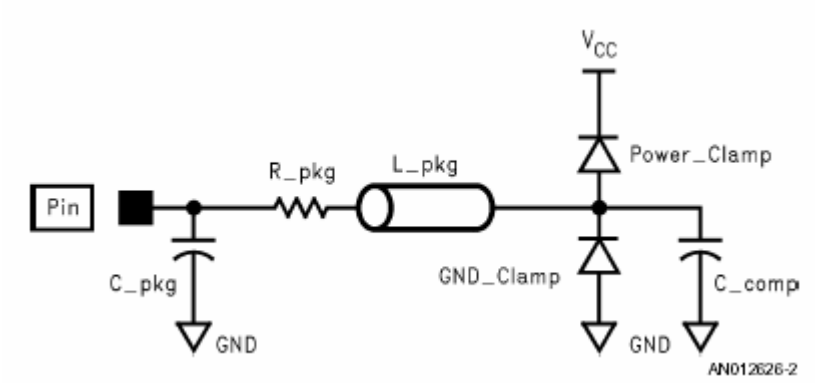

Figure 1. Input Model Structure

The Input Model is made up of the following elements:

- Package elements resistance, inductance, and capacitance (C_pkg, R_pkg, L_pkg)
- A clamp (Power_Clamp) that is active when the input voltage is above Vcc
- A clamp (GND_Clamp) that is active when the input voltage is below Ground
- Die capacitance of the input (C_comp)

The power and ground clamp curves define the ESD structure of the Input Model. When the input is between Ground and Vcc, the circuit is in normal operation. For voltages much higher than the supply Vcc or much lower than Ground, one of the diodes should turn on in order to prevent excess voltage at the circuit input. For typical input structures, the power clamp diode is forward biased when the input is approximately 0.7 V above Vcc, and the ground clamp diode is forward biased when the input is approximately 0.7 V less then Ground.

The IBIS specification uses keywords to define the circuit elements in an Input Model structure. The following keywords can be found in the current IBIS Specification version 3.2:

- (**Model**): Name of input model.
- (**Model_type**): Type of model (ie. Input, output, etc.).
- (**Vinh**): Minimum upper threshold voltage. This is Vih from the datasheet for a receiver input. For a differential input, the Vdiff parameter defined under the Differential Pin Mapping section will override Vinh.
- (**Vinl**): Maximum lower threshold voltage. This is Vil from the datasheet for a receiver input. For a differential input, the Vdiff parameter defined under the Differential Pin Mapping section will override Vinh.
- (**C_comp**): Input die capacitance. This includes parasitic capacitance from the transistor and circuit elements, capacitance due to metallization, and pad capacitance. This does not include package capacitance.
- (**Temperature Range**): Specified operating temperature range of device.
- (**Voltage Range**): Specified supply voltage (Vcc) of device.
- (**GND Clamp Reference**): Reference voltage for the ground clamp circuit. In most cases, the reference is ground. However, in some cases it may be different than ground. If GND Clamp Reference is not defined, it is ground by default.
- (**GND Clamp**): Current-Voltage characteristics of ground clamp circuit. The data is referenced to ground clamp reference voltage. The data is entered in the IBIS file as Vtable = Vin – [Ground Clamp Reference Voltage]. The data is taken from –Vcc to Vcc. The diode is forward biased from –Vcc to 0, and from 0 to Vcc the diode is in normal operating region.
- (**Power Clamp Reference**): Reference voltage for the power clamp circuit. In most cases, the reference is the specified supply voltage. However, in some cases it may be different than Vcc or the specified supply voltage range. If Power Clamp Reference is not defined, it is the specified supply voltage by default.
- (**Power Clamp**): Current-Voltage characteristics of the power clamp circuit. The data is referenced to the power clamp reference voltage. The data is entered in the IBIS file as Vtable = [Power Clamp Reference Voltage] – Vin. The power clamp data is taken from Vcc to 2 * Vcc. The diode is forward biased from Vcc to 2 * Vcc. The power clamp data does not include data from 0 to Vcc in the normal operating region because the ground clamp data already has this data. If this data were to be included in the power clamp curve, then a simulator would double-count the data in the normal operating region.

The following is an example of an IBIS LVDS input model.

```
[Model]                  LVDS_INPUT
Model_type Input
Vinh=1.30              | Vth
Vinl=1.10              | Vtl
|
|                        TYP        MIN         MAX
|
C_comp                   3p         2.8p         3.2p
|
[Temperature Range]   25         85          -40
|
[Voltage Range]          2.5        2.375        2.625
|
[GND Clamp]
|
|Vtable              I(typ)          I(min)          I(max)
|
-2.50E+00       -5.70E-01       -5.32E-01       -6.12E-01
…
…
2.45E+00        7.30E-07        7.43E-07        7.18E-07
|
[POWER Clamp]
|
|Vtable              I(typ)          I(min)          I(max)
|
0.00E+00        4.11E-10        5.49E-10        1.85E-10
…
…
-2.48E+00       3.19E-09        2.34E-09        2.40E-09
|
| End                    LVDS_INPUT
```

Figure 2. **Example IBIS Input Model Structure Syntax**

3-State Output Model

The 3-State Output Model can be viewed as a driver. A 3-State device has an enable pin to disable the output.

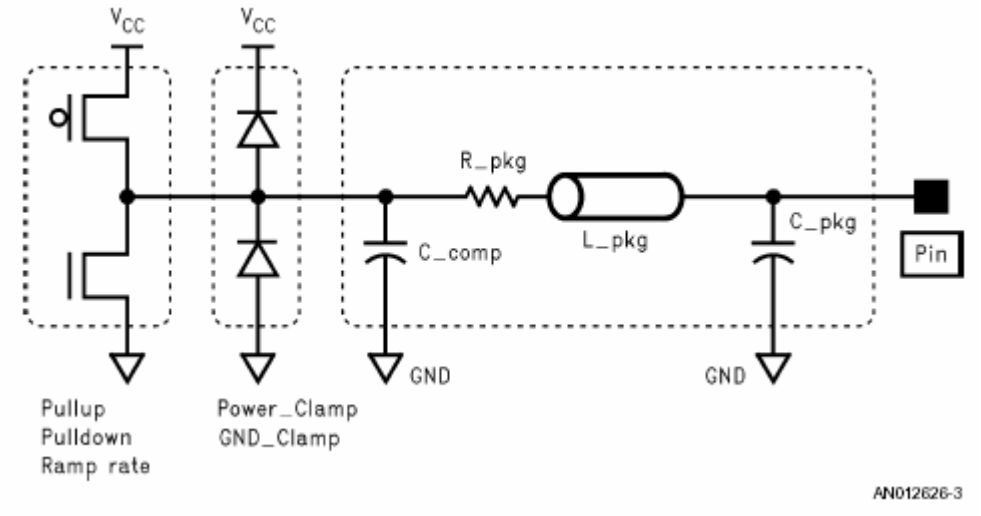

Figure 3. **Output Model Structure**

The Output Model is made up of the following elements:

- Package elements resistance, inductance, and capacitance (C_pkg, R_pkg, L_pkg)
- A clamp (Power_Clamp) that is active when the output voltage is above Vcc
- A clamp (GND_Clamp) that is active when the output voltage is below Ground
- Die capacitance of the output (C_comp)
- A circuit (Pullup) that is active when the output is high
- A circuit (Pulldown) that is active when the output is low
- A Ramp rate that describes the output slew rate
- Rising and Falling waveform data that describes the transient output

In a 3-State Output device, the output can be put into a high-impedance state as well as a low and high state. The I-V data in the high-impedance state is the power and ground clamp data. The power and ground clamp curves define the ESD structure of the Output Model and behave in the same manner as the clamps on the input. The pullup data is the drive strength of the device at a logic-high state. The pulldown data is the total drive strength of the device at a logic-low state. The power and ground clamp data is subtracted from the pullup and pulldown data, so the IBIS file contains I-V characteristics of only the device in a high or low state, with the high-impedance I-V characteristics described by the power and ground clamp curves. When a simulator uses an IBIS 3-State output model, it will combine the pulldown and pullup curves with the power and ground clamp curves. So separating the data is necessary so the simulator does not double count the curves.

The IBIS specification uses keywords to define the circuit elements in an Output Model structure. The following keywords can be found in the current IBIS Specification version 3.2:

- (**Model**): Name of output model.
- (**Model_type**): Type of model (i.e. Input, output, etc.).
- (**Enable**): Active-High or Active-Low.
- (**Polarity**): Inverting or Non-Inverting. With a pair of differential outputs, one is inverting and the other is non-inverting.
- (**Vref**): Reference voltage level that the semiconductor vendor uses for the model.
- (**Vref/Rref/Cref**): Test load applied to the output that the semiconductor vendor uses to define timing such as propagation delay and/or output switching time of the model.
- (**C_comp**): Output die capacitance. This includes parasitic capacitance from the transistor and circuit elements, capacitance due to metallization, and pad capacitance. This does not include package capacitance.
- (**Temperature Range**): Specified operating temperature range of device.
- (**Voltage Range**): Specified supply voltage (Vcc) of device.
- (**GND Clamp Reference**): Reference voltage for the ground clamp circuit. In most cases, the reference is ground. However, in some cases it may be different than ground. If GND Clamp Reference is not defined, it is ground by default.
- (**GND Clamp**): Current-Voltage characteristics of ground clamp circuit. The data is referenced to ground clamp reference voltage. The data is entered in the IBIS file as Vtable = Vin – [Ground Clamp Reference Voltage]. The data is taken from –Vcc to Vcc. The diode is forward biased from –Vcc to 0, and from 0 to Vcc the diode is in normal operating region.
- (**Power Clamp Reference**): Reference voltage for the power clamp circuit. In most cases, the reference is the specified supply voltage. However, in some cases it may be different than Vcc or the specified supply voltage range. If Power Clamp Reference is not defined, it is the specified supply voltage by default.
- (**Power Clamp**): Current-Voltage characteristics of the power clamp circuit. The data is referenced to the power clamp reference voltage. The data is entered in the IBIS file as Vtable = [Power Clamp Reference Voltage] – Vin. The power clamp data is taken from

Vcc to 2 * Vcc. The diode is forward biased from Vcc to 2 * Vcc. The power clamp data does not include data from 0 to Vcc in the normal operating region because the ground clamp data already has the data and if included then a simulator would double-count the data in the normal operating region.

- (**Pulldown Reference**): Reference voltage for the pulldown circuit. In most cases, the reference is specified as ground. However, in some cases it may be different than ground. If Pulldown Reference is not defined, it is ground by default.
- (**Pulldown**): Current-Voltage characteristics of the pulldown circuit. The data is referenced to the pulldown reference voltage. The data is entered in the IBIS file as Vtable = Vin – [Pulldown Reference Voltage]. The data is taken from –Vcc to 2 * Vcc.
- (**Pullup Reference**): Reference voltage for the pullup circuit. In most cases, the reference is specified as Vcc. However, in some cases it may be different than Vcc or the specified supply voltage range. If Pullup Reference is not defined, it is the specified supply voltage by default.
- (**Pullup**): Current-Voltage characteristics of the pullup circuit. The data is referenced to the pullup reference voltage. The data is entered in the IBIS file as Vtable = [Pullup Reference Voltage] – Vin. The data is taken from –Vcc to 2 * Vcc.
- (**Ramp**): Describes the output rise and fall slew rate as dV/dt_r and dV/dt_f. The slew rate is measured at the 20% and 80% points. R_load is the resistive load used to generate the dV/dt data. If R_load is not specified, the default value is 50 Ohms.
- (**Falling Waveform**): The time it takes the device to go from a high to a low driving a resistive load (R_fixture) connected to a pullup reference (V_fixture).
- (**Rising Waveform**): The time it takes the device to go from a low to a high driving a resistive load (R_fixture) connected to a pullup reference (V_fixture).

The following is an example of an IBIS LVDS output model.

```
[Model]                  LVDS_3STATE_OUTPUT
Model_type 3-state
Enable Active-High
Polarity Non-Inverting
Vref=1.2
Vmeas=1.2
Rref=50                  | 100 Ohms Across Outputs OUTP and OUTM
Cref=5p
|
|                        TYP          MIN          MAX
|
C_comp                   4p           3.5p         4.5p
|
[Temperature Range]      25           85           -40
|
[Voltage Range]          2.5          2.375        2.625
|
[Pullup]
|
|Vtable        I(typ)         I(min)         I(max)
|
     5       -45.69e-3      -38.31e-3      -59.04e-3
    …
    …
  -2.5        206.9e-6       533.5e-6       103.6e-6
|
[Pulldown]
|
|Vtable          I(typ)          I(min)          I(max)
|
```

```
   -2.5          -45.73e-3       -38.15e-3       -59.34e-3
     …
     …
   5.0          23.23e-3        19.51e-3        29.47e-3
|
[GND Clamp]
|
|Vtable              I(typ)             I(min)             I(max)
|
-2.50E+00       -1.54E+00       -1.34E+00       -1.79E+00
     …
     …
2.45E+00        8.15E-10        1.05E-09        5.01E-10
|
[POWER Clamp]
|
|Vtable        I(typ)         I(min)         I(max)
|
0.00E+00        8.83E-10        1.12E-09        5.50E-10
     …
     …
-2.48E+00       4.33E-09        3.87E-09        3.33E-09
|
[Ramp]
|
|                TYP                        MIN                        MAX
|
dV/dt_r    241mV/.06997ns       229mV/.09485ns       245mV/.04859ns
dV/dt_f    241mv/.05878ns       229mV/.08440ns       245mV/.03894ns
|
R_load=50
|
[Falling Waveform]
R_fixture=50
V_fixture=1.2
V_fixture_min=1.2
V_fixture_max=1.2
|
|Time             V(typ)         V(min)         V(max)
|
      0         1.401          1.385          1.405
     …
     …
9.90E-10          1.01          1.007          1.01
|
[Rising Waveform]
R_fixture=50
V_fixture=1.2
V_fixture_min=1.2
V_fixture_max=1.2
|
|Time             V(typ)         V(min)         V(max)
|
0                 1.01          1.008          1.01
     …
     …
9.90E-10          1.401          1.385          1.405
|
| End                    LVDS_3STATE_OUTPUT
```

Figure 4. Example IBIS Output Model Structure Syntax

Output Reference Load in IBIS

As stated previously, for an IBIS 3-State Output model, a timing reference load is defined with the following parameters: Rref, Cref, Vref, and Vmeas.

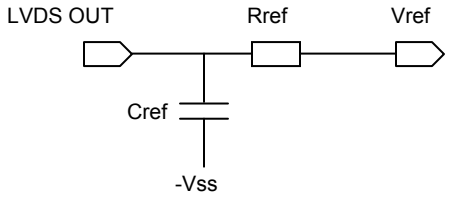

Figure 5. **IBIS Timing Load Schematic**

This timing load is used to perform a "time to measurement voltage" simulation. This is the time from when the output starts switching to when it crosses a specific voltage level, which is usually Vmeas. This time is referred to as the "buffer delay." The Rref, Cref, and Vref parameters correspond to the same test load that the semiconductor manufacturer uses when specifying the propagation delay or output switching time of the device. For LVDS technology, 100 Ohms usually terminate the non-inverting output and inverting output. To adhere to the IBIS specification, Rload/2 defines Rref, and Vref is the VOS of the device. In this manner, either of the differential output buffers can be operated as a single-ended buffer. Vmeas is the voltage at which the propagation delay is measured. For LVDS, this is typically equal to the VOS of the device. All of these parameters can typically be obtained from the device's datasheet.

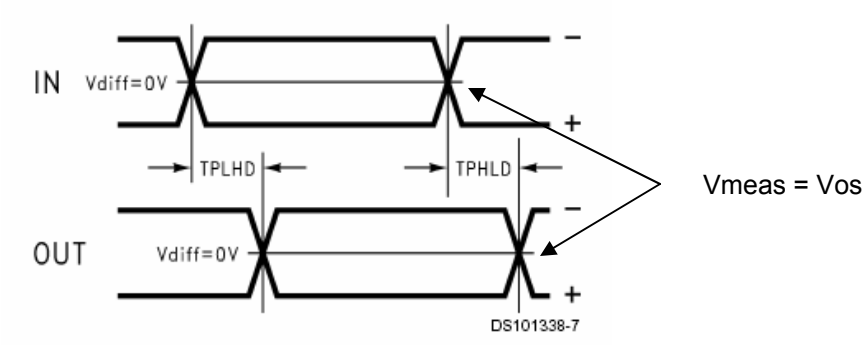

Figure 6. **Datasheet Propagation Delay Measurement of LVDS Repeater**

This timing load is used for board-level timing simulation. (The IBIS standard does not include any timing information internal to the device.) This time is required by most simulators to calculate correct flight times and is also used to determine the receiver setup and hold time windows for analysis.

IBIS Model Data Extraction

An IBIS file can be created from lab data or from SPICE simulation data. The disadvantages of IBIS files created from lab data is that it is difficult to create process corner models and de-embed the effects of the package. National Semiconductor uses the most accurate SPICE netlists available to generate IBIS data for all new Interface Products.

A SPICE netlist used to generate IBIS data has no package model attached to it. The IBIS specification requires that there be no package effects in the generated IBIS data. Three different process corners are obtained: typical, minimum, and maximum. The typical process data is generated at nominal supply voltage VCC, nominal temperature (room temperature), and nominal process. The minimum process data is generated at minimum supply voltage Vcc, weak process, and a hot temperature. The maximum process data is generated at maximum supply voltage Vcc, strong process, and a cold temperature. These process data sets will yield the typical case, worst case, and best-case scenarios of the device. Note that MIN and MAX are related to the conditions noted above and are not specifying the edge rate MIN and MAX. For a CMOS device, typically the MIN model (minimum supply, weak process, hot temperature) would generate the slower transition time of the signal – thus the MIN model generates the “max” transition time.

The IBIS specification requires that the DC I-V data be generated over a voltage range of –Vcc to 2 * Vcc. This range is chosen so that the generated data will be over a range of voltages the input or output could possibly see in a transmission line environment. The maximum negative reflection from a shorted transmission line would be at –Vcc while the maximum positive reflection from an open transmission line would be at 2 * Vcc.

The required voltage range of –Vcc to 2 * Vcc often puts the device under test outside of it’s recommended operating region. This applies to the ground and power clamp curves. The ground clamp curve data is generated from –Vcc to Vcc. However, most devices do not work far below ground. If you were to apply –Vcc to the input, the device would malfunction. There are differences of opinion in the IBIS community as to how important it is to have accurate data beyond the rail curves. National Semiconductor extrapolates the ground clamp curve beyond the rail to make a “best-fit” realistic curve. Issues can arise when the current is really large (in the K Amps) only after a half of a volt or one volt beyond where the diode conducts.

Generation of Ground Clamp Curve

In order to create a ground clamp curve, a DC voltage source is applied to one of the input pins, the source voltage is swept from –Vcc to Vcc, and the current is measured at the input.

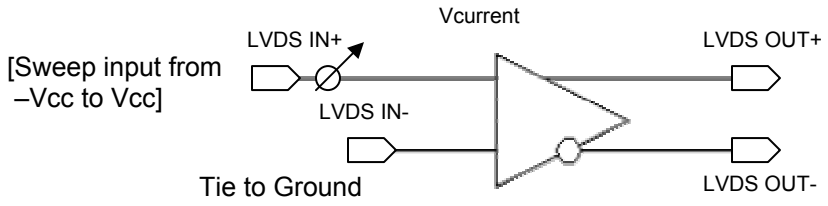

Figure 7. **SPICE Setup to Generate Ground Clamp Curve**

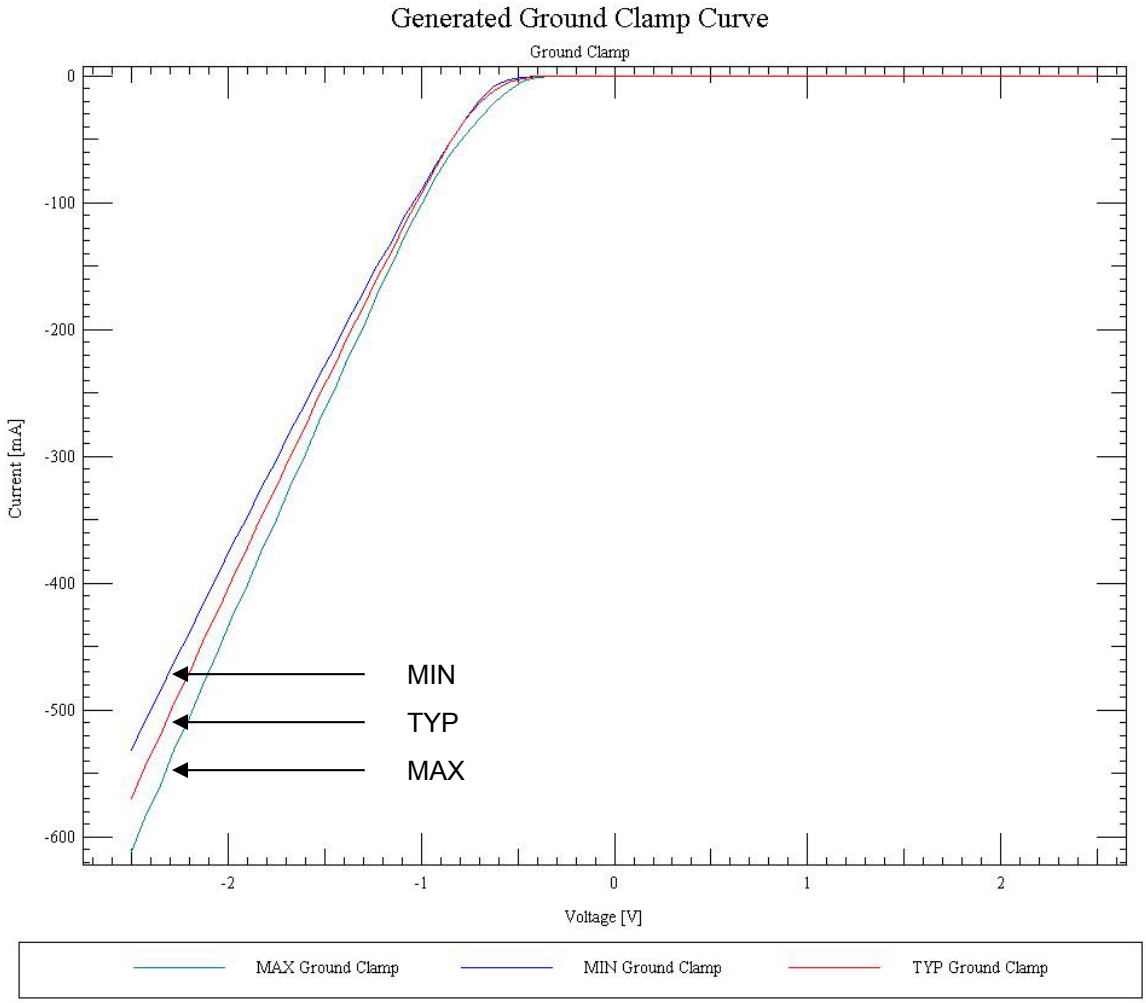

Figure 8. SPICE Generated Ground Clamp Curve for LVDS Device for a 2.5V device

It makes no difference which input pin is used to obtain the ground clamp curve since the inputs are symmetric, and the same result will be obtained on either pin. The other pins do not affect the simulation data, but usually the other input pin is tied to ground while the outputs are left floating. The same procedure can be used for enable and output pins, if they are tri-state outputs. For the tri-state outputs, the enable pin has to be set in order for the output to be put into a high-impedance state.

One issue with using SPICE netlists to create the ground clamp curve (as well as the power clamp curve) is that the diodes in the ESD structure can be too ideal. This sometimes results in the diode having no intrinsic resistance. If this is the case, then a small (usually 1 to 3 Ohms) resistor is added in series with the ESD structure for compensation.

Generation of Power Clamp Curve

The same procedure to create the ground clamp curve is used to generate the power clamp curve. The only difference is that the applied voltage source is swept from Vcc to 2 * Vcc.

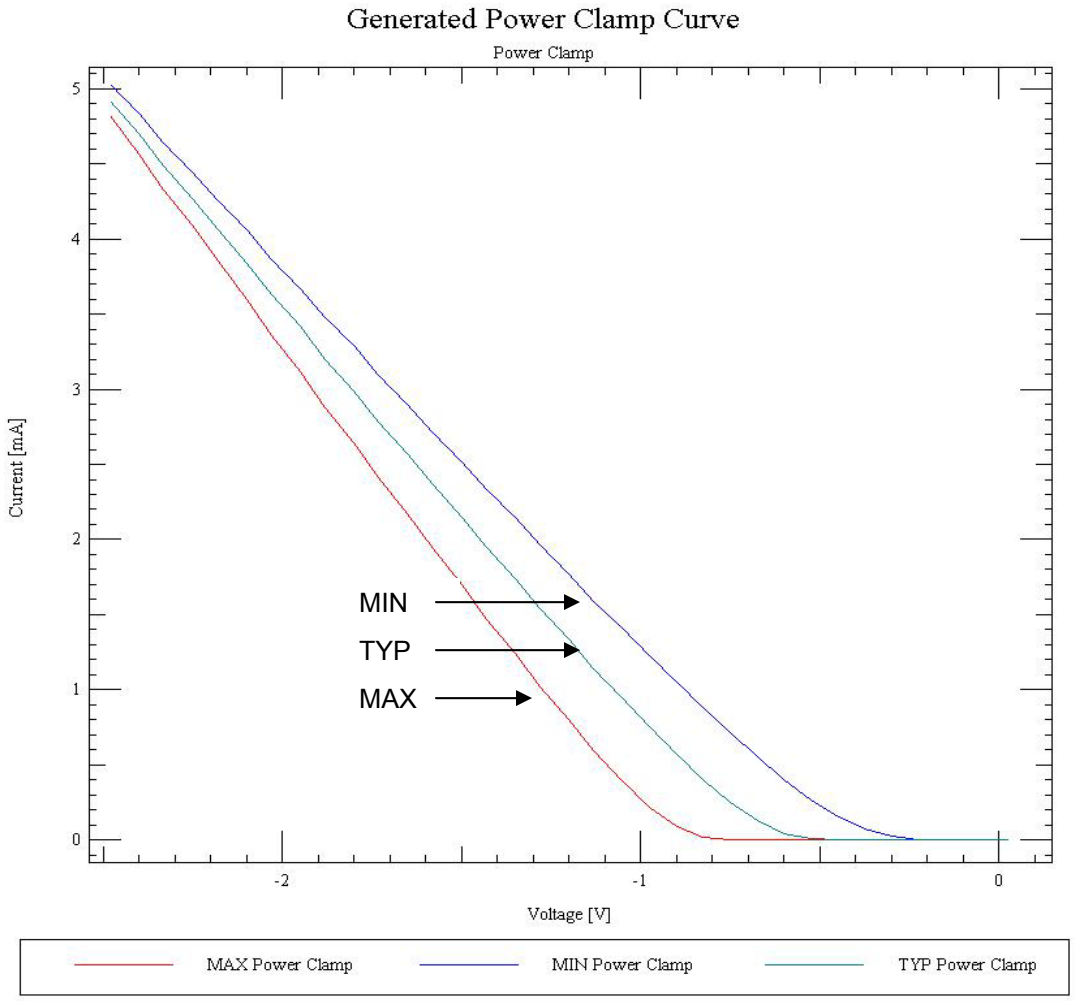

Figure 9. **SPICE Generated Power Clamp Curve for LVDS Device**

The power clamp curve (along with the pullup curve) is Vcc relative. When doing the minimum and maximum process corner sweeps, the Vcc has to be made relative to the supply voltage for that process corner and the sweep voltage has to track the variation in Vcc. For example, assume a device has typical supply voltage of 3.3 V, a minimum supply voltage of 3.0 V, and maximum supply voltage of 3.6 V. For the typical case, the voltage sweep is 3.3 V to 6.6 V. For the minimum case, the sweep voltage is 3.0 V to 6.3 V. The difference between the typical and minimum supply voltage is -0.3 V, so the sweep voltage for the minimum process corner has to be adjusted by –0.3 V. The same can be done for the maximum supply voltage, except the difference is +0.3 V. The sweep voltage range for each process corner is 3.3 V, which keeps each data point the same ‘distance’ from Vcc.

Generation of Pulldown Curve

In order to create a pulldown curve, the input is set to a logic low, the enable pin is set to make the output active, a voltage source is applied to one of the output pins, and the voltage source is swept from –Vcc to 2 * Vcc while the current is measured.

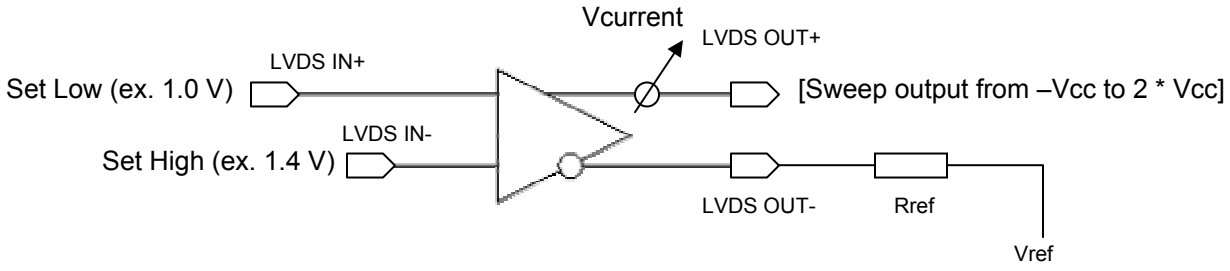

Figure 10. **SPICE Setup to Generate Pulldown Curve**

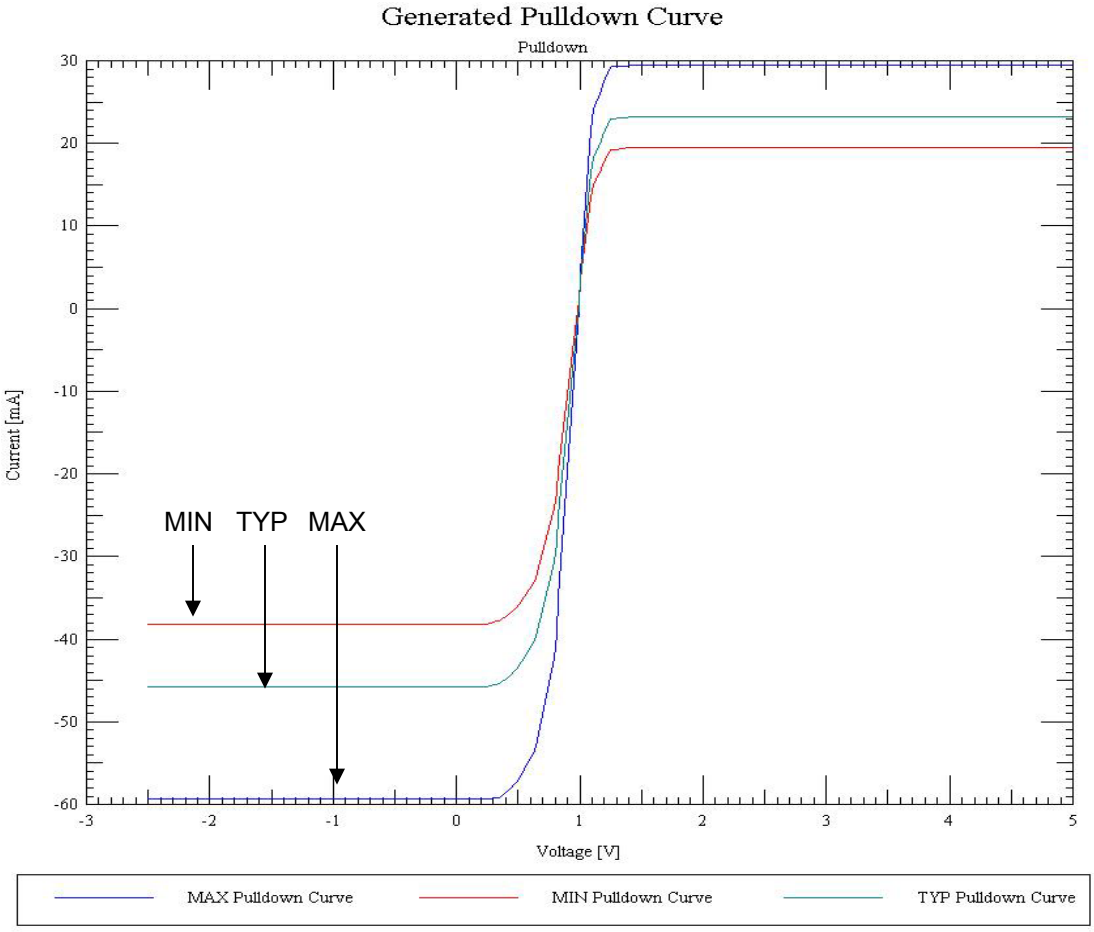

Figure 11. **SPICE Generated Pulldown Curve for LVDS Device**

If the device has differential inputs, then the differential input signal VID, where VID = (Vin+) – (Vin-), is used to define the input logic state. Since the output pins are symmetric, it does not make any difference which output pin is used to generate the IBIS data. However, the output pin not being swept with a DC voltage needs to be tied to a reference voltage Vref through a resistor Rref. The outputs of the LVDS device are dependent on one another, and this dependency must be accounted for when generating IBIS data. By holding one of the output pins in a steady state, the output pin being swept by a DC voltage sees the other pin behaving correctly. A SPICE simulation is done beforehand using the specified differential resistor from the datasheet and the simulated VOS is used as the Vref. The resistor used, Rref, is simply half of the specified differential resistor in the datasheet.

Unlike TTL devices, the pulldown and pullup curves generally do not cross at the origin. The output structure of the device will influence where the curves cross the zero-current point. For the example LVDS device in this paper, the pulldown will typically cross at 1.0 V and the pullup will typically cross at 1.4 V. (When relative to Ground.)

Generation of Pullup Curve

The same procedure to create the pulldown curve is used to generate the pullup curve. The only difference is that the input is set to logic high. The pullup curve is Vcc relative, like the power clamp curve.

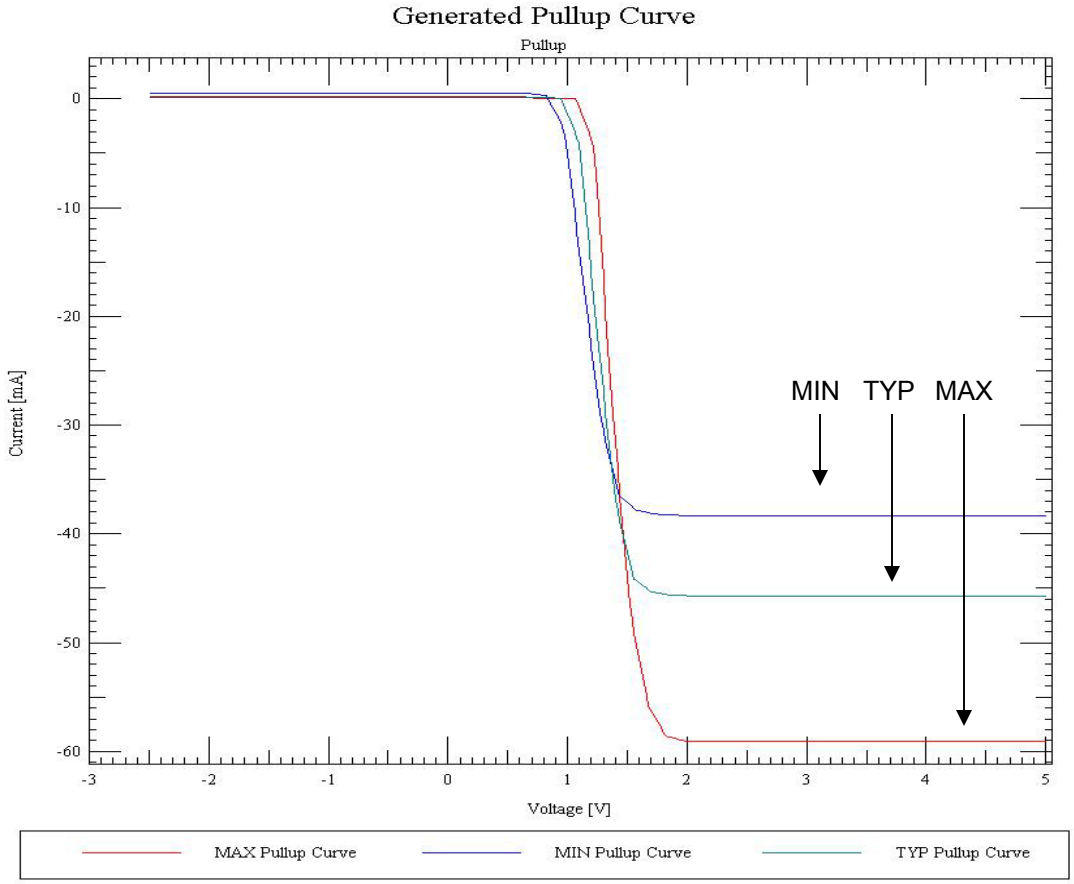

Figure 12. SPICE Generated Pull-up Curve for LVDS Device

Generation of Rising Waveform Curve

In order to create a rising waveform curve, a rising ramp is applied to the input, and the time it takes the output to reach a steady state is measured.

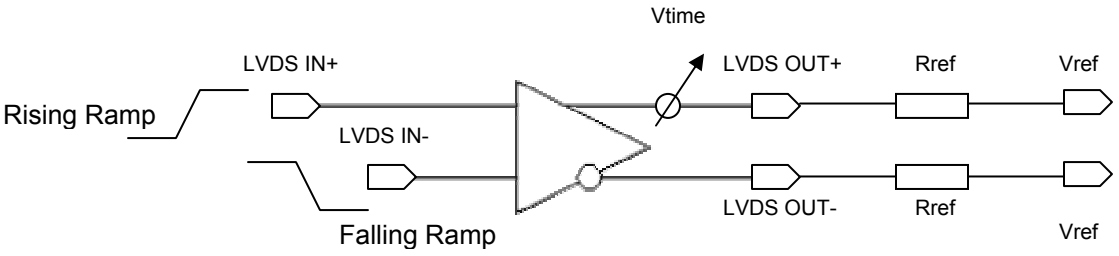

Figure 13. SPICE Setup to Generate Rising Waveform

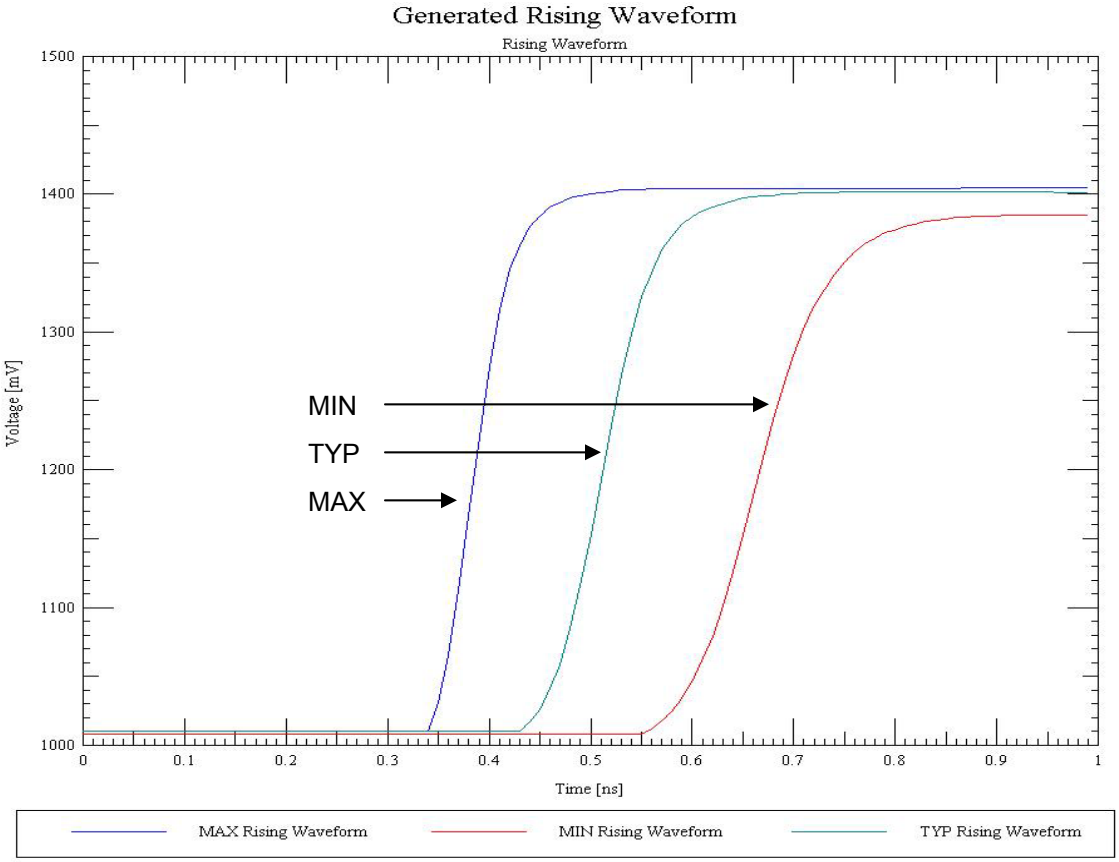

Figure 14. SPICE Generated Rising Waveform for LVDS Device

Since the device is symmetric, it does not matter which input and output pin is used to generate the IBIS data. (The same polarity pin should be used on the input as the output. For example, if the voltage ramp is applied to the non-inverting pin, then the transient time should be measured on the non-inverting output pin.) If the device has differential inputs, then an opposite polarity

voltage ramp should be applied to the input pin not being used to generate the IBIS data. In this way, the differential inputs are behaving properly. The input voltage ramp should switch from Ground to Vcc for the process, and the slew rate of the input signal should match the slew rate of the device. For the differential outputs to work properly, the outputs are tied through a resistor Rref to a voltage source Vref. The resistor Rref is equal to one half the specified differential resistor and the reference voltage Vref is equal to the VOS of the device. All of the V-T data needs to be generated at the same starting reference point (usually zero), to ensure an accurate duty cycle and proper switching characteristics.

This rising waveform curve is also used to extract the rising slew rate of the device for the Ramp keyword in IBIS. The rising slew rate (dV/dt_r) should be measured at the 20% and 80% points. The Ramp data is intended only to be used if there is not any V-T data available and also to keep backward compatibility as some older IBIS versions do not support V-T data.

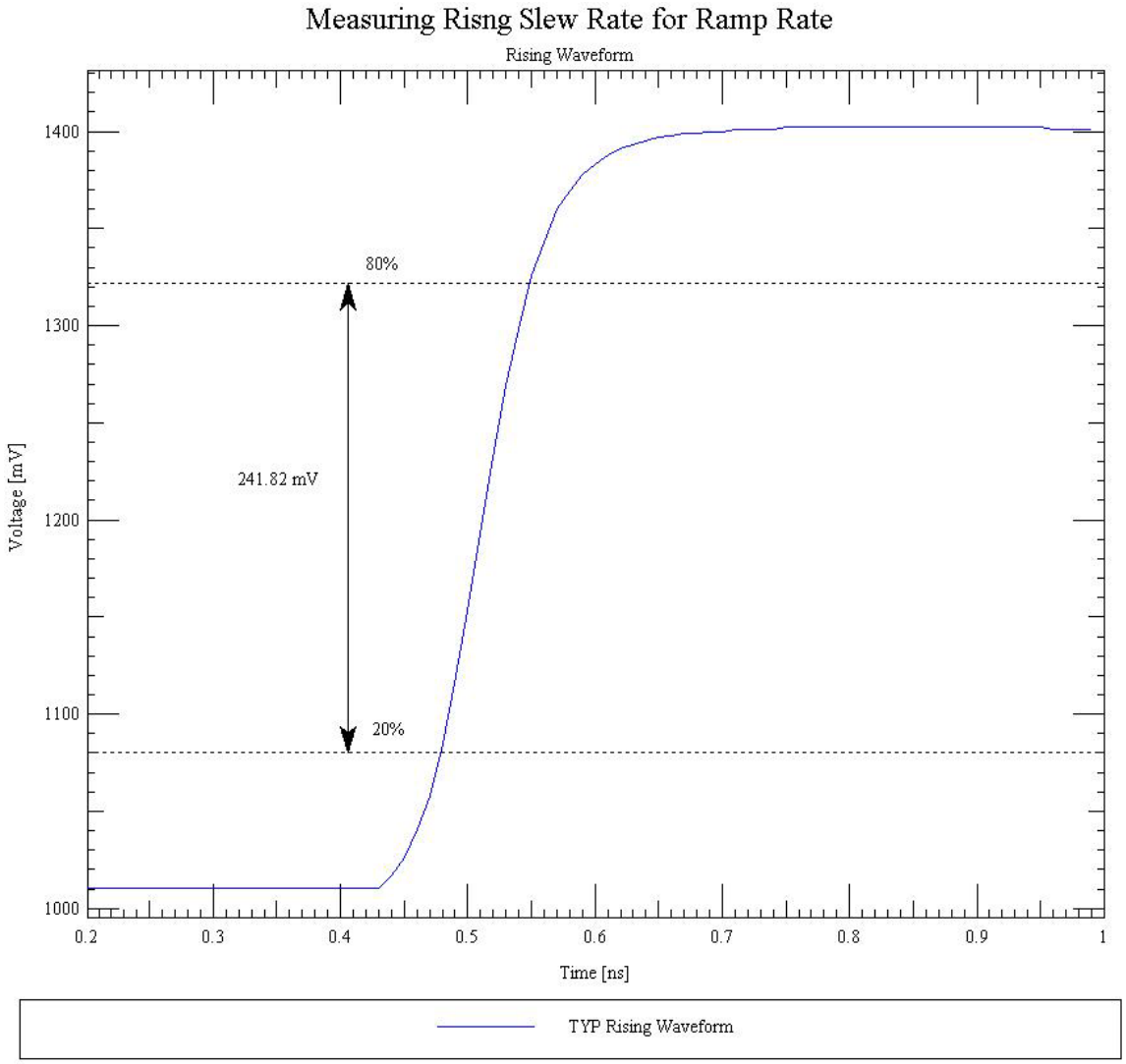

Figure 15. **Measuring Rising Slew Rate for LVDS Device**

The “time window” in which the transition switches state is kept as small as possible. Some IBIS simulators have issues if the time window in the IBIS file is longer than the period of the input signal used to simulate the IBIS file.

For TTL devices, a set of four V-T curves is necessary to describe the switching characteristics of the device. One set is rising/falling waveform to Vcc, and the other set is rising/falling waveform to Ground. However, with LVDS, the rising/falling waveforms to Ground are out of the operating region of the device and are not necessary.

Generation of Falling Waveform Curve

The same procedure to create the rising waveform curve is used to generate the falling waveform curve. The only difference is that a falling input voltage ramp is used.

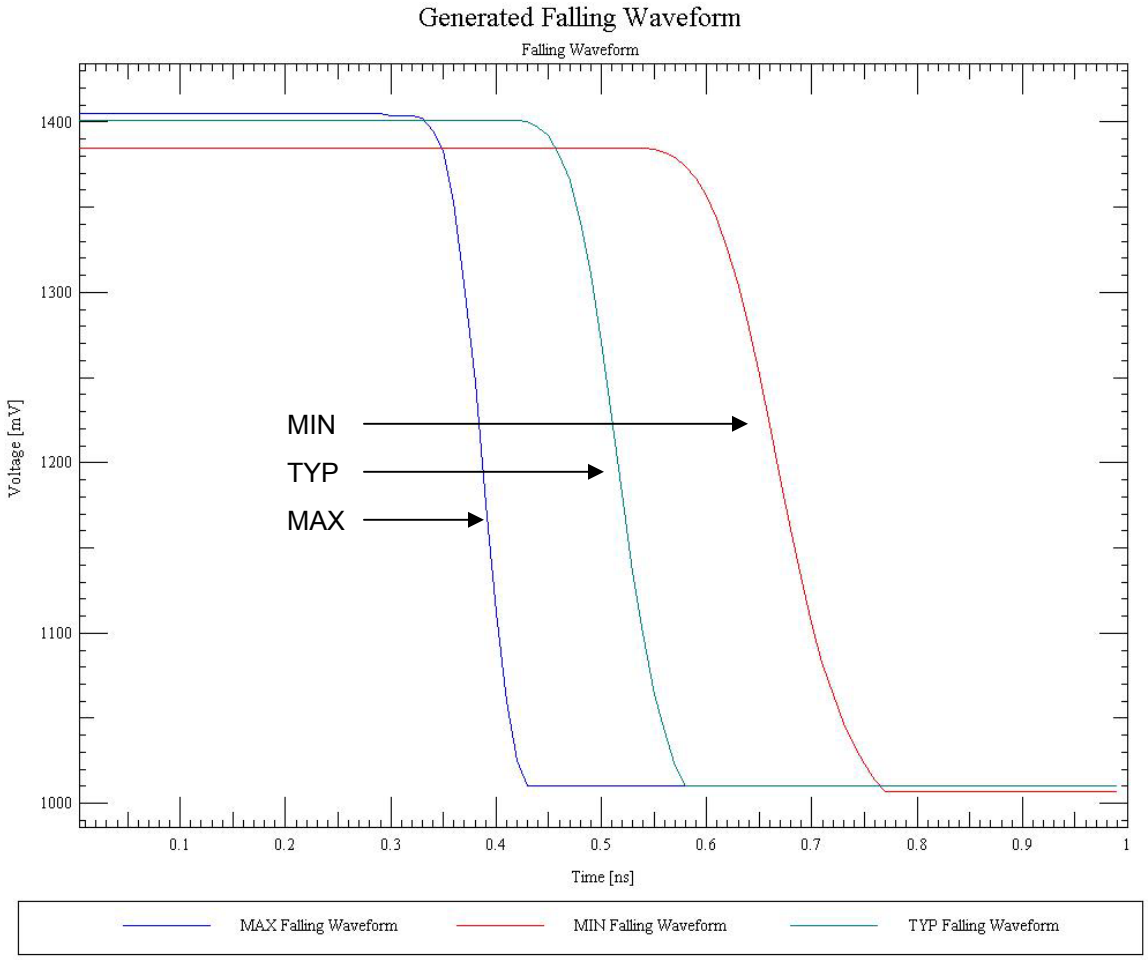

Figure 16. SPICE Generated Falling Waveform for LVDS Device

Generation of C_comp Parameter

In order to measure the die capacitance of any of the pins (input, output, or enable), the same procedure is used. The following procedure is the most commonly used to extract the C_comp parameter using a SPICE simulation.

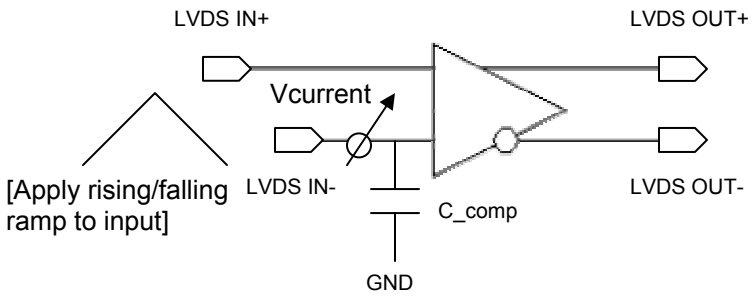

Figure 17. SPICE Setup to Measure C_comp on Input

A rising and falling voltage ramp is applied to the pin using the same slew rate, and the current is measured for both of the ramps. The C_comp value is determined by the equation I = C * dV/dt. The issue with this time-domain method is that the capacitance varies with the voltage.

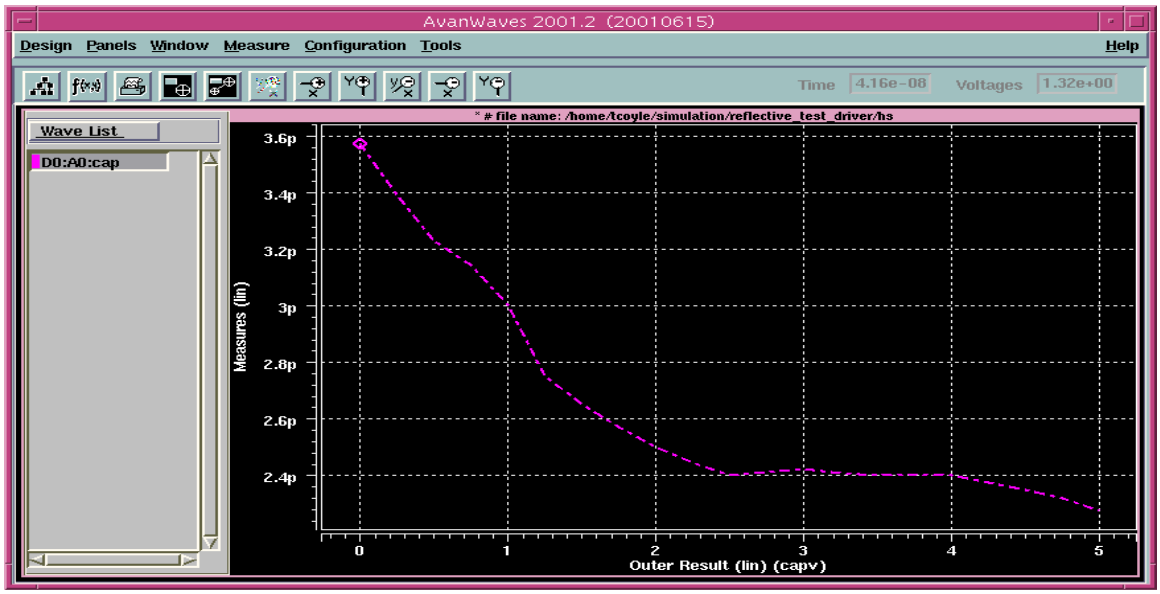

Figure 18. C_comp of LVDS Input vs. Input Voltage in HSPICE

For the capacitance vs. voltage curve obtained by the above method, the maximum and minimum values are averaged to get the average C_comp value. Simulating the IBIS file against the SPICE file under certain conditions with different C_comp values, and adjusting C_comp until it correlates to the SPICE file will find the final value of C_comp.

If the SPICE netlist used to generate the IBIS data contains pre-layout transistors, then the C_comp value will not contain the capacitance due to metallization or the pad capacitance, which

can be a significant source of the input capacitance. Due to the way that the C_comp parameter is defined in IBIS, at best it can only be an estimate of the input or output die capacitance. The capacitance is dependent on voltage, frequency, and other parameters that are not currently addressed by the IBIS Specification. Future versions of the specification will be addressing this issue.

The input or output capacitance can easily be measured in the lab using a TDR technique. This measurement includes the package capacitance, which needs to be subtracted out to determine the C_comp value. Some software packages such as TDA Systems IConnect automatically do this for you. In the graph below, the TDR waveform is shown along with a reference open waveform. An impedance profile is then created from these two waveforms, and the capacitance can be calculated and graphed.

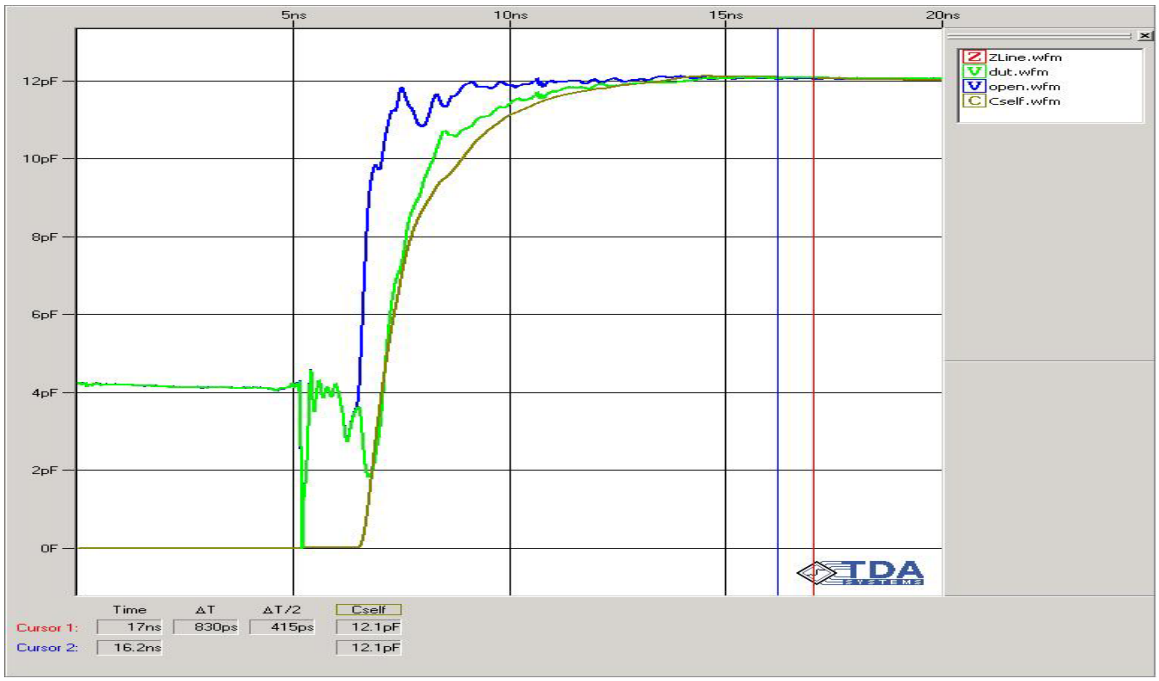

Figure 19. Output Capacitance of LVDS Buffer

Formatting an IBIS File

The generated IBIS data needs to be formatted as required by the IBIS specification. The specification limits the number of allowable data points to 100 in the current specification. (Version 3.2) National Semiconductor often generates more than 100 data points, and a "best fit" curve is used to make up the 100 data points. With a typical LVDS device, since the active region is between 1.0 V and 1.40 V, most of the data points are concentrated in this region to give the best accuracy.

In a 3-State output model, the power and ground clamp curves need to be subtracted from the pulldown and pullup curves. This can lead to numerical errors that give a "bump" in the curve or make the curve go to zero. This comes from subtracting two large numbers and not using enough significant digits.

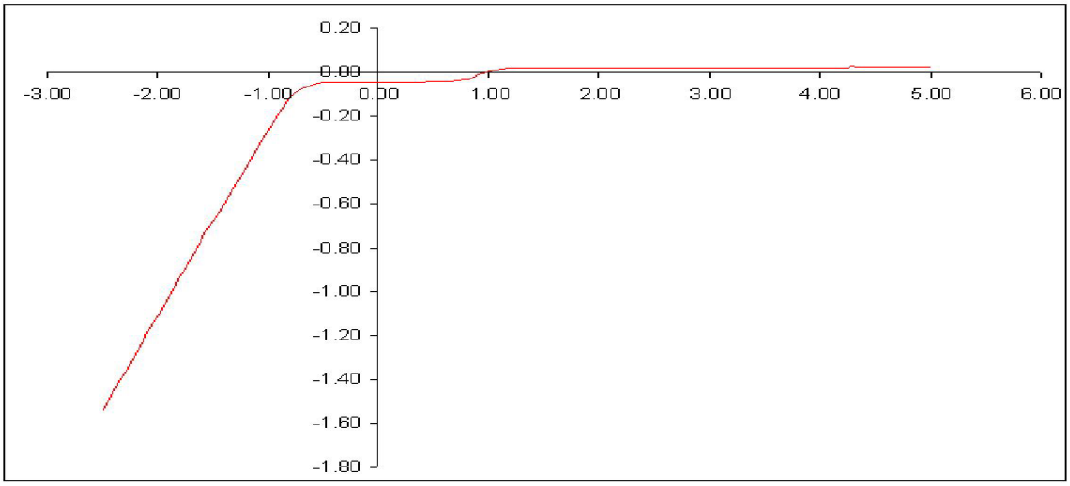

Figure 20. Generated Pulldown Curve with Power and Ground Clamp Data

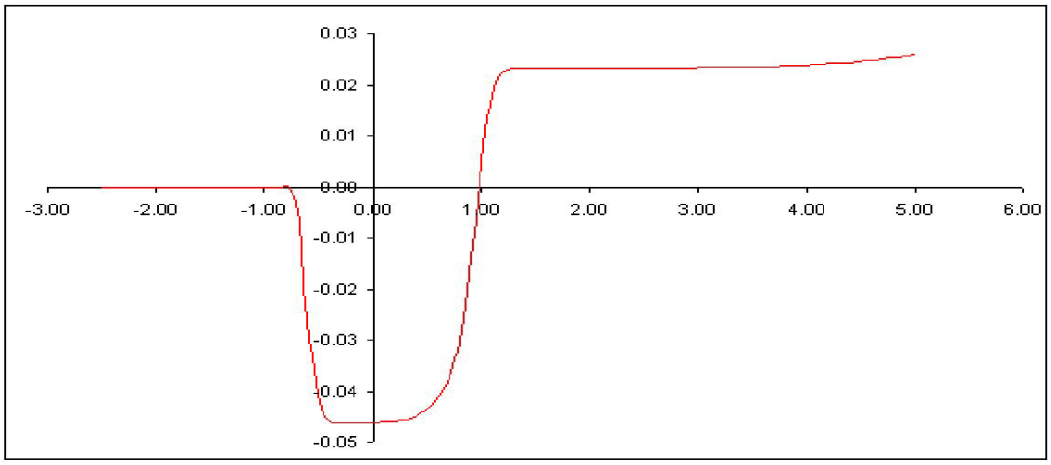

Figure 21. Pulldown Curve with Power and Ground Clamp Data Subtracted

As long as the numerical error occurs outside of the operating region of the device, then it can be filtered and smoothed out. An extraction method is used to ensure that the pulldown (or pullup)

data is not compromised by the power and ground clamp data. The following graph shows a properly extracted pulldown curve.

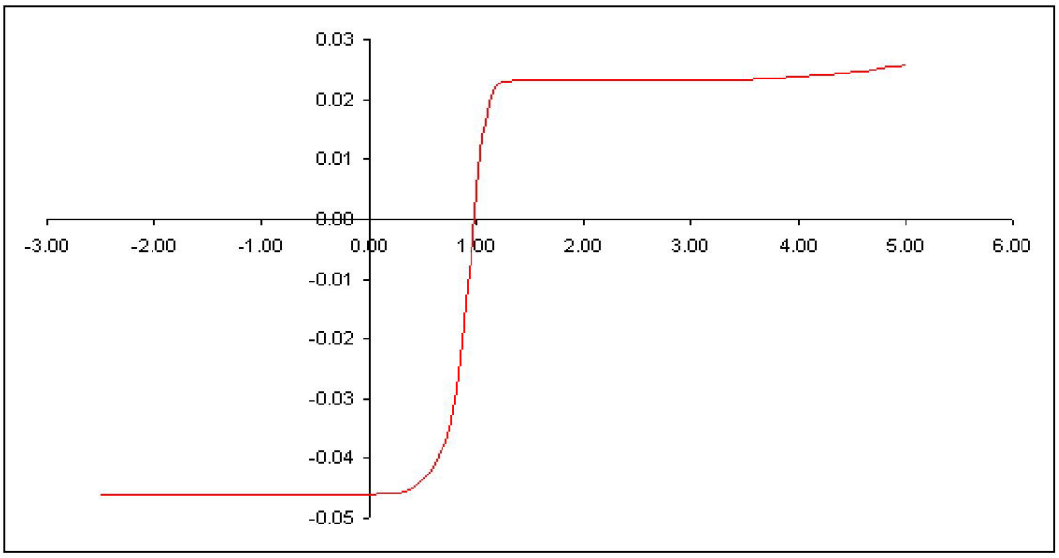

Figure 22. Properly Extracted Pulldown Curve

For the rising and falling waveform data, the repeated trailing values are truncated in order to make the "time window" as small as possible. Any data that is truncated in the rising waveform must also be truncated in the falling waveform to keep consistency between the rising and falling edges.

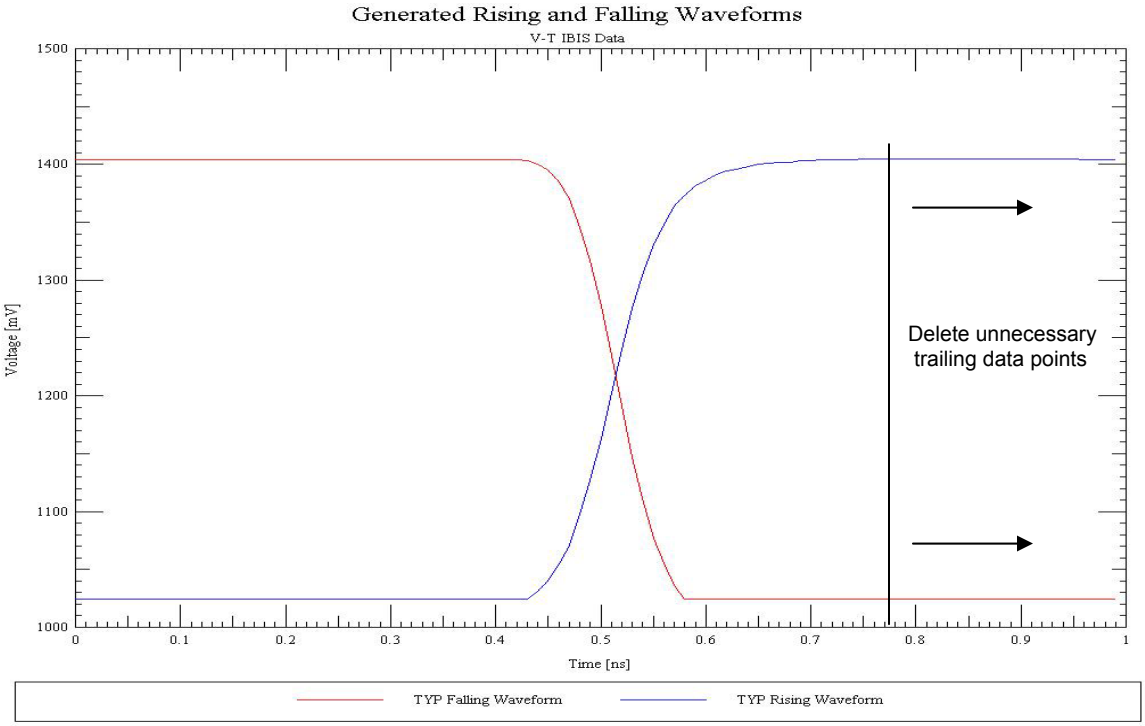

Figure 23. IBIS Rising and Falling Waveforms of LVDS Driver Output

In the previous graph, it can be seen that the rising and falling waveforms reach a steady state before 1nsec. Both the rising and falling waveforms can be truncated at 800psec, since the data after this time is repeating data. This also ensures that the “time window” for the V-T data is as small as possible to remain compatible with different IBIS simulators.

Package Model

The IBIS file also contains lumped R, L, and C values to represent the package of the device. National Semiconductor uses a 3-D field solver to extract these parameters and they are entered into the IBIS file. An IBIS simulator treats the package parasitic elements as a “lumped” model. For fast edge rates (<1 ns), this can affect simulation accuracy. For slower edge rates (>1 ns), the affect on accuracy is much less. The diff pin mapping section also needs to be filled in, assigning the differential pairs as inverting and non-inverting pins.

```
[Diff Pin] inv_pin     vdiff       tdelay_typ   tdelay_min   tdelay_max
|
| The '+' pin is Diff_pin and the '-' pin is the inv_pin
|
3        2          100mv       0            0            0
```

Figure 24. **Example of Diff Pin Mapping in IBIS File**

The Diff Pin is the non-inverting pin and the inv_pin is the inverting pin of the differential pair. If it is a differential input, then the vdiff parameter needs to be specified, which is the Vid of the inputs. The vdiff parameter is not specified for output pins. (0V is used) The tdelay parameters are for specifying launch delays of the non-inverting pin relative to the inverting pin.

Validating an IBIS File

Once an IBIS file has been created, the first step of validation is a syntax and IBIS parser check. The IBIS file must be passed through the IBIS parser, which is available for free from the IBIS Open Forum, in order to ensure that they are no errors in the model file. The IBIS parser checks for correct syntax and also checks to make sure that the IBIS data is valid. The following are some of the more important validation checks that National Semiconductor Interface Products Group uses on a newly created IBIS files:

- All model types have required keywords, such as logic levels and timing loads.
- All pins are declared with a package model.
- Data matches with all datasheet parameters such as VOD, Voh, Vol, etc.
- Conforms to current IBIS specification version 3.2.
- No errors when passed through IBIS parser.
- All warnings are documented.
- All I-V curves monotonic. Any non-monotonic points due to actual device operation should be documented.
- All V-T curves monotonic and reach steady. Any non-monotonic points due to actual device operation should be documented.
- All process corner data included unless lab generated IBIS file.
- Visual check on all waveforms to ensure monotonic and reasonable values.

Once an IBIS file has passed the initial parser check and a visual check, then the IBIS file is correlated to the original SPICE file under certain load conditions. This ensures that the IBIS file will behave properly in simulation.

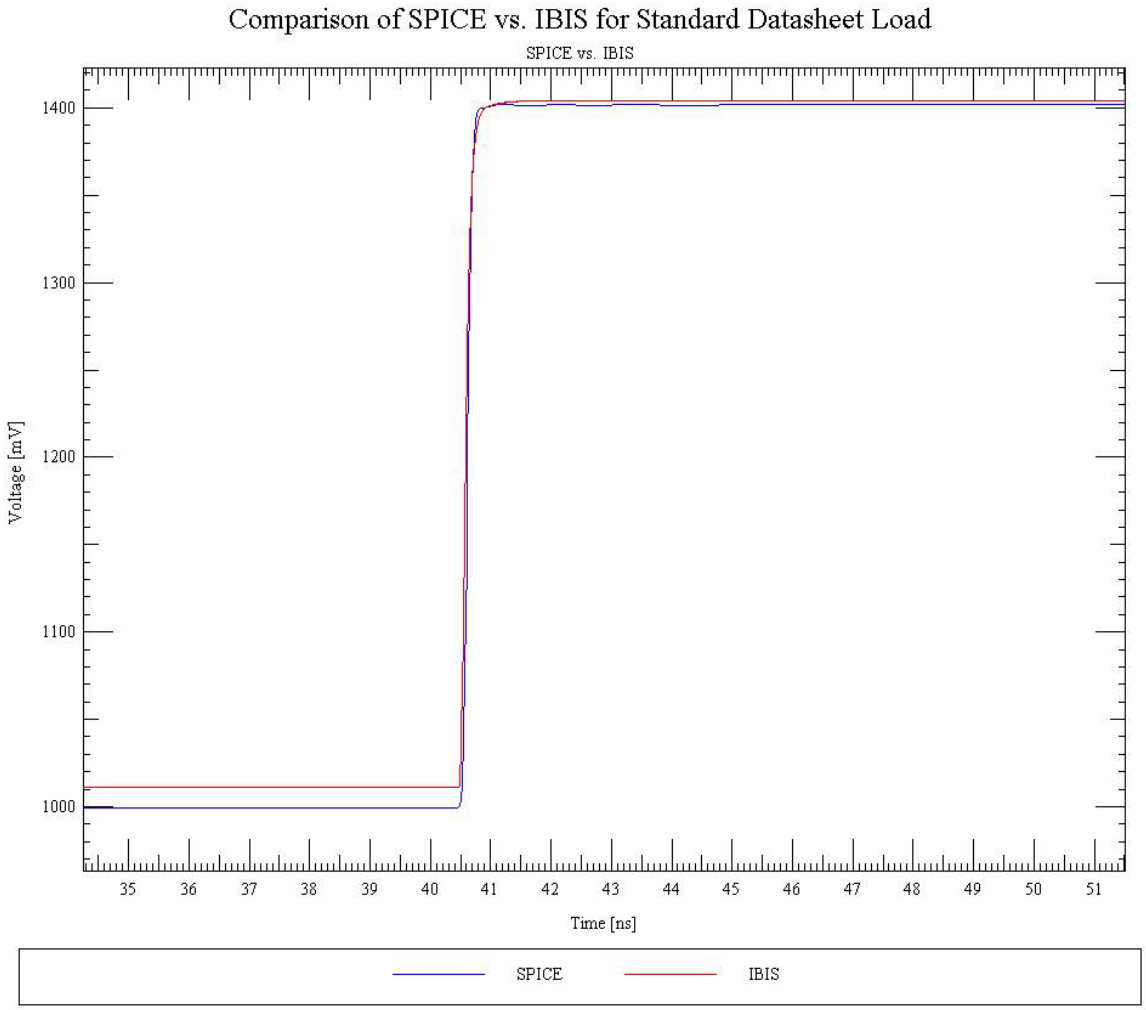

Figure 25. SPICE vs. IBIS for a Typical LVDS Device

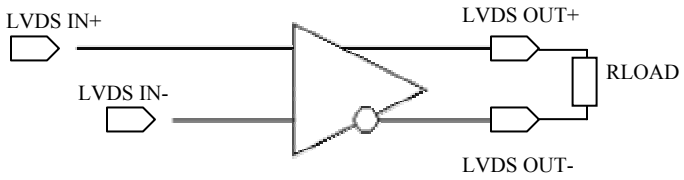

Figure 26. Simulation Setup for SPICE vs. IBIS Comparison

Notice there is a 10mV difference on the Vol between the SPICE and IBIS file. This can be attributed to the resolution of the generated IBIS data as well as the specific IBIS simulator used to simulate the IBIS file. Every IBIS simulator will interpret an IBIS file differently, as each simulator uses it's own algorithm to process the data. The following graph illustrates this point. The original SPICE model file was compared to the IBIS file under the same load, using different IBIS simulators. The three IBIS simulators used was Avanti HSPICE, Innoveda XTK, and Cadence Signal Explorer Expert.

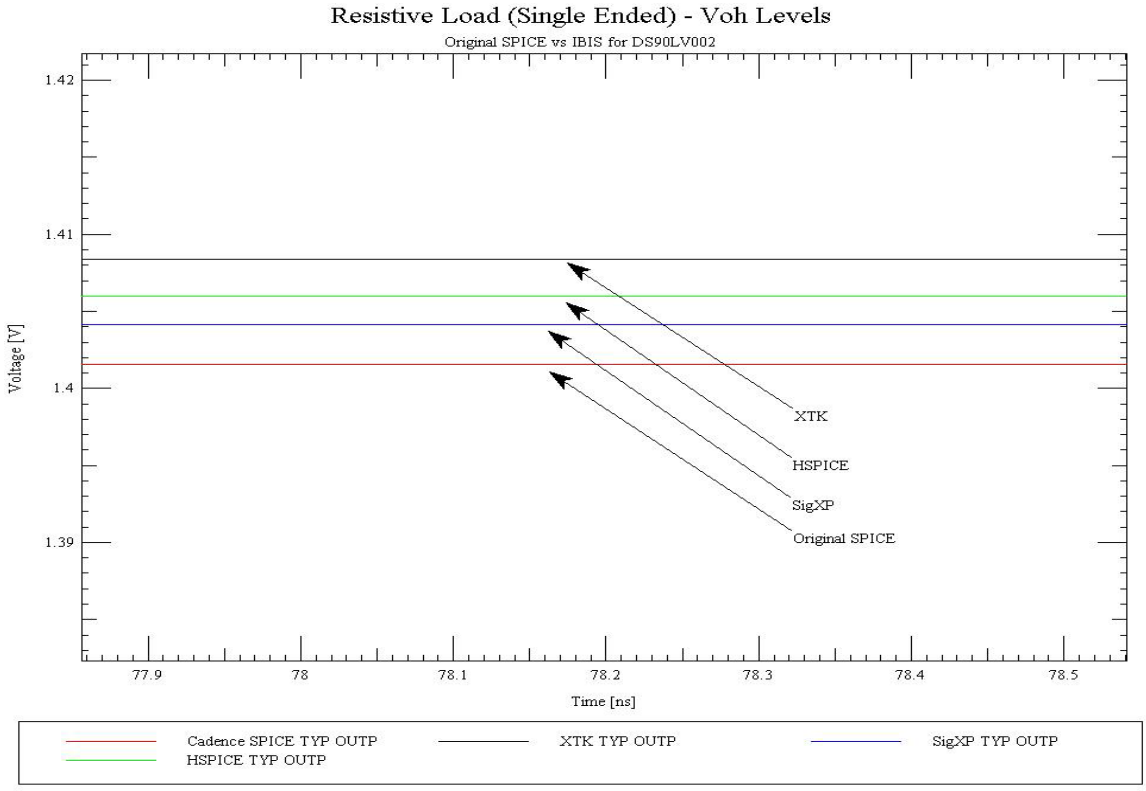

Figure 27. Comparison of IBIS Simulators vs. Original SPICE Model File

As can be seen from the graph above, the same IBIS file with the same test load in different simulators results in different Voh levels. The overall difference between the SPICE model file and the IBIS files is less than 10mV, but there is still a slight difference. Differences this small are deemed minor and can be ignored.

Summary

National Semiconductor has a rigid process in place to generate and validate IBIS files for Interface Products. This white paper covered the process of generating IBIS data, formatting the data, and validating the IBIS file using a LVDS device as an example. National Semiconductor will continue to enhance its model generation and validation process to provide the most accurate models possible.

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DS90LV001 IBIS File, National Semiconductor