Artix-7 FPGAs Data Sheet: DC and Switching Characteristics

DS181 (v1.10) January 23, 2014 **Product Specification**

Introduction

Artix®-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two V_{CCINT} voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at V_{CCINT} = 1.0V, the speed specification of a -2L device is the same as the -2 speed grade. When operated at V_{CCINT} = 0.9V, the -2L static and dynamic power is reduced.

Artix-7 FPGA DC and AC characteristics are specified in commercial, extended, industrial, expanded (-1Q), and military (-1M) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1M speed grade military device are the same as for a -1C speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range. For example, -1M is only available in the defense-grade Artix-7Q family and -1Q is only available in XA Artix-7 FPGAs.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in:

- *7 Series FPGAs Overview* (DS180)
- *Defense-Grade 7 Series FPGAs Overview* (DS185)
- *XA Artix-7 FPGAs Overview* (DS197)

This Artix-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.5	1.1	V
V_{CCAUX}	Auxiliary supply voltage	–0.5	2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5	1.1	V
V_{CCO}	Output drivers supply voltage for 3.3V HR I/O banks	–0.5	3.6	V
V_{REF}	Input reference voltage	–0.5	2.0	V
V_{IN}(2)(3)(4)	I/O input voltage	–0.4	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(5)	–0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTP Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTP transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	14	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	6.5	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	14	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(6)	–	+260	°C
T_j	Maximum junction temperature(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}(3)	Internal supply voltage	0.95	1.00	1.05	V
	For -2L (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}(3)	Block RAM supply voltage	0.95	1.00	1.05	V
V_{CCO}(4)(5)	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
V_{IN}(6)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(7)	–0.20	–	2.625	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(9)	Battery voltage	1.0	–	1.89	V
GTP Transceiver					
$V_{MGTAVCC}$(10)	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}$(10)	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices	–40	–	125	°C
	Junction temperature operating range for military (M) temperature devices	–55	–	125	°C

Notes:
1. All voltages are relative to ground.
2. For the design of the power distribution system consult UG483, *7 Series FPGAs PCB Design and Pin Planning Guide*.
3. If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
4. Configuration data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. The lower absolute voltage specification always applies.
7. See Table 9 for TMDS_33 specifications.
8. A total of 200 mA per bank should not be exceeded.
9. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
10. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}(2)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}(3)	Battery supply current	–	–	150	nA
R_{IN_TERM}(4)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40)	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50)	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60)	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI @–55°C to 125°C	AC Voltage Undershoot	% of UI @–55°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 5% or below GND – 0.30V, must not exceed the values in this table.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade					Units
			1.0V				0.9V	
			-3	-2	-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A35T						mA
		XC7A50T						mA
		XC7A75T	155	155	155	155	108	mA
		XC7A100T	155	155	155	155	108	mA
		XC7A200T	328	328	328	328	232	mA
		XA7A35T	N/A		N/A		N/A	mA
		XA7A50T	N/A		N/A		N/A	mA
		XA7A75T	N/A	155	N/A	155	N/A	mA
		XA7A100T	N/A	155	N/A	155	N/A	mA
		XQ7A50T	N/A		N/A		N/A	mA
		XQ7A100T	N/A	155	N/A	155	N/A	mA
		XQ7A200T	N/A	328	N/A	328	N/A	mA

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade					Units
			1.0V				0.9V	
			-3	-2	-2L	-1	-2L	
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A35T						mA
		XC7A50T						mA
		XC7A75T	4	4	4	4	4	mA
		XC7A100T	4	4	4	4	4	mA
		XC7A200T	5	5	5	5	5	mA
		XA7A35T	N/A		N/A		N/A	mA
		XA7A50T	N/A		N/A		N/A	mA
		XA7A75T	N/A	4	N/A	4	N/A	mA
		XA7A100T	N/A	4	N/A	4	N/A	mA
		XQ7A50T	N/A		N/A		N/A	mA
		XQ7A100T	N/A	4	N/A	4	N/A	mA
		XQ7A200T	N/A	5	N/A	5	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A35T						mA
		XC7A50T						mA
		XC7A75T	36	36	36	36	36	mA
		XC7A100T	36	36	36	36	36	mA
		XC7A200T	73	73	73	73	73	mA
		XA7A35T	N/A		N/A		N/A	mA
		XA7A50T	N/A		N/A		N/A	mA
		XA7A75T	N/A	36	N/A	36	N/A	mA
		XA7A100T	N/A	36	N/A	36	N/A	mA
		XQ7A50T	N/A		N/A		N/A	mA
		XQ7A100T	N/A	36	N/A	36	N/A	mA
		XQ7A200T	N/A	73	N/A	73	N/A	mA

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade					Units
			1.0V				0.9V	
			-3	-2	-2L	-1	-2L	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A35T						mA
		XC7A50T						mA
		XC7A75T	4	4	4	4	4	mA
		XC7A100T	4	4	4	4	4	mA
		XC7A200T	11	11	11	11	11	mA
		XA7A35T	N/A		N/A		N/A	mA
		XA7A50T	N/A		N/A		N/A	mA
		XA7A75T	N/A	4	N/A	4	N/A	mA
		XA7A100T	N/A	4	N/A	4	N/A	mA
		XQ7A50T	N/A		N/A		N/A	mA
		XQ7A100T	N/A	4	N/A	4	N/A	mA
		XQ7A200T	N/A	11	N/A	11	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies

have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: **Power-On Current for Artix-7 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7A35T					mA
XC7A50T					mA
XC7A75T	I_{CCINTQ} + 170	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7A100T	I_{CCINTQ} + 170	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7A200T	I_{CCINTQ} + 340	I_{CCAUXQ} + 50	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 80	mA
XA7A35T					mA
XA7A50T					mA
XA7A75T	I_{CCINTQ} + 170	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7A100T	I_{CCINTQ} + 170	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XQ7A50T					mA
XQ7A100T	I_{CCINTQ} + 170	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XQ7A200T	I_{CCINTQ} + 340	I_{CCAUXQ} + 50	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 80	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	T_J = 125°C(1)	–	300	ms
		T_J = 100°C(1)	–	500	
		T_J = 85°C(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00

Table 8: **SelectIO DC Input and Output Levels(1)(2) *(Cont'd)***

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}(1)			V_{ID}(2)			V_{OCM}(3)			V_{OD}(4)		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

Table 11: **LVDS_25 DC Specifications**[1]

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.