No R_{SENSE}™, Low Input Voltage, Synchronous Step-Down DC/DC Controller

FEATURES

- **No Current Sense Resistor Required**
- **All N-Channel MOSFET Synchronous Drive**
- **High Current Outputs Possible**
- Constant Frequency Current Mode Operation for Excellent Line and Load Transient Response
- V_{IN}: 2.75V to 4.5V
- ±1% 0.6V Reference
- Low Dropout Operation: 99% Duty Cycle
- Selectable Frequency (300kHz/550kHz/750kHz)
- Internal Soft-Start Circuitry
- Selectable Maximum Peak Current Sense Threshold
- Digital RUN Control Pin
- Output Overvoltage Protection
- Micropower Shutdown: I_Q = 7.5µA
- Tiny Thermally Enhanced Leadless (3mm x 3mm) DFN or 10-Lead MSOP Package

DESCRIPTION

The LTC3822 is a synchronous step-down switching regulator controller that drives external N-channel power MOSFETs using few external components. The constant frequency current mode architecture with MOSFET V_{DS} sensing eliminates the need for sense resistors and improves efficiency.

A maximum duty cycle of 99% provides low dropout operation. The switching frequency can be programmed up to 750kHz, allowing the use of small surface mount inductors and capacitors.

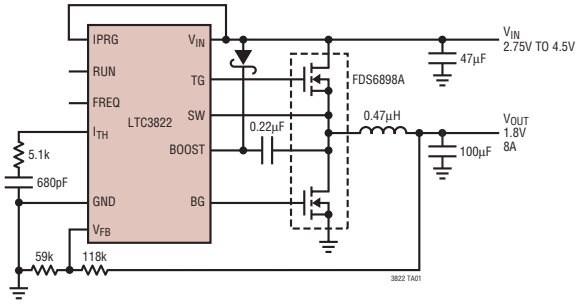
The LTC3822 is available in thermally enhanced DFN and 10-lead MSOP packages.

APPLICATIONS

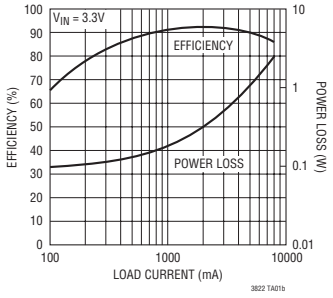
- 3.3V_{IN} Systems
- Li-Ion Battery Systems

TYPICAL APPLICATION

1.8V/8A High Efficiency, 550kHz Step-Down Converter



Efficiency and Power Loss vs Load Current

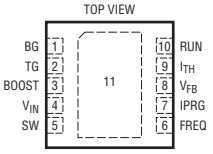


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 4.5V
BOOST Voltage ..... –0.3V to 10V
FREQ, RUN, IPRG Voltages ..... –0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH} Voltages ..... –0.3V to 2.4V
SW Voltage ..... –2V to V_{IN} + 1V
TG, BG Peak Output Current (<10µs) 1A

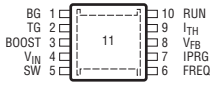
Operating Temperature Range
(Note 2) ..... –40°C to 85°C
Storage Ambient Temperature Range ... –65°C to 125°C
Junction Temperature (Note 3) ..... 125°C
Lead Temperature
(Soldering, 10 sec, MSE only) ..... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD IS GND
(MUST BE SOLDERED TO PCB)



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD IS GND
(MUST BE SOLDERED TO PCB)

ORDER PART NUMBER	DD PART MARKING	ORDER PART NUMBER	MSE PART MARKING
LTC3822EDD	LCBF	LTC3822EMSE	LTCBG

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
Input DC Supply Current Normal Operation Shutdown UVLO	(Note 4) RUN = 0 V_{IN} = UVLO Threshold – 200mV			 340 7.5 10	 500 20 20	 µA µA µA
Undervoltage Lockout Threshold	V_{IN} Falling V_{IN} Rising	● ●	1.95 2.15	2.25 2.45	2.55 2.75	V V
Shutdown Threshold Of RUN Pin			0.7	1.1	1.4	V
Regulated Feedback Voltage	(Note 5)	●	0.594	0.6	0.606	V
Output Voltage Line Regulation	2.75V < V_{IN} < 4.5V (Note 5)			0.025	0.1	%/V
Output Voltage Load Regulation	I_{TH} = 1.3V to 0.9V (Note 5) I_{TH} = 1.3V to 1.7V			0.1 –0.1	0.5 –0.5	% %

ELECTRICAL CHARACTERISTICS

The ● indicates specifications that apply over the full operating temperature range; otherwise, specifications are at T_A = 25°C. V_{IN} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB} Input Current	(Note 5)			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.66	0.68	0.70	V
Overvoltage Protect Hysteresis				20		mV
Top Gate (TG) Drive Rise Time	C_L = 3000pF			40		ns
Top Gate (TG) Drive Fall Time	C_L = 3000pF			40		ns
Bottom Gate (BG) Drive Rise Time	CL = 3000pF			50		ns
Bottom Gate (BG) Drive Fall Time	CL = 3000pF			40		ns
Maximum Duty Cycle	In Dropout			99		%
Maximum Current Sense Voltage (V_{IN} – SW) ($\Delta V_{SENSE(MAX)}$)	IPRG = Floating	●	110	120	140	mV
	IPRG = 0V	●	70	82	100	mV
	IPRG = V_{IN}	●	185	200	220	mV
Soft-Start Time	Time for V_{FB} to Ramp from 0.05V to 0.55V			650		µs
Oscillator						
Oscillator Frequency	FREQ = Floating		480	550	600	kHz
	FREQ = 0V		240	300	340	kHz
	FREQ = V_{IN}		640	750	850	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3822E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating range are assured by design characterization, and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

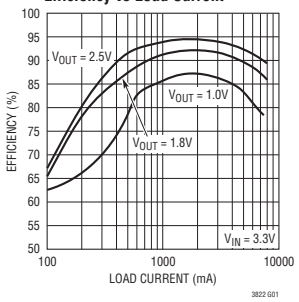
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3822 is tested in a feedback loop that servos I_{TH} to a specified voltage and measures the resultant V_{FB} voltage.

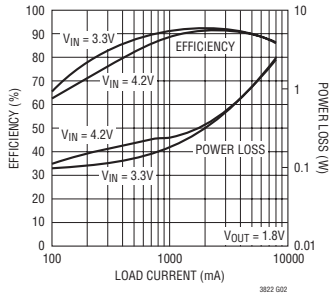
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

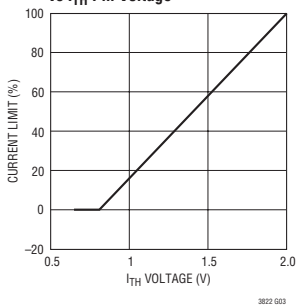
Efficiency vs Load Current



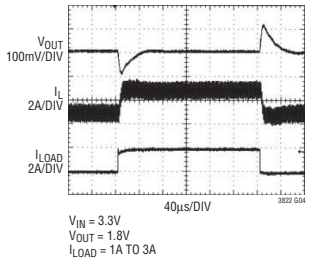
Efficiency and Power Loss vs Load Current



Maximum Current Sense Voltage vs I_{TH} Pin Voltage

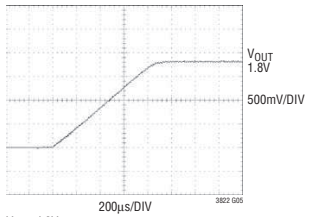


Load Step



V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 1A TO 3A

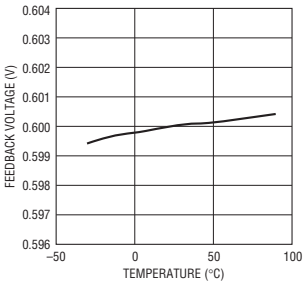
Start-Up with Internal Soft-Start



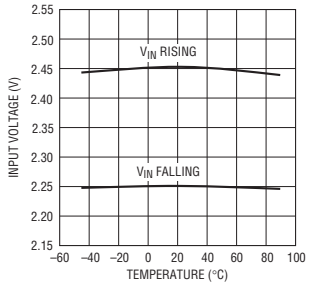
V_{IN} = 4.2V
R_{LOAD} = 1Ω

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

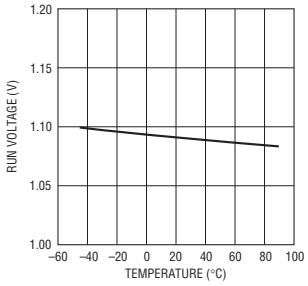
Regulated Feedback Voltage vs Temperature



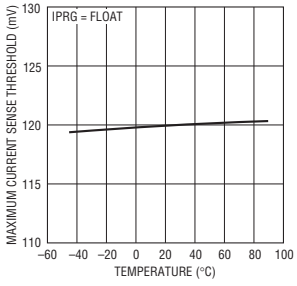
Undervoltage Lockout Threshold vs Temperature



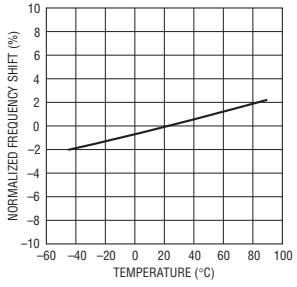
Shutdown (RUN) Threshold vs Temperature



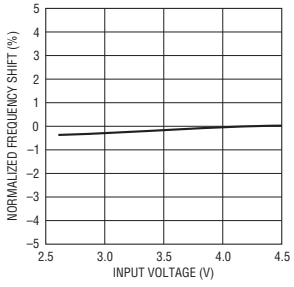
Maximum Current Sense Threshold vs Temperature



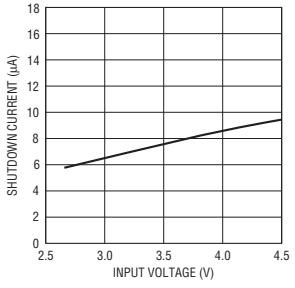
Oscillator Frequency vs Temperature



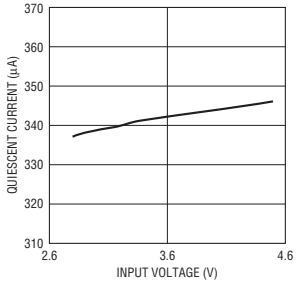
Oscillator Frequency vs Input Voltage



Shutdown Quiescent Current vs Input Voltage



Quiescent Current in Normal Operation vs Input Voltage



PIN FUNCTIONS

BG (Pin 1): Bottom Gate Driver Output. This pin drives the gate of the external bottom MOSFET. This pin has an output swing from GND to BOOST.

TG (Pin 2): Top Gate Driver Output. This pin drives the gate of the external topside MOSFET. This pin has an output swing from GND to BOOST.

BOOST (Pin 3): Positive Supply Pin for the Gate Driver Circuitry. A bootstrapped capacitor, charged through an external Schottky diode from V_{IN}, is connected between the BOOST and SW pins. Voltage swing at the BOOST pin is from V_{IN} to $2V_{IN}$. Alternatively, the diode can be connected to SW and a separate 5V supply to provide 5V gate drive. In this case, the BOOST pin swings from 5V to 5V + V_{IN}.

V_{IN} (Pin 4): This pin powers the control circuitry and serves as the positive input to the differential current comparator. Pin 4 must not be locally decoupled with a capacitor as it is also the positive terminal for current sense.

SW (Pin 5): Switch Node Connection to Inductor. This pin is also the negative input to the differential current comparator and an input to the reverse current comparator. Normally this pin is connected to the source of the external top-side MOSFET, the drain of the external bottom-side MOSFET, and the inductor.

FREQ (Pin 6): This pin serves as the frequency select input. Tying this pin to GND selects 300kHz operation; tying this pin to V_{IN} selects 750kHz operation. Floating this pin selects 550kHz operation.

IPRG (Pin 7): Selects maximum peak sense voltage between the V_{IN} and SW pins (i.e., the maximum allowed drop across the external top-side MOSFET). Tie to V_{IN}, GND or float to select 200mV, 82mV or 120mV respectively.

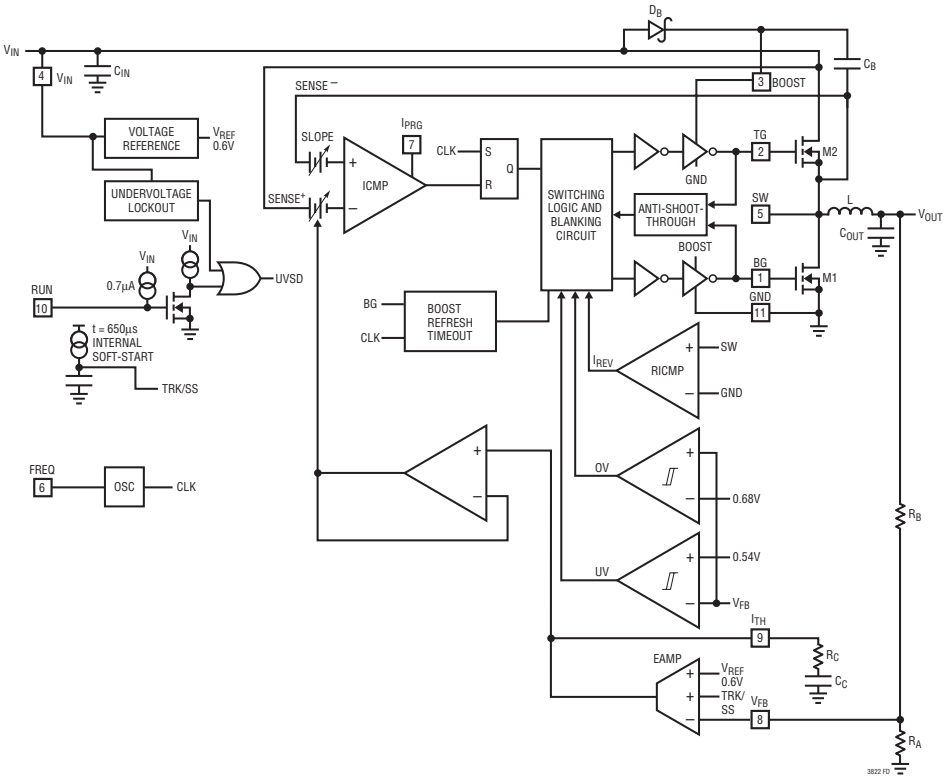
V_{FB} (Pin 8): Feedback Pin. This pin receives the remotely sensed feedback voltage from an external resistor divider across the output.

I_{TH} (Pin 9): Current Threshold and Error Amplifier Compensation Point. Nominal operating range on this pin is from 0.7V to 2V. The voltage on this pin determines the threshold of the main current comparator.

RUN (Pin 10): Run Control Input. Forcing this pin below 1.1V shuts down the chip. Driving this pin to V_{IN} or releasing this pin enables the chip to start-up with the internal soft-start.

GND (Pin 11): Exposed Pad. The exposed pad is ground and must be soldered to the PCB ground for electrical contact and optimal thermal performance.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3822 uses a constant frequency, current mode architecture. During normal operation, the top external N-channel power MOSFET is turned on when the clock sets the RS latch, and is turned off when the current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is determined by the voltage on the I_{TH} pin, which is driven by the output of the error amplifier (EAMP). The V_{FB} pin receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top N-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator RICMP, or the beginning of the next cycle.

Shutdown and Soft-Start (RUN Pin)

The LTC3822 is shut down by pulling the RUN pin low. In shutdown, all controller functions are disabled and the chip draws only 7.5µA. The TG and BG outputs are held low (off) in shutdown. Releasing the RUN pin allows an internal 0.7µA current source to pull up the RUN pin to V_{IN}. The controller is enabled when the RUN pin reaches 1.1V.

The start-up of V_{OUT} is controlled by the LTC3822's internal soft-start. During soft-start, the error amplifier EAMP compares the feedback signal V_{FB} to the internal soft-start ramp (instead of the 0.6V reference), which rises linearly from 0V to 0.6V in about 650µs. This allows the output voltage to rise smoothly from 0V to its final value while maintaining control of the inductor current.

Light Load Operation

LTC3822 operates discontinuously at low load currents. The reverse current comparator RICMP senses the drain-to-source voltage of the bottom external N-channel MOSFET. This MOSFET is turned off when the inductor current reaches zero. Under certain operating conditions brief inductor current reversal may cause continuous switching operation.

Short-Circuit Protection

The LTC3822 monitors V_{FB} to detect a short-circuit on V_{OUT}. When V_{FB} is near ground, switching frequency is reduced to prevent the inductor current from running away. The oscillator frequency will progressively return to normal when V_{FB} rises above ground. This feature is disabled during startup.

Output Overvoltage Protection

As further protection, the overvoltage comparator (OVP) guards against transient overshoots, as well as other more serious conditions that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 13.33% above the reference voltage of 0.6V, the external top-side MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage is cleared.

OPERATION (Refer to Functional Diagram)

Frequency Selection and Phase-Locked Loop (FREQ Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3822 is controlled via the FREQ pin. The FREQ pin can be floated, tied to V_{IN} or tied to GND to select 550kHz, 750kHz or 300kHz, respectively.

Undervoltage Lockout

To prevent operation of the power supply below safe input voltage levels, an undervoltage lockout is incorporated in the LTC3822. When the input supply voltage (V_{IN}) drops below 2.25V, the external MOSFETs and all internal circuits are turned off except for the undervoltage block, which draws only a few microamperes.

Peak Current Sense Voltage Selection and Slope Compensation (IPRG Pin)

When the LTC3822 controller is operating below 20% duty cycle, the peak current sense voltage (between the V_{IN} and SW pins) allowed across the external top-side MOSFET is determined by:

$$\Delta V_{SENSE(MAX)} = A \bullet \frac{V_{ITH} - 0.7V}{10}$$

where A is a constant determined by the state of the IPRG pin. Floating the IPRG pin selects A = 1; tying IPRG to V_{IN} selects A = 5/3; tying IPRG to GND selects A = 2/3. The maximum value of V_{ITH} is typically about 1.98V, so the maximum sense voltage allowed across the external P-channel MOSFET is 120mV, 82mV or 200mV for the three respective states of the IPRG pin.

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by a scale factor (SF) given by the curve in Figure 1.

The peak inductor current is determined by the peak sense voltage and the on-resistance of the external P-channel MOSFET:

$$I_{PK} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

Boost Capacitor Refresh Timeout

In order to maintain sufficient charge across C_B, the converter will briefly turn off the top MOSFET and turn on the bottom MOSFET if at any time the bottom MOSFET has remained off for 10 switching cycles. This most commonly occurs in a dropout situation.

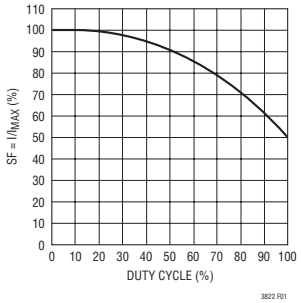


Figure 1. Maximum Peak Current vs Duty Cycle

APPLICATIONS INFORMATION

The typical LTC3822 application circuit is shown on the front page of this data sheet. External component selection for the controller is driven by the load requirement and begins with the selection of the inductor and the power MOSFETs.

Power MOSFET Selection

The LTC3822's controller requires external N-channel power MOSFETs for the topside (main) and bottom (synchronous) switches. The main selection criteria for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, turn-off delay $t_{D(OFF)}$ and the total gate charge Q_G.

The gate drive voltage is usually the input supply voltage. See Figure 7 for an application with a higher gate drive voltage. Since the LTC3822 is designed for operation at low input voltages, a sublogic level MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required.

The topside MOSFET's on-resistance is chosen based on the required load current. The maximum average load current $I_{OUT(MAX)}$ is equal to the peak inductor current minus half the peak-to-peak ripple current I_{RIPPLE}. The LTC3822's current comparator monitors the drain-to-source voltage V_{DS} of the top MOSFET, which is sensed between the V_{IN} and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin, of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 120mV when IPRG is floating (82mV when IPRG is tied low; 200mV when IPRG is tied high).

The output current that the LTC3822 can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation).

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}} \text{ for Duty Cycle} < 20\%$$

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ to provide the required amount of load current:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

where SF is a scale factor whose value is obtained from the curve in Figure 1.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3822 and external component values:

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho_T}$$

The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 2. Junction-to-case temperature ΔT_{JC} is about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C} \sim 1.3$ in the above equation is a reasonable choice.

APPLICATIONS INFORMATION

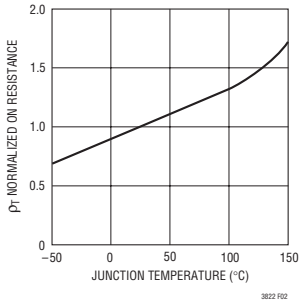


Figure 2. $R_{DS(ON)}$ vs Temperature

The power dissipated in the MOSFETs strongly depends on their respective duty cycles and load current. When the LTC3822 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$\text{Top MOSFET Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom MOSFET Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)} + 2 \bullet V_{IN}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Both MOSFETs have I^2R losses and the P_{TOP} equation includes an additional term for transition losses, which are largest at high input voltages. The bottom MOSFET losses are greatest at high input voltage or during a short-circuit when the bottom duty cycle is 100%.

The LTC3822 utilizes a non-overlapping, anti-shoot-through gate drive control scheme to ensure that the MOSFETs are not turned on at the same time. To function properly, the control scheme requires that the MOSFETs used are intended for DC/DC switching applications. Many power MOSFETs are intended to be used as static switches and therefore are slow to turn on or off.

Reasonable starting criteria for selecting the MOSFETs are that they must typically have a gate charge (Q_G) less than 30nC (at 2.5V_{GS}) and a turn-off delay ($t_{D(OFF)}$) of less than approximately 140ns. However, due to differences in test and specification methods of various MOSFET manufacturers, and in the variations in Q_G and $t_{D(OFF)}$ with gate drive (V_{IN}) voltage, the MOSFETs ultimately should be evaluated in the actual LTC3822 application circuit to ensure proper operation.

Shoot-through between the MOSFETs can most easily be spotted by monitoring the input supply current. As the input supply voltage increases, if the input supply current increases dramatically, then the likely cause is shoot-through.

Operating Frequency

The choice of operating frequency, f_{OSC}, is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

APPLICATIONS INFORMATION

The internal oscillator for the LTC3822's controller runs at a nominal 550kHz frequency when the FREQ pin is left floating. Pulling FREQ to V_{IN} selects 750kHz operation; pulling FREQ to GND selects 300kHz operation.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. Core saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when several layers of wire can be used, while inductors wound on bobbins are generally easier to surface mount. However, designs for surface mount that do not increase the height significantly are available from Coiltronics, Coilcraft, Dale and Sumida.

Schottky Diode Selection (Optional)

The schottky diode D in Figure 6 conducts current during the dead time between the conduction of the power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. A 2A Schottky diode is generally a good size for most LTC3822 applications, since it conducts a relatively small average current. Larger diodes result in additional transition losses due to larger junction capacitance. This diode may be omitted if the efficiency loss can be tolerated.

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle (V_{OUT}/V_{IN}). To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\,Required\,I_{RMS} \approx I_{MAX} \bullet \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})^{1/2}}{V_{IN}}$$

This formula has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the LTC3822, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE} \bullet \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increase with input voltage.

Top-Side MOSFET Drive Supply (C_B, D_B)

In the Functional Diagram, external bootstrap capacitor C_B is charged from a boost power source (usually V_{IN}) through diode D_B when the SW node is low. When a MOSFET is to be turned on, the C_B voltage is applied across the gate-source of the desired device. When the top-side MOSFET is on, the BOOST pin voltage is above the input supply. $V_{BOOST} = 2V_{IN}$. C_B must be 100 times the total input capacitance of the top-side MOSFET. The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$. Figure 6 shows how a 5V gate drive can be achieved if a secondary 5V supply is available. Note that in applications where the supply voltage to C_B exceeds V_{IN}, the BOOST pin will draw approximately 500µA in shutdown mode.

Setting Output Voltage

The LTC3822 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

For most applications, a 59k resistor is suggested for R_A. In applications where minimizing the quiescent current is critical, R_A should be made bigger to limit the feedback divider current. If R_B then results in very high impedance, it may be beneficial to bypass R_B with a 50pF to 100pF capacitor C_{FF}.

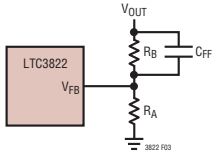


Figure 3. Setting the Output Voltage

APPLICATIONS INFORMATION

Low Input Supply Voltage

Although the LTC3822 can function down to below 2.4V, the maximum allowable output current is reduced as V_{IN} decreases below 3V. Figure 4 shows the amount of change as the supply is reduced down to 2.4V. Also shown is the effect on V_{REF}.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$ is the smallest amount of time that the LTC3822 is capable of turning the top MOSFET on. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle and high frequency applications may approach the minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f_{OSC} \bullet V_{IN}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3822 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase. The minimum on-time for the LTC3822 is typically about 170ns. However, as the peak sense voltage ($I_{L(PEAK)} \bullet R_{DS(ON)}$) decreases, the minimum on-time gradually increases up to about 260ns.

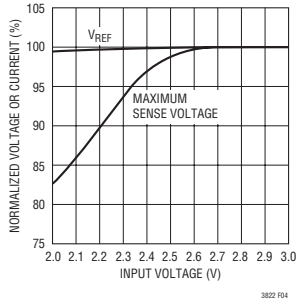


Figure 4. Line Regulation of V_{REF} and Maximum Sense Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + …)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3822 circuits: 1) LTC3822 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses and 4) transition losses.

1) The V_{IN} (pin) current is the DC supply current, given in the Electrical Characteristics, which excludes MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN}.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from BOOST to ground. The resulting dQ/dt is a current out of BOOST, which is typically much larger than the V_{IN} supply current. In continuous mode, $I_{GATECHG} = f \bullet Q_P$.

3) I^2R losses are calculated from the DC resistances of the MOSFETs, inductor and/or sense resistor. In continuous mode, the average output current flows through L but is "chopped" between the top MOSFET and the bottom MOSFET. Each MOSFET's $R_{DS(ON)}$ can be multiplied by its respective duty cycle and summed together with the DCR of the inductor to obtain I^2R losses.

4) Transition losses apply to the external MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

Transition Loss = $2 \bullet V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD}) \bullet (ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C-C_C filter (see the Functional Diagram) sets the dominant pole-zero loop compensation.

The I_{TH} external components showed in the figure on the first page of this data sheet will provide adequate compensation for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitor needs to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25) \bullet (C_{LOAD})$. Thus a 10µF capacitor would be require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

For a design example, V_{IN} will be a 3.3V power supply. Output voltage is 1.2V with a load current requirement of 10A. The IPRG and FREQ pins will be left floating, so the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ will be approximately 120mV and the switching frequency will be 550kHz.

$$\text{Duty Cycle} = \frac{V_{OUT}}{V_{IN}} = 36.4\%$$

From Figure 1, SF = 96%.

$$R_{DS(ON)MAX} = \frac{5}{6} \bullet 0.9 \bullet SF \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \bullet \rho T} = 0.011\Omega$$

The Si4486DY has an $R_{DS(ON)}$ of 9mΩ. To prevent inductor saturation during a short circuit, the inductor current rating should be higher than 20A.

For 4A I_{RIPPLE}, the required minimum inductor value is:

$$L_{MIN} = \frac{1.2V}{550kHz \bullet 4A} \bullet \left(1 - \frac{1.2V}{3.3V}\right) = 0.35\mu H$$

A 22A 0.39µH inductor works well for this application.

C_{IN} will require an RMS current rating of at least 5A at temperature. A C_{OUT} with 25mΩ ESR will cause approximately 100mV output ripple. Figure 7 shows a 12A, $3.3V_{IN}/1.8V_{OUT}$ application.

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, use the following checklist to ensure proper operation of the LTC3822. Figure 5 shows a suggested PCB floorplan.

- The power loop (input capacitor, MOSFET, inductor, output capacitor) and high di/dt loop (V_{IN}, through both MOSFETs to power GND and back through C_{IN} to V_{IN}) should be as small as possible and located on one layer. Excess inductance here can cause increased stress on the MOSFETs and increased high frequency ringing on the output.
- Put the feedback resistors close to the V_{FB} pins. The I_{TH} compensation components should also be very close to the LTC3822. All small-signal circuitry should be isolated from the main switching loop with ground Kelvin connected to the output capacitor ground.
- The current sense traces (V_{IN} and SW) should be Kelvin connected right at the top-side MOSFET source and drain. The positive current sense pin is shared with the V_{IN} pin. This must not be locally decoupled with a capacitor.
- Keep the switch node (SW) and the gate driver nodes (TG, BG) away from the small-signal components, especially the feedback resistors, and I_{TH} compensation components.
- Place CB as close as possible to the SW and BOOST pins. This capacitor carries high di/dt MOSFET gate drive currents. The charging current to the boost diode should be provided from a separate V_{IN} trace than that to the V_{IN} pin.
- Beware of ground loops in multiple layer PC boards. Try to maintain one central signal ground node on the board. If the ground plane must be used for high DC currents, keep that path away from small signal components.

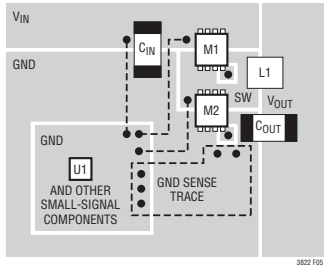


Figure 5. LTC3822 Suggested PCB Floorplan

APPLICATIONS INFORMATION

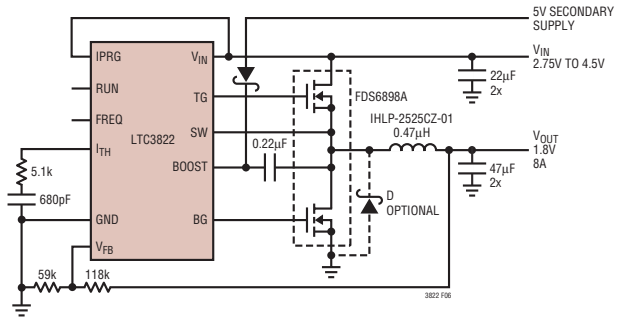


Figure 6. Nominal 3.3V$_{IN}$ 1.8V/8A High Efficiency 550kHz Step-Down Converter with 5V Gate Drive

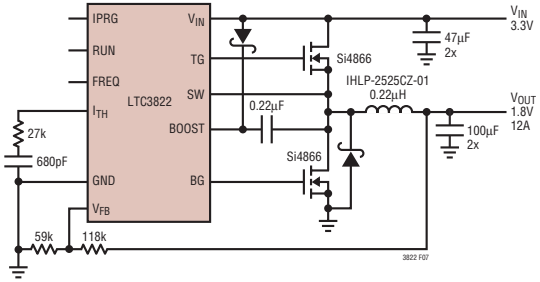
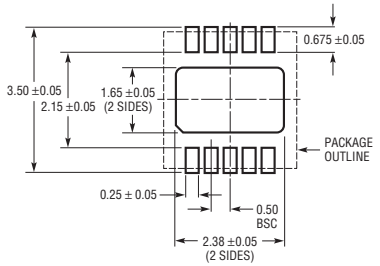


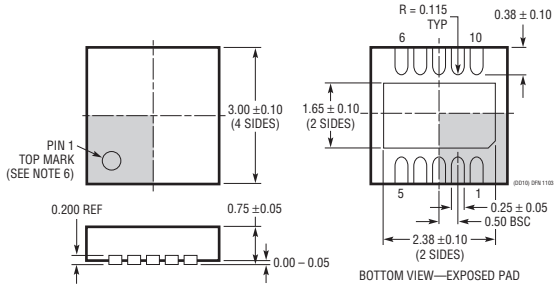
Figure 7. 3.3V$_{IN}$ 1.8V/12A High Efficiency, High Current 550kHz Step-Down Converter

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



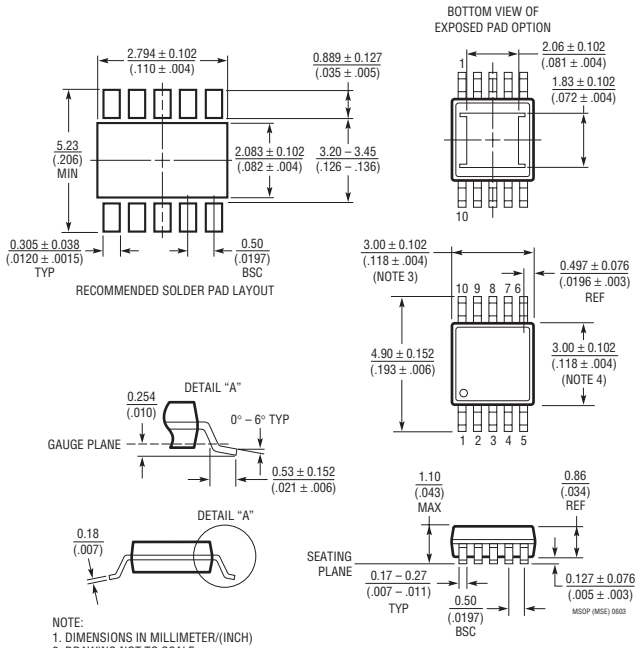
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1663)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC3728	Dual High Efficiency, 2-Phase Synchronous Step Down Controllers	Constant Frequency, Standby, 5V and 3.3V LDOs, V_{IN} to 36V, 28-Lead SSOP
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, $3.5V \le V_{IN} \le 36V$
LTC1778	No R_{SENSE}, Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, $4V \le V_{IN} \le 36V$
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT} \ge 0.8V$, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT} \ge 0.8V$, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3416	4A, 4MHz, Monolithic Synchronous Step-Down Regulator	Tracking Input to Provide Easy Supply Sequencing, $2.25V \le V_{IN} \le 5.5V$, 20-Lead TSSOP Package
LTC3418	8A, 4MHz, Synchronous Step-Down Regulator	Tracking Input to Provide Easy Supply Sequencing, $2.25V \le V_{IN} \le 5.5V$, QFN Package
LTC3708	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	Constant On-Time Dual Controller, V_{IN} Up to 36V, Very Low Duty Cycle Operation, 5mm × 5mm QFN Package
LTC3736/LTC3736-2	2-Phase, No R_{SENSE}, Dual Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN
LTC3736-1	Low EMI 2-Phase, Dual Synchronous Controller with Output Tracking	Integrated Spread Spectrum for 20dB Lower "Noise," $2.75V \le V_{IN} \le 9.8V$
LTC3737	2-Phase, No R_{SENSE}, Dual DC/DC Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, $0.6V \le V_{OUT} \le V_{IN}$, 4mm × 4mm QFN
LTC3772/LTC3772B	Micropower No R_{SENSE} Step-Down DC/DC Controller	$2.75V \le V_{IN} \le 9.8V$, 3mm × 2mm DFN or 8-Lead SOT-23, 550kHz, I_Q = 40µA, Current Mode
LTC3776	Dual, 2-Phase, No R_{SENSE} Synchronous Controller for DDR/QDR Memory Termination	Provides V_{DDQ} and V_{TT} with One IC, $2.75V \le V_{IN} \le 9.8V$, Adjustable Constant Frequency with PLL Up to 850kHz, Spread Spectrum Operation, 4mm × 4mm QFN and 24-Lead SSOP Packages
LTC3808	Low EMI, Synchronous Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, 4mm × 3mm DFN, Spread Spectrum for 20dB Lower Peak Noise
LTC3809/LTC3809-1	No R_{SENSE} Synchronous Controller	$2.75V \le V_{IN} \le 9.8V$, 3mm × 3mm DFN and 10-Lead MSOPE Packages
LTC3830	High Power Synchronous Step-Down Controller for Low Voltages (3V to 8V)	$3V \le V_{IN} \le 8V$, 500kHz, S8, S16 and SSOP-16 Packages

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