MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation

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A B S T R A C T

This paper presents a novel four-terminal variable capacitor (FTVC) dedicated to the recent concept of low power capacitive adiabatic logic (CAL). This FTVC is based on silicon nano/micro technologies and is intended to achieve adiabatic logic functions with a better efficiency that by using field effect transistor (FET). The proposed FTVC consists of two capacitors mechanically coupled and electrically isolated, where a comb-drive input capacitor controls a gap-closing capacitor at the output. To fully implement the adiabatic combinational logic, we propose two types of variable capacitors: a positive variable capacitor (PVC) where the output capacitance value increases with the input voltage, and a negative variable capacitance (NVC) where the output capacitance value decreases when the input voltage increases. A compact and accurate electromechanical model has been developed. The electromechanical simulations demonstrate the ability of the proposed FTVC devices for CAL, with improved features such as high logic states differentiation larger than 50% of the full-scale input signal and cascadability of both buffers and inverters. Based on the presented analysis, 89% of the total injected energy in the device can be recovered, the remaining energy being dissipated through mechanical damping. During one cycle of operation, a buffer gate of 10 × 2.5 µm\(^2\) dissipates only 0.9fJ.

1. Introduction

A digital electronic circuit can be considered as a chain of interconnected elementary blocks [1], each of them having an input capacitance \(C_0\) corresponding to the gate capacitor of a field effect transistor (FET) and some parasitic interconnections. In current CMOS technology, the classical combinational logic is based on the abrupt charge and discharge of \(C_0\) through PMOS and NMOS transistors for coding a logic state, as in the CMOS inverter (Fig. 1a). When changing from “0” to “1” logic state (\(V_{in} \to 0\), \(C_0\) is charged from the power supply \(V_{CC}\) through the PMOS resistance in on-state \(R_{on}\) while the NMOS is in its cut-off region (Fig. 1b). During this operation, the energy provided by the source is given by \(Q_{VCC} = C_0V_{CC}^2f\): half of it is dissipated through \(R_{on}\) and the other half is stored in \(C_0\). When changing from “1” to “0” (\(V_{in} \to 1\)), \(C_0\) is now discharged to the ground through the NMOS transistor in ON state (Fig. 1c). The energy previously stored in \(C_0\) is now dissipated into the ground and the total energy provided by the source is eventually fully dissipated.

In addition to the active power dissipation \(C_0V_{CC}^2f\), where \(f\) is the operating frequency, there are dissipation due to the short-circuit transition and the sub-threshold leakage \(I_{leak}V_{CC}\), where \(I_{leak}\) is the sub-threshold leakage current. The short-circuit transition power corresponds to about 10% of the average power and is typically the smallest contribution to the losses [3–5]. Though among all VLSI logic families, CMOS circuits have the lowest power dissipation [2,3], reducing the energy consumption is one of the main concerns in modern integrated circuits (IC). It can be reduced by (i) developing devices with higher sub-threshold slope, (ii) reducing \(C_0\) and (iii) working at low frequency. Reducing \(C_0\) is limited by the lithography. Reducing the supply voltage \(V_{CC}\) is a powerful method but this solution has limits related to the transistor size reduction [6]. Consequently, the dissipation cannot be reduced significantly.

In the early sixties, Landauer stated that to erase one bit of known information, which is consider as the most basic computing event, it requires the dissipation of at least \(k_B T \ln(2)\), where \(k_B\) is the Boltzman constant and \(T\) is the temperature in Kelvin [7]. At room temperature, it corresponds to 18 meV. However, to overcome the energy barrier due to the thermal noise, a minimum of 100.\(k_B\) \(T\) (~ 2.6 eV at 300°K) is required [8]. As a comparison, the current dissipated energy at each switching event, with the 10nm CMOS technology, is given by \(0.5C_0V_{CC}^2\sim 40\) eV, which is about 3 orders of magnitude above the Landauer limit and one order of magnitude above the thermal noise...

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A good way to even further reduce the power consumption is the adiabatic logic approach [6,9], which can be combined with the concept of “energy recovery” [10]. It consists in charging the gate capacitor with a constant current, instead of a constant voltage as in classical digital circuits, then to recover the injected charge when going back to the initial state. It results in an optimized power dissipation [11] but requires a dynamic logic: the charge and discharge of $C_o$ have to be performed by a ramped supply voltage signal $V_{PC}$ called the Power Clock (PC).

1.1. Dissipated energy in CMOS adiabatic logic

The principle of the adiabatic logic is detailed in [6,9]. To explain the principle of operation of an adiabatic logic gate, let us consider the schematic of the inverter gate in Fig. 1a. The PC signal is typically divided into 4 equal steps of equal duration $T$, that we named the Evaluate ($E$), Hold ($H$), Recovery ($R$) and Wait ($W$) intervals. Consequently, a logic “1” state at the input voltage $V_{in}$ is not a DC voltage value anymore as well. It corresponds to the power clock signal but shifted by a quarter of period $T$, as shown in Fig. 1d.

During the charging phase (Evaluate stage), the supply voltage is ramped from 0 to $V_{CC}$ within the charging time $T$, and the current $i$ is determined by:

$$i = C_o \frac{dV_{CC}}{dt} = C_o \frac{V_{CC}}{T}$$

The energy dissipated through $R_{on}$ during the charging and discharging phases is then given by:

$$E_{\text{dynamic}} = 2i^2R_{on}T = 2 \left( \frac{C_oV_{CC}}{T} \right)^2 R_{on}T = 2 \frac{R_{on}C_o^2}{T} C_o V_{CC}^2$$

If the time constant $2R_{on}C_o$ is lower than $T$, the energy dissipation is reduced compared to the energy dissipation $C_o V_{CC}^2$ in classical CMOS circuits. The ramp duration of the PC (also equal to $T$) strongly affects the Joule dissipation: $E_{\text{dynamic}}$ vanishes for long charging times. Similarly, scaling down the supply voltage and reducing the capacitance load also reduce the dissipated energy in adiabatic logic, as we mentioned earlier.

In addition, it exists a non-adiabatic energy associated to the incompressible threshold voltage $V_{th}$ of the MOS transistor equal to:

$$E_{\text{non-adiabatic}} = \frac{1}{2} C_o V_{th}^2$$

A nanorelay current can flow from the supply voltage to the ground through the disable transistors due to the semiconductor technology, leading to a static energy dissipation given by:

$$E_{\text{static}} = \frac{I_{\text{leak}} V_{CC}}{f}$$

where $I_{\text{leak}}$ is the mean leakage current.

By taking into account the (adiabatic) dynamic losses, the (static) leakage and the (incompressible) non-adiabatic losses, we can express the total energy dissipation of an adiabatic inverter gate based on CMOS transistors as:

$$E_{\text{Total}} = 2 \frac{R_{on}C_o^2}{T} C_o V_{CC}^2 + \frac{1}{2} C_o V_{th}^2 + I_{\text{leak}} V_{CC} \frac{1}{f}$$

1.2. Electromechanical devices to reduce the non-adiabatic losses

Nano-Electromechanical relays (NEMS relays) have been proposed to replace CMOS transistors in order to reduce the static and non-adiabatic losses. Most of them are electrostatically actuated [12,13] but a nanomagnetic switch could also be used [8]. These nanorelays need low switching energy and promise perfect isolation with zero leakage.
current in the OFF state. They have already been evaluated for classical logic \cite{14,15} and even tested with an integrated circuit \cite{16}. In addition, they can be used efficiently for the adiabatic logic \cite{17}.

A classical NEMS relay has typically three terminals, the gate (G), the source (S) and the drain (D) (Fig. 1e). It consists in an electrostatic actuator made of a flexible beam S and a fixed electrode G, forming a variable capacitance \( C_g \). The voltage across \( C_g \) determines the state of the relay. In the OFF state, \( C_g \) is low and the resistance \( R \) between the drain and the source is infinite (open circuit). When an input voltage is applied between \( S \) and \( G \), the beam deflects and creates a resistive contact between the drain and the source (ON states). Consequently, the relay can be seen as a capacitor controlling a variable resistor, represented with the symbol in Fig. 1f. To implement all combinational logic, we need two types of relay: normally-ON and normally-OFF relays to replace the NMOS and PMOS transistors in integrated circuits respectively. Fig. 1g illustrates how the relays (or the MOS transistors) can be implemented in an adiabatic inverter.

However, the unavoidable contact resistance of resistive micro/nano-electromechanical relays, their poor mechanical reliability and their low switching frequencies have been highlighted in literature \cite{12–17}. In order to avoid the resistive contact in the on-state and to reduce the dynamic dissipation, a purely capacitive electromechanical switch could be a better solution \cite{18}. Based on this new paradigm, the so-called Capacitive Adiabatic Logic (CAL), Galsultanov et al. have detailed in \cite{19} the concept of a fully contact-less electromechanical device for the CAL. In this paper we described new four-terminal variable capacitors (FTVC) for the CAL that still have a contact zone but present several major advantages, like a better differentiation between a “0” and a “1” logic state, a higher frequency of operation or a smaller area. In addition, based on our simulations, we demonstrated for the first time the ability to cascade several devices.

The organization of the paper is as follows. In the next section, we detail these new FTVC and their mathematical models that can be used to implement the CAL approach. In Section 3, we analyze the different energy losses of the proposed configurations. We conclude with the demonstration of the operation of cascaded elementary combinational gates.

2. Proposed architectures for the CAL devices

2.1. General description

In the Capacitive Adiabatic Logic approach, the resistive elements (transistors or relays) are replaced by purely capacitive elements. Similarly to the resistive-based adiabatic logic, the logic function required an input capacitance \( C_{in} \) between the gate \( G \) and the ground, and an output capacitance \( C_{out} \) between the terminals \( D \) and \( S \) (we use the FET transistor notation, i.e. the input voltage \( V_{in} \) is applied between the gate and the ground). The only difference is that the electrodes of \( C_{in} \) are never in ohmic contact. All the terminals are electrically isolated, but two of them (\( G \) and \( S \)) are mechanically connected. Two types of output variable capacitances are needed to fully implement the adiabatic combinational logic: Positive Variable Capacitances (PVC) where \( C_{POS} \) increases with the control voltage \( V_{PC} \) and Negative Variable Capacitances (NVC) where \( C_{NOS} \) decreases when \( V_{in} \) increases.

In the following, we propose implementations for a PVC and a NVC that can be fabricated in silicon micro/nanotechnologies. Each device consists of an electrostatic comb-drive actuator for the input capacitance \( C_{in} \) and a gap-closing (possibly with interdigitated-combs) for the output capacitor \( C_{out} \). The capacitance \( C_{in} \) and \( C_{out} \) are mechanically connected but electrically separated by a dielectric. Fig. 2a shows a schematic top-view of a practical buffer using a PVC and Fig. 2b depicts an inverter with a NVC, both in the OFF state. Fig. 2c,d,e give more geometric details of \( C_{in} \), the spring mechanical suspensions and \( C_{out} \) respectively.

2.2. Principle of the PVC configuration

Let’s assume that the buffer in Fig. 2a is loaded with the signals presented in Fig. 1d. In the OFF state \( (V_{out}=0) \), the electrodes \( S \) and \( D \) are separated by \( d_{max} \), and the capacitance \( C_{POS} \) is minimum (Fig. 3a). When \( V_{out} \) is applied (ON state), the comb-drive moves the rotor in the \( x \) direction, resulting in an increase of \( C_g \) and \( C_{POS} \). According to the capacitor divider \( C_g/C_{POS} \), the output \( V_{out} \) follows \( V_{PC} \). The electrical force \( F_e \), created by the voltage \( V_{POS}=V_{PC}-V_{out} \), is opposed to the mechanical spring force \( F_m \) (Fig. 3b). Consequently, during the Hold interval when \( V_{in} \) decreases, \( F_e \) balances \( F_m \) and the equilibrium is maintained: \( C_g \) and \( C_{POS} \) remain constant, allowing \( V_{out} \) to still follow \( V_{PC} \).

2.3. Principle of the NVC configuration

Now we consider the inverter in Fig. 2b loaded with the same signals in Fig. 1d. In the OFF state \( (V_{out}=0) \), \( C_{POS} \) is maximal because \( S \) and \( D \) are separated by \( d_{max} \), the thickness of a dielectric layer covering the electrodes (Fig. 3c). When \( V_{out} \) is applied (ON state), the comb-drive moves the rotor in the \( x \) direction, resulting in an increase of \( C_g \) and a decrease of \( C_{NOS} \). This time, the electrical force \( F_e \) and spring force \( F_m \) are in the same direction (Fig. 3d). Consequently, during the Hold interval when \( V_{in} \) decreases, the mobile electrode may return to its initial position causing an incorrect operation. To avoid this problem, we proposed to add an additional electrode \( M \) connected to the ground and forming with \( S \) a capacitance \( C_{GM} \). The voltage across \( C_{GM} \) creates an additional electrical force \( F_e' \) that balances the other forces and the equilibrium can be maintained (Fig. 3e,f).

2.4. The adiabatic conditions

2.4.1. Conditions related to input signals

In order to satisfy the adiabatic conditions, the inputs have to be stable during ramp-up and ramp-down phases of the PC, and the durations of the Evaluate, Hold, and Wait phases of both input and power-clock signals have to be equal \cite{20,21}. Therefore, as already stated in the introduction, a four-phase power clock consisting in four equal intervals \( T \) is required, and the input signal is shifted by a quarter of period with respect to the PC. In the ON state, the following rules have to be followed :

(i) During the Wait interval, \( V_{in} \) ramps up, \( C_{in} \) increases and reaches its maximum value at the end of the interval. As soon as \( C_{in} \) increases, \( C_{POS} \) evolves depending on the gate configuration: for a PVC, it increases until its maximum and for the NVC, it decreases to its lower value.

(ii) During the Evaluate interval, \( V_{PC} \) increases and \( V_{in} \) remains constant at its high value. In the PVC configuration, the output \( V_{out} \) follows the PC and the capacitance node \( C_o \) starts to charge. In the NVC, the output remains at a low level.

(iii) During the Hold interval, \( V_{in} \) decreases but \( V_{PC} \) remains high, and then the variables capacitances \( C_g \) and \( C_{POS} \) doesn’t change (thanks to the help of electrode \( M \) for the NVC).

(iv) During the Recover interval, \( V_{PC} \) decreases while \( V_{in} \) remains grounded. The mechanical equilibrium is holded until low value of \( V_{PC} \), thanks to the typical hysteresis in electrostatic transducers \cite{23}. Both \( C_g \) and \( C_{POS} \) remain constant till then, and the charge stored in \( C_o \) can be recovered by the source.

To build a circuit, the CALs gates are cascaded and each gate is supplied by a PC, as shown in Fig. S1. Since the output signal follows the PC, two subsequent PC should be delayed by a quarter of period to satisfy the adiabatic conditions. Therefore, a four-phase power-clock \((V_{P(1)} \text{ to } V_{P(4)})\) is needed to cascade several gates.
2.4.2. Conditions related to CDS

Fig. 4 shows schematic representations of a buffer and an inverter. The PVC design has four terminals while NVC has five, since it includes the additional electrode $M$. The electrical equations are given by:

$$V_{DS} = V_{DS} + V_{out}$$  \hspace{1cm} (6)

$$i = C_{DS} \frac{dV_{DS}}{dt} + V_{DS} \frac{dC_{DS}}{dt} = C_{o} \frac{dV_{out}}{dt}$$  \hspace{1cm} (7)

where $V_{DS}$, $C_{o}$, and $i$ are the voltage across the drain and source of either PVC or NVC, the input capacitance of the following gate and the current provided by the power clock respectively. We can deduce the instantaneous logic output voltage as:

$$V_{out} = V_{PC} \frac{C_{DS}}{C_{DS} + C_{o}}$$  \hspace{1cm} (8)

Since the input voltage $V_{in}$ controls the value of $C_{DS}$, it also controls the voltage ratio between the power-clock signal and the output node through the capacitor bridge divider ($C_{DS}$-$C_{o}$). The values of $C_{DS}$ have to be carefully chosen: the minimum value of $C_{DS}$ has to be small compared to $C_{o}$ in order to obtain the low logic state, and the maximum value of $C_{DS}$ has to be high compared to $C_{o}$ to achieve the high logic level.

2.5. Modeling the CAL devices

2.5.1. Modeling the input capacitance variation

Various models can be found in the literature to model capacitances and their fringe fields. In this work, we use the Mejis-Fokkema formula [22] for the comb-drive $C_{g}$ and the Palmer formula [24] for the gap-closing capacitances $C_{DS}$ and $C_{SM}$.

For $C_{g}$ (Eq. (9)), the first term $C_{l}$ represents the lateral capacitance without fringe effect, $C_{f}$ estimates the fringe capacitance and $C_{s}$ is the capacitance at the tip of fingers (c.f. Fig. 2c):

$$C_{g} = 2C_{l} + C_{f} + C_{s}$$  \hspace{1cm} (9)

$$C_{g} = \frac{2n_{f}c\eta_{f}(l_{f} + x)}{d_{f}} + 2n_{f}c\eta_{f} \left[ 0.77 + 1.06 \left( \frac{l_{f} + x}{d_{f}} \right)^{1/4} + 1.06 \left( \frac{h_{f}}{d_{f}} \right)^{1/2} \right]$$  \hspace{1cm} (10)

where $n_{f}$ and $h_{f}$ represents the comb’s finger numbers and their thickness respectively. $l_{f}$, $d_{f}$, $l_{g}$ and $t_{f}$ are the initial overlapping distance between the fingers, the initial gap distance between the fixed and movable fingers, the length and width of the finger respectively. $\varepsilon$ is the air permittivity and $x$ is the displacement in the $X'$ direction. This
model is in good agreement with the commercial software MEMS+ from Coventor ware (cf Fig. S2)

2.5.2. Modeling the output capacitance variation

The gap-closing capacitance $C_{DS}$ is given by the Palmer formula [24], (Eq.(11)) and (Eq.(12)) for PVC and NVC respectively:

$$C_{DS_{PVC}} = \frac{n_s h_s L_s \varepsilon}{d_{\text{max}} - x} \left[ 1 + 2 \left( \frac{d_{\text{max}} - x}{h_s \pi} \right) \left( 1 + \log \left( \frac{h_s \pi}{d_{\text{max}} - x} \right) \right) \right]$$  \hspace{1cm} (11)

$$C_{DS_{NVC}} = \frac{n_s h_s L_s \varepsilon}{d_{\text{min}} + x} \left[ 1 + 2 \left( \frac{d_{\text{min}} + x}{h_s \pi} \right) \left( 1 + \log \left( \frac{h_s \pi}{d_{\text{max}} + x} \right) \right) \right]$$  \hspace{1cm} (12)

The expression of $C_{SM}$ is similar to the expression of $C_{DS}$ in PVC, and is expressed by:

$$C_{SM} = C_{DS_{PVC}} = \frac{n_s h_s L_s \varepsilon}{d_{\text{max}} - x} \left[ 1 + 2 \left( \frac{d_{\text{max}} - x}{h_s \pi} \right) \left( 1 + \log \left( \frac{h_s \pi}{d_{\text{max}} - x} \right) \right) \right]$$  \hspace{1cm} (13)

where $n_s$, $h_s$, $L_s$, $d_{\text{max}}$ or $d_{\text{min}}$ are the number of $C_{DS}$ electrodes, their thickness, their length and their initial gap distance respectively.

2.5.3. Modeling the device dynamics

From the Newton’s second law, the dynamic behavior of the PVC and NVC structures is represented by the non-dimensional equation (Eq. (14)). The first term is associated to the kinetic force, the second term is associated to the mechanical damping force, the third one is related to the spring force, the fourth one represents the electrical force from $C_g$ and the next one is the electrical force from $C_{DS}$. The last term represents the electrical force associated to $C_{SM}$ for the NVC structure. The non-dimensional variables used in (Eq.(14)) are given in Table 1.

$$\ddot{x} + \lambda \dot{x} + x - (V_{in})^2 \left( 1 + \frac{1}{(\beta_0 - x)^3} + \frac{y}{(\beta_0 + x)^{\gamma\sigma}} \right) + \alpha (\dot{V}_{in})^2 \left( 1 + \beta_0 (\beta_0 + x) \right) = 0$$  \hspace{1cm} (14)

where $\gamma = 0.265$, $\beta_0 = \frac{2\pi}{h_s}$, $\alpha = \frac{n_s h_s L_s}{2nh_s \pi}$, $\alpha_1 = -1$ and $\alpha_2 = 0$, for PVC configuration and $\alpha_1 = \alpha_2 = 1$ for NVC.

2.5.4. Modeling the impact

At each impact between the drain and the source electrodes, the

![Fig. 3. Different states of the buffer (PVC) and the inverter (NVC). a) Buffer in the OFF state. b) Buffer in the ON state during the Hold phase. c) Inverter without $M$ in OFF state. d) Inverter without $M$ in the ON state during the Hold phase. e) Inverter with $M$ in OFF state. f) Inverter with $M$ in the ON state during the Hold phase.](image)

![Fig. 4. Equivalent circuit of a) a CAL buffer, and b) a CAL inverter.](image)
Table 1
Non-dimensional variables.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\dot{x}$</td>
<td>Displacement in the direction $\mathbb{T}$</td>
</tr>
<tr>
<td>$t$</td>
<td>Time</td>
</tr>
<tr>
<td>$\dot{e}$</td>
<td>Damping</td>
</tr>
<tr>
<td>$\beta_i$</td>
<td>Gap of the side capacitance $C_s$</td>
</tr>
<tr>
<td>$\beta_{i\bar{E}}$</td>
<td>Overlapping distance between fingers</td>
</tr>
<tr>
<td>$\beta_{i\bar{D}}$</td>
<td>Initial gap of PVC $C_{DS}$</td>
</tr>
<tr>
<td>$\beta_{i\bar{H}}$</td>
<td>Initial gap of NVC $C_{dH}$</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Input signal, where $\mu = \frac{m_0 \omega^2}{\sqrt{K_{nH}}}$</td>
</tr>
<tr>
<td>$V_{PC}$</td>
<td>Power Clock signal</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Signal across the output capacitance $C_{DS}$</td>
</tr>
<tr>
<td>$V_{VPC}$</td>
<td>Maximal supply voltage of different signal</td>
</tr>
<tr>
<td>$E_{in}$</td>
<td>Mechanical energy where $z_i = \kappa d_i^2$</td>
</tr>
<tr>
<td>$E_{in}$</td>
<td>Input energy produced by the input source where</td>
</tr>
<tr>
<td>$E_{el}$</td>
<td>Electrical energy stored in the input capacitance $C_e$</td>
</tr>
<tr>
<td>$E_{el}$</td>
<td>Electrical input energy produced by the Power clock</td>
</tr>
<tr>
<td>$E_{el}$</td>
<td>Electric energy stored in $C_{DS}$ and $C_o$</td>
</tr>
<tr>
<td>$C_{el} = C_{el}^{-}$</td>
<td>Output capacitance</td>
</tr>
<tr>
<td>$C_{el} = C_{el}^{+}$</td>
<td>Input capacitance</td>
</tr>
<tr>
<td>$C_{el} = C_{el}^{+} - C_{el}^{-}$</td>
<td>Output capacitance</td>
</tr>
</tbody>
</table>

Table 2
Physical and geometric parameters used in simulations.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E$</td>
<td>Young’s modulus of silicon (N/m$^2$)</td>
<td>$169 \times 10^9$</td>
</tr>
<tr>
<td>$\epsilon$</td>
<td>Permittivity of air (F/m$^3$)</td>
<td>$8.854 \times 10^{-12}$</td>
</tr>
<tr>
<td>$L_e$</td>
<td>Length of the gap closing capacitance $C_{dH}$ (µm)</td>
<td>8.72</td>
</tr>
<tr>
<td>$h_0$</td>
<td>Thickness of the gap closing capacitance $C_{dH}$ (µm)</td>
<td>0.4</td>
</tr>
<tr>
<td>$h_1$</td>
<td>Thickness of the comb-drive capacitance $C_{DS}$ (µm)</td>
<td>0.4</td>
</tr>
<tr>
<td>$d_{in}$</td>
<td>Initial gap distance of $C_{dH}$ (µm)</td>
<td>0.25</td>
</tr>
<tr>
<td>$d_{in}$</td>
<td>Thickness of the dielectric (µm)</td>
<td>0.01</td>
</tr>
<tr>
<td>$n_e$</td>
<td>Number of the gap-closing capacitance $C_{dH}$</td>
<td>1</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Number of finger in $C_{DS}$</td>
<td>55</td>
</tr>
<tr>
<td>$l_f$</td>
<td>Length of the mechanical suspension (µm)</td>
<td>5</td>
</tr>
<tr>
<td>$h$</td>
<td>Thickness of the mechanical suspension (µm)</td>
<td>0.02</td>
</tr>
<tr>
<td>$L_f$</td>
<td>Length of the comb-drive capacitance $C_{DS}$ (µm)</td>
<td>8.8</td>
</tr>
<tr>
<td>$d_{f}$</td>
<td>Gap distance of the comb-drive capacitance $C_{DS}$ (µm)</td>
<td>0.04</td>
</tr>
<tr>
<td>$l_f$</td>
<td>Width of the finger of the comb-drive capacitance $C_{DS}$ (µm)</td>
<td>0.04</td>
</tr>
<tr>
<td>$l_f$</td>
<td>Overlapping distance between fingers of $C_{DS}$ (µm)</td>
<td>0.02</td>
</tr>
<tr>
<td>$l_f$</td>
<td>Length of the finger of the comb-drive capacitance $C_{DS}$ (µm)</td>
<td>0.4</td>
</tr>
<tr>
<td>$m$</td>
<td>Effective mass of the movable part (Kg)</td>
<td>$1.98 \times 10^{-14}$</td>
</tr>
<tr>
<td>$K_s$</td>
<td>Spring constant in the direction $\mathbb{T}$ (N/m)</td>
<td>0.02</td>
</tr>
<tr>
<td>$c$</td>
<td>Damping (Kg/s)</td>
<td>$1.96 \times 10^{-8}$</td>
</tr>
<tr>
<td>$C_L$</td>
<td>Load capacitance (F)</td>
<td>1</td>
</tr>
</tbody>
</table>

mobile electrode loses a small part of its kinetic energy during a bouncing phenomenon. During successive contacts, the velocity can be expressed as [25,26]:

$$\dot{x}_n = -K_{B NST} \frac{\dot{x}_n}{x_{n-1}}$$

where $\dot{x}_{n-1}$ and $\dot{x}_n$ are the velocities before and after the $n^{th}$ impact, and $K_{B NST}$ is the coefficient of restitution. When the mobile electrode reaches the contact, its velocity is set according to (Eq.(15)). The characteristics of the bounces depend on the mass of the mobile part and its velocity, the elastic response of the material and the surface hardness [26].

3. Simulations and analysis

In this section, we present and analyze the simulations of Capacitive Adiabatic Logic circuits using the MEMS devices presented previously. The physical and geometrical features of the proposed implementations are given in Table 2. These dimensions are carefully chosen in order to match the FET transistor parameters. First, we present how a buffer or an inverter works. Then we study the energy transfer and losses in a buffer gate. Finally, we demonstrate the possibility to cascade in series several buffers or inverters.

In the following, a “1” adiabatic logic input (i.e. the “ON state”) corresponds to a 4-interval pulse similar to $V_{PC}$, but with a phase shift of a quarter of period in order to satisfy the adiabatic logic conditions. A “0” (“OFF state”) means $V_{in} = 0$ during the entire sequence (Fig. 1d).

4. Analysis of a single gate

4.1. Simulation of a buffer

In order to understand how a CAL buffer works, we plotted in Fig. 5b the output voltage of a PVC and the displacement of its mobile part for the input logic sequence “1 0” shown in Fig. 5a. $C_o$ is set to 1 fF according to [1]. During the “1” state, as soon as $V_{in}$ increases (Wait interval), the comb-drive at the input moves the mobile part, $d_i = d_{in} + x$ decreases and $C_{DS}$ increases from its minimum to its maximum value, with a short oscillation induced by the impact of the mobile mass onto the rigid frame. Then, during the Evaluate interval, $V_{in}$ and $C_{DS}$ are constant, while $V_{PC}$ increases. $C_{DS}$ is at its maximum value and $V_{out}$ follows $V_{PC}$ through the constant capacitive divider formed by the $C_{DS}$ capacitance. This lasts even beyond the Hold interval, while $V_{in}$ decreases till 0V, because of the electrostatic force $F_e$ across $C_{DS}$ introduced by $V_{PC}$ is still higher than the restoring force of the mechanical springs $F_m$. This memory effect corresponding to the hysteresis of electrostatic transducers [23] is important to keep $C_{DS}$ at its maximum value, allowing $V_{out}$ to follow the PC. During the Recovery interval, $V_{out}$ progressively decreases with $V_{PC}$, and at some point the electrostatic force associated to $C_{DS}$ is not sufficient to compensate the restoring spring force, so $C_{DS}$ rapidly decreases to its minimum value, bringing $V_{out}$ definitely to 0 V.

Then the “0” state starts. $V_{in}$ remains equal to 0 during the 4 intervals of $V_{PC}$ and the electrostatic force across $C_o$ is null. However, when $V_{PC}$ increases during the Evaluate interval, its associated electrostatic force leads to a small variation of $V_{in}$ and at some point the electrostatic force associated to $C_{DS}$ is not sufficient to compensate the restoring spring force, so $C_{DS}$ rapidly decreases to its minimum value, bringing $V_{out}$ definitely to 0 V.

4.1.1. Simulation of an inverter

Similarly, the time history of a NVC loaded with a capacitor $C_o$ of 1 fF is given in Fig. 5c and d for the same “1 0” logic input. At $t = 0$, $C_{DS}$ is at its maximum and $V_{in}$ starts to increase from 0 V to $V_{PC}$ (Wait interval). $V_{out}$ is initially equal to 0 V, so the mobile electrode easily moves with the increase of $V_{in}$ and $C_{DS}$ quickly decreases to its minimum value. During the Evaluate interval, $V_{in}$ and so $C_{DS}$ remain constant. Since $V_{PC}$ increases and $C_{DS}$ is not negligible, $V_{out}$ follows $V_{PC}$ but has to remain below the maximum voltage allowed for a “0” logic level. During the following Hold interval, $V_{in}$ decreases. First $C_{DS}$ remains at its minimum because the electrostatic force across $C_o$ is still higher that the spring restoring force. However, at some point, this is not the case anymore. Then $C_{DS}$ increases, while $V_{PC}$ is still high, which leads to an unexpected increase of $V_{out}$ before the next “0” logic at the input (case 1 Fig. 5e). To avoid this, we added the M electrode connected to the ground that creates an additional electrostatic force across $C_{DS}$, controlled by $V_{PC}$ and opposed to the spring force (Fig. 3e,f). Hence, $C_{DS}$ can be maintained at its minimum value during the whole Hold interval (case 2 Fig. 5d).

Close to the end of the Recover interval, while $V_{PC}$ is small enough, the mobile part progressively moves back to its initial position. Simultaneously $C_{DS}$ progressively gets back to its maximum value, which is reached at the beginning of the Wait interval. Hence $V_{out}$ is
always bellow the “1” logic state before the end of the “1” sequence at the input.

4.2. Energy analysis

In this section, we investigate the energy balance of the design and we show that only a small part of the energy provided by the electrical sources cannot be recovered.

\( C_g \) and \( C_{DS} \) are two electromechanically coupled transducers having two electrical inputs and one mechanical output (Fig. 6a). The instantaneous electrical energy is given by:

\[
\mathcal{E}_e(t) = \int (V_{in}i_{in} + V_{PC}i_{PC})dt
\]

(16)

The instantaneous mechanical energy output of the system is given by:

\[
\mathcal{E}_m(t) = \int f(t)\dot{x}(t)dt
\]

(17)

where \( f(t) \) is the mechanical force applied on the mobile part and \( \dot{x}(t) \) is its velocity. The expression of \( i_{in} \) and \( i_{PC} \) are given by:

\[
i_{in} = \int \frac{d(C_gV_{in})}{dt} = C_g\frac{dV_{in}}{dx} \frac{dx}{dt} + \frac{dC_g}{dx}V_{in}\dot{x}(t),
\]

(18)

\[
i_{PC} = \int \frac{d(C_{DS}V_{DS})}{dt} = C_{DS}\frac{dV_{DS}}{dx} \frac{dx}{dt} + \frac{dC_{DS}}{dx}V_{DS}\dot{x}(t) = \frac{dV_{out}}{dt}
\]

(19)

Combining equations (Eq. 10), (Eq. 12) and (Eq. 13), the expression of \( E_e(t) \) becomes:

\[
E_e(t) = \frac{C_g}{2}V_{in}^2 + \frac{C_{DS}}{2}V_{DS}^2 + \frac{C_{in}}{2}V_{out}^2 + \int \left( \frac{dC_g}{dx}V_{in}^2 + \frac{dC_{DS}}{dx}V_{DS}^2 \right)\dot{x}(t)dt
\]

(20)

The first three terms of (Eq. 20) represent the electrostatic energy stored in the capacitances \( C_g \), \( C_{in} \) and \( C_{DS} \) respectively. The last term \( E_m \) represents the mechanical energy. In other words, the electrical energy supplying a capacitive transducer is converted in two parts, the electrostatic energy stored in the variable capacitance and the output mechanical energy [27,28].

Fig. 5. Operation of simple gates for a “1 0” logic input. a) the input and PC signals. b) Simulation of a CAL buffer. c) Simulation of a CAL inverter without electrode \( M \) (case 1) and d) with electrode \( M \) (case 2). All dimensions are given in Table 1.
We have investigated the energy conversion and losses in the CAL buffer shown in Fig. 4a, and loaded by a logical sequence $V_{in}$ (101) (Fig. 6b). The variations of $C_{DS}$ and $C_{g}$, the non-dimensional values of $C_{DS}$ and $C_{g}$ (see Table 1) are shown in Fig. 6c. During the Wait interval, $V_{in}$ increases and a large part of the electrical input energy $E_{in}$ is stored in $C_{g}$ (we call it $E_{Cg}$). The rest is converted into the mechanical energy $E_{m}$; part of it is stored in the mechanical springs that moves the body, leading to an increase of $C_{g}$ and $C_{DS}$ until they reach their maximum values. The remaining energy is converted into kinetic energy and part of it is lost during the impact between the drain and the source electrodes (see the oscillations of $C_{DS}$ and $C_{g}$ in Fig. 6c). During the Evaluate interval, $V_{PC}$ increases, generating an electrical input energy $E_{PC}$. However $C_{g}$ and $C_{DS}$ remain maximum and there is no electromechanical energy conversion: all the electrical energy $E_{PC}$ is stored in $C_{DS}$ and $C_{g}$.

During the Hold interval, $V_{in}$ decreases but the capacitances $C_{DS}$ and $C_{g}$ do not change, as explained previously: only $E_{Cg}$ is recovered by $V_{in}$. During the Recovery interval, both electrical energies stored in $C_{DS}$ and $C_{g}$ are recovered by $V_{PC}$, and $C_{DS}$ remains constant for a while.

The electrical energy necessary to supply the buffer is not fully recovered: some energy is dissipated by damping losses and during the impact. Fig. 6d shows the evaluation of the non-dimensional electric energy $E_{in}$ produced by the source $V_{in}$, the energy $E_{Cg}$ stored in $C_{g}$, the energy $E_{PC}$ produced by the source $V_{PC}$ and the energy $(E_{Cg} + E_{PC})$ stored in both capacitances $C_{DS}$ and $C_{g}$. During one cycle, with the dimension in Table 2 corresponding to a realistic device of 25 $\mu$m², the
dissipated energy is equal to 0.9 J. However, most of the input energy \( (E_{\text{in}} + E_{\text{r}}) \) is recovered: the ratio between the recovered and the input energy is 89%.

### 4.3. Cascability

Now we consider the circuit composed of four cascaded CAL buffers and inverters. The buffer and inverter chain circuits are presented in Fig. 7a,d respectively. Each gate is supplied by a PC, and the subsequent PCs are delayed by a quarter of period in order to satisfy the adiabatic conditions. The dynamic behavior of the cascaded buffers and inverters is given by the following non-dimensional equation:

\[
\dot{x}_1 + \lambda \dot{x}_1 + x_1 - \dot{V}_{\text{in}} i \left[ \frac{1}{(\beta_1 - \dot{x}_1)^2} + \frac{1}{(\beta_2 + \dot{x}_1)^2} \right] = 0
\]

\[
\alpha_1 \dot{V}_{\text{DS},1} \left[ \frac{1}{(\beta_1 + \dot{x}_1)^2} \right] - \alpha_2 \dot{V}_{\text{PC},1} \left[ \frac{1}{(\beta_2 - \dot{x}_1)^2} \right]
\]

(21)

where \( i \) refers to the position of the gate in the chain, \( \alpha_1 = -1 \) and \( \alpha_0 = 0 \), for PVC configuration and \( \alpha_1 = \alpha_2 = 1 \) for NVC and:

\[
\dot{V}_{\text{in},i} = \frac{V_{\text{PC},i-1} C_{\text{DS},i-1} + C_{\text{E},i} + C_{\text{g},i}}{C_{\text{DS},i-1} + C_{\text{E},i} + C_{\text{g},i}}.
\]

\[
\dot{V}_{\text{DS},i} = V_{\text{PC},i}(C_{\text{E},i+1} + C_{\text{g},i})/(C_{\text{DS},i} + C_{\text{E},i+1} + C_{\text{g},i}).
\]

We studied the dynamical response of the cascaded elements to an input logic sequence \( V_{\text{in}} \) (1011). Fig. 7b,e depict the dynamic output of the first gate for the buffer and inverter series. The logic state at the 4th gate for the buffer and inverter series are shown in Fig. 7c,f respectively. The high (1) level corresponds to 77% of the PC’s maximum voltage (equal to 1.38 V) for both buffers and inverters chains, and the low (0) level corresponds to 23% and 20% of the PC for the buffers and the inverters chains respectively.

### 5. Conclusion

We have presented novel four-terminal variable capacitors (FTVC) based on silicon nano/micro technologies that can be used in Capacitive Adiabatic Logic. The FTVC intends to replace the field effect transistor (FET) in adiabatic logic in order to drastically reduce the energy consumption by avoiding the static losses and the non-adiabatic dissipation in classical CMOS circuits. It is a better alternative than nanorelays, also envisaged in adiabatic logic using electromechanical devices, because of the absence of resistive contact.

The electromechanical simulations demonstrated that with only two types of FTVC, it is possible to implement basic adiabatic logic functions as inverters and buffers. We also demonstrated for the first time the cascadability of both class of devices. During one cycle, a buffer gate of \( 10 \times 2.5 \mu m^2 \), dissipated 0.9 J, which is in the same order of the energy dissipated by nano-scale FET transistors. However, it scales in the cube of the size. Gaining one order of magnitude in volume will allow to beat the dissipation of the state of the art of CMOS circuits: the simulations shows that a buffer gate of \( 1 \times 0.25 \mu m^2 \) would dissipate 0.7 aJ. The simulations presented in this paper are performed with dimensions of devices that can be fabricated with classical MEMS and IC technologies. The characteristic dimension is 40 nm for both structures and gaps, and is still possible to achieve using photolithography as in last generations of IC technologies. In addition, there is much less steps in the fabrication process that for ICs and it does not require any expensive material. Reducing even more the dimensions will need the use of e-beam lithography, which is currently still quite expensive because of the longer time required for this step. Etching gaps in silicon at the nanometer scale would be also a challenge. However, reducing the size of the etching areas is very favorable to Deep Reactive Ion Etching of silicon because of an increase of the etching aspect-ratio (AR) with small dimensions: for instance in [29], Parasuraman et al have performed an AR of 125 for a gap of 35 nm.

When adiabatic conditions are satisfied, most of the provided energy (89%) is recovered after one cycle. This is a bit less than the non-contact device we have presented in [19]. However, the logic state differentiation has been dramatically improved from a few percents to more than 50%. This is a considerable advantage for a practical implementation.
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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.nanoen.2018.10.059

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