Contact-Free MEMS Devices for Reliable and Low-Power Logic Operations

Y. Perrin, A. Galisultanov, L. Hutin, *Member, IEEE*, P. Basset, H. Fanet, and G. Pillonnet, *Senior Member, IEEE*

***Abstract*— We report the first experimental proof of concept of a new electromechanical adiabatic logic family operating without any kind of electrical and mechanical contacts. Based on comb-drive actuators and standard microelectromechanical system (MEMS) microfabrication, we demonstrate the cascadability of logic gates up to 170 °C, and operation in the kilohertz-range under a power supply of 4.5 V. Assuming that state-of-the-art microfabrication can downscale our MEMS gates by a factor of 100, we expect a dissipation of 0.1 aJ/op (24 k_BT) at 250 kHz at 45 mV. This study paves the way toward new reliable low-power electromechanical digital circuits.**

***Index Terms*— Adiabatic logic, Landauer switches, microelectromechanical system (MEMS).**

I. Introduction

THE inherent subthreshold slope of conventional field-effect transistors (60 mV/d at 300 K) sets the minimum amount of energy dissipated during a single logic operation. For state-of-the-art nanoscale devices, this limit is about 1000's k_BT (1's aJ/op) and remains orders of magnitude above Landauer's limit [1]. Since the 1990s, unconventional logic families or transistor outsiders have been introduced to overcome the minimal power consumption of conventional architectures. Table I compares different implementations of conventional and adiabatic architectures.

By trading the constant power supply V_{DD} for a variable and reversible power supply, adiabatic logic reduces charging losses and recycles the energy invested to code the logic state. Although various transistor-based adiabatic schemes have been proposed, the tradeoff between leakage and dynamic losses inherent to solid-state transistors has restrained these efforts [2]. According to the principle of adiabatic clocking, if the power supply is trapezoidal and recovers the energy back after each cycle, the dissipation should scale with the ramping time T. But the FET implementation of adiabatic logic gates leads to a fixed residual loss due to FET hysteresis behavior and the significant leakage contribution at the operating temperature.

To overcome these limitations in conventional or adiabatic logic clocking, low-power architectures must take advantage of microelectromechanical system (MEMS) relays that received growing interest over the last two decades, as they do not suffer from static power loss [3]. Substantial improvements in terms of dynamic power consumption have been recently reported, such as steep effective subthreshold slope driving voltage in the sub-100 mV range [4], [5]. However, they show poor reliability inherent to mechanical and electrical contacts, which are destructive at the microscale. Recent MEMS switches can handle millions of cycles [6], which is not enough to operate a MEMS-based general-purpose processor longer than a few minutes.

To increase the reliability of MEMS switches, we recently proposed to use them in contact-free operation [7]–[9]: instead of opening or closing an air gap, "contact-free switches" stay open and act as a variable capacitor. By modulating a capacitance divider rather than a resistance divider for conventional switches (Table I), the output logic state is given by the inputs states through a variable ac-coupling between the power supply and the output. This energy-reversible ac supply, also called power-clock, allows us to determine the dynamic logic state value using the modulation of the capacitive contrast. Like in dynamic logic, [7]–[9] exploits the temporary storage of information in capacitances. But, the capacitive coupling (and thus the logic states differentiation) is affected by the parasitic capacitance of gate-to-gate connections. To overcome this limitation, we introduced contact-free Electromechanical Adiabatic Computing (EMAC) in [10], where logic states are processed and propagated mechanically. By coding the logic state in the MEMS position, the parasitic capacitance is no longer an issue. EMAC shows a reversible displacement, thus suppressing the fixed residual term in energy consumption compared to others logic families summarized in Table I.

Manuscript received January 11, 2021; revised March 5, 2021 and March 29, 2021; accepted March 30, 2021. Date of publication April 16, 2021; date of current version May 21, 2021. The review of this article was arranged by Editor C. Yang. *(Corresponding author: G. Pillonnet.)*

Y. Perrin was with CEA-LETI, 38000 Grenoble, France. He is now with Seagate Technology, Londonderry BT48 0BF, U.K. (e-mail: yann.perrin@mailoo.org).

A. Galisultanov was with CEA-LETI, 38000 Grenoble, France. He is now with eLichens, 38000 Grenoble, France (e-mail: galisultanov@gmail.com).

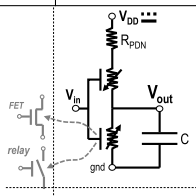
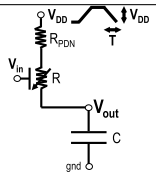
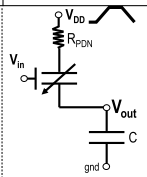
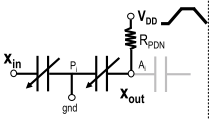
L. Hutin, H. Fanet, and G. Pillonnet are with CEA-LETI, 38000 Grenoble, France (e-mail: louis.hutin@cea.fr; herve.fanet@cea.fr; gael.pillonnet@cea.fr).

P. Basset is with ESYCOM, CNRS, CNAM, ESIEE Paris, Université Gustave Eiffel, 77454 Marne-la-Vallée, France (e-mail: philippe.basset@esiee.fr).

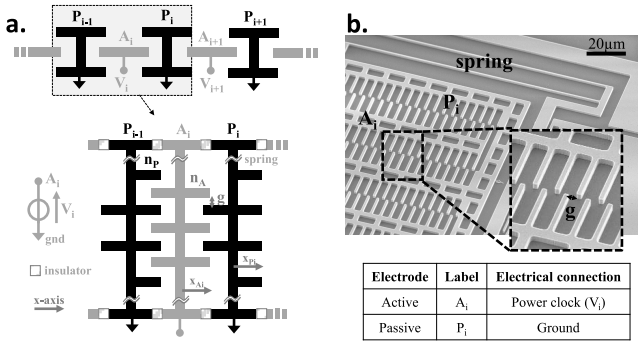
Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3070844.

Digital Object Identifier 10.1109/TED.2021.3070844

TABLE I
CONTACT-FREE OPERATIONS AND ADIABATIC COMPATIBILITY OF SOME SELECTED LOGIC FAMILIES

	Resistive-based logic	Adiabatic resistive-based logic	Contact-free logics	
Reference	[4,5,6]	[11,12]	CAL [7,8,9]	EMAC [10]
Electrical contact	Y	Y	N	N
Mechanical contact*	Y	Y	Y	**N**
Devices	FET or relay	FET or relay	variable capacitor	comb drive
Logic state coding nature	charge	charge	charge	position
Adiabatic-compatible**	N	**Y*****	**Y**	**Y**
Leakage	Y*	Y*	**N**	**N**
Sensible to capacitive interconnects	Y	Y	Y	**N**
				
Energy dissipation	$E_{op} \sim CV_{DD}^2 + I_{leak} V_{DD} T_{op}$	$E_{op} \sim \frac{(R + R_{PDN})C}{T} CV_{DD}^2 + 4TI_{leak}V_{DD}$	$E_{op} \sim \frac{R_{PDN} C_o}{T} CV_{DD}^2 + E_{mecha}$	$E_{op} \sim \frac{R_{PDN} C_o}{T} CV_{DD}^2 + E_{mecha}(\frac{1}{T})$

** If FET are used*
*** energy dissipation scales when lowering the operation frequency*
**** limited by the hysteresis of relays or V_{TH} of FET*



Electrode	Label	Electrical connection
Active	A_i	Power clock (V_i)
Passive	P_i	Ground

Fig. 1. (a) Elementary contactless devices (CDSs) used in electromechanical adiabatic computing. (b) Micrograph of a CDS.

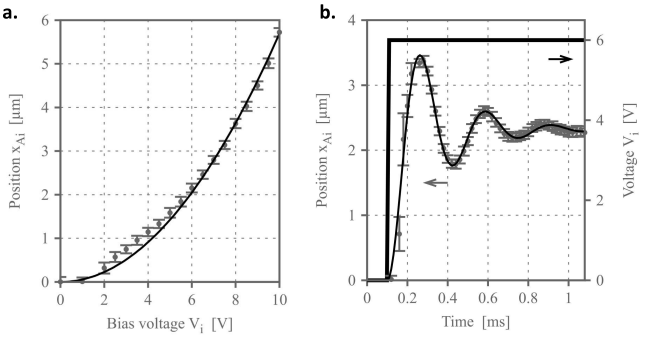


Fig. 2. (a) Equilibrium positions versus dc bias V_i ($g = 1.16$ μm, $n = 68$, $k = 0.1$ N/m). Measured (dot), fitted to αV_2 (line). (b) Stroboscopic measurement of the response of the input actuator to a step voltage function.

This article shows the fabrication and operation of elementary devices, then the design of electromechanical logic gates and their integration inside a pipeline. As an extension of [10], we report the first experimental proof of concept of EMAC, implemented with reliable elementary devices, i.e., comb-drive actuators made from a standard fabrication process. We also show that we propagate series of logic states through a pipeline with no attenuation. Since the EMAC family is based on electrostatic and mechanical couplings, it is not affected by the usual limitations of semiconductor-based electronics. Thus, EMAC is suitable for operating under high temperatures or radiation exposure. Our EMAC pipeline has operated up to 170 °C, which was the maximum temperature we could reach with our experimental setup.

II. CONTACT-FREE MEMS DEVICE

Fig. 1(a) depicts a simplified view of an elementary device in EMAC. Each comb-drive structure (CDS) consists of one active (A_i) and one passive (P_i) electrodes allowed to move along the x-axis with a stiffness k. Active and passive electrodes are connected to the power-clock V_i and the ground, respectively. They are electrostatically coupled by n interdigitated fingers separated by an air gap g. Comb-drive actuators have strong assets for implementing EMAC.

1) Displacement in the micrometer range by applying only a few volts between the electrodes (and by taking advantage of low-stiffness spring designs).
2) Already proven reliable operation by avoiding any mechanical contact.
3) Stable and hysteresis-free position-versus-voltage curve, allowing physically reversible operation [12], [13].
4) Relatively simple fabrication process (cf., Section V).

Fig. 1(b) shows a scanning electron micrograph of a CDS after fabrication, with $g = 1.16$ μm and $n = 68$. From the geometry of the springs (folded beams, 0.9 μm wide, 1.75 μm thick, and 165 μm long), the stiffness k is about 0.1 N $\cdot$ m $-$ 1. Fig. 2(a) shows the quasistatic electrode motion along the x-axis x_{Ai} versus V_i biasing. The experimental curve has a parabolic shape in accordance with the elementary model of the comb-drive actuator ($x = aV^2$, with $a = 0.057$ μm $\cdot$ V^{-2} for our device). These data were gathered with the same experimental setup as for the gate pipeline shown later (Section IV).

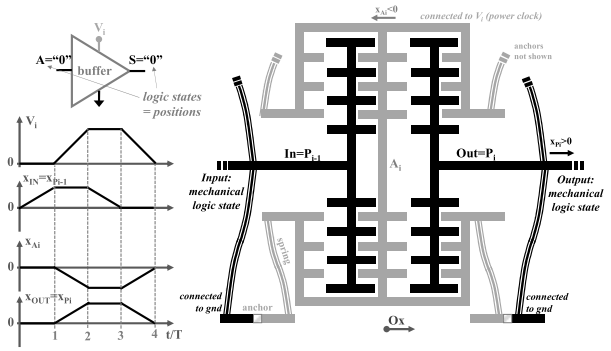


Fig. 3. Buffer logic gate in EMAC when the input logic state is "low."

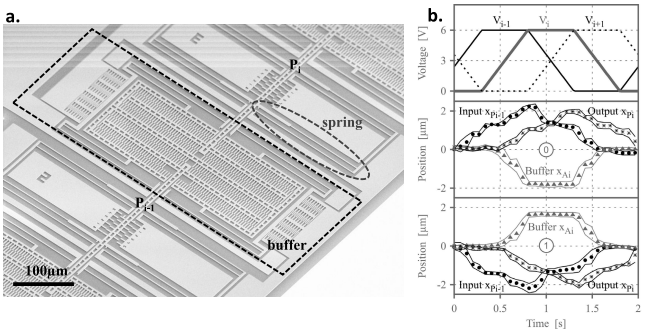


Fig. 4. (a) SEM picture of an EMAC buffer gate within a pipeline. (b) Measured positions of three electrodes in a buffer gate when the input logic state is "0" or "1."

To characterize the dynamical properties of an electrode, we measured its response to a voltage step V_i [Fig. 2(b)]. Fitting the dynamic response with an elementary damped mass-spring system leads to a Q-factor of 2.3 and a resonance frequency of about 3.16 kHz.

III. Single Buffer Logic Gate

The CDS design must be tailored for adiabatic logic gates because stray field effects may lead to a significant electrostatic force between electrodes, even when they are pulled apart [10]. This problem, which was challenging for the design of logic gates, was solved by adding a complementary electrode to the actuators, as shown on the buffer gate in Fig. 3. This gate is composed of 1) an input electrode P_i; 2) a central electrode A_i; and 3) an output electrode P_{i+1}. Electrodes P_i and P_{i+1} are electrically grounded, whereas A_i is connected to the trapezoidal-shaped power-clock V_i. The reference of position x is the OFF-state, where no voltage is applied to the circuit. A picture of fabricated devices is shown in Fig. 3(a), which will be scaled down in the future by using thinner lithography processes.

In an EMAC buffer, bits are processed in the following way:

Logic State "0" (Fig. 3): At $t = T$, the input electrode P_i is slightly pushed toward the right ($x_{Pi} > 0$) by the previous gate and the buffer is ready to evaluate the bit. The clock voltage V_i rises, and electrostatic forces appear between P_i and A_i. Because the displacement x_{Pi} breaks the symmetry of the actuator, the electrode A_i is attracted toward the left. At $t = 2$ T, V_i and $x_{Ai} < 0$ are maximum, the bit is stored in the buffer. As the displacement of A_i breaks the symmetry of the output actuator, the output electrode P_{i+1} is fully attracted toward the right ($x_{Pi} + 1 > 0$). The output can then be evaluated by the next logic gate where V_{i+1} is shifted by T.

Logic State "1": The situation is the opposite as for the logic state "0." At $t =$ T, the input electrode P_i is pushed toward the left ($x_{Pi} < 0$). Thus, when the clock voltage V_i rises, the electrode A_i is attracted to the right. At $t = 2$ T, $x_{Ai} > 0$ so the output electrode P_{i+1} is attracted toward the left ($x_{Pi+1} < 0$).

Fig. 4(b) shows how bits "0" and "1" are processed experimentally in the buffer gate pictured in Fig. 4(a), when included in a buffer pipeline (see Section IV). As explained earlier, a "0" logic state is encoded when x_P is positive compared to the steady-state position. When the output is equal to "0," the buffer gate (A_i) is moved backward ($x_{Ai} < 0$). With a peak-to-peak clock voltage of 6 V, amplitudes of motion for electrodes P_i, A_i, and P_{i+1} are $x_{Pi} = \pm 1.2$ μm, $x_{Ai} = \pm 2$ μm, and $xP_{i+1} = \pm 1.2$ μm, respectively.

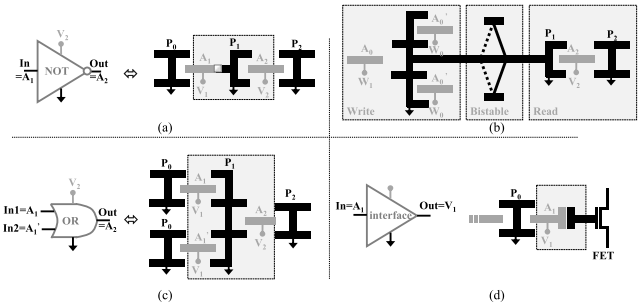


Fig. 5. Other logic gates in EMAC and interface with standard computation. (a) NOT logic gate. (b) Nonvolatile latch. (c) OR logic gate. (d) EMAC-to-classical logic interface.

Although this experimental study is focused on buffer gates only, EMAC can be extended to any combinatorial and sequential logic gates to implement a general-purpose processor. Reversible gates such as the Fredking gate [14] could also be envisaged. Possible designs for combination logic such as NAND and XOR gates are given in Fig. 5.

OR *Gate:* The OR gate [cf., Fig. 5(c)] combines two mechanically encoded logic inputs. If one or two inputs have the state "1," P_i will be attracted to the left and break the symmetry as in the buffer gate. The spring design must be optimized to prevent the gate from twisting due to the asymmetric applied forces and constrain the displacement along the x-axis.

RS Latch: Making an reset set (RS) latch [cf., Fig. 5(b)] for EMAC requires a hysteretic element such as a nonvolatile bistable beam. The writing terminal moves the moving part P_i in one of two stable positions. The latched logic state can be read by the reading terminal A_2. When V_2 increases, the position of A_2 will be determined by the state of P_i.

Interface: If EMAC is envisaged as a low-power logic unit inside a conventional digital circuit, position-encoded logic states can be converted to charge-encoded states by the device in Fig. 5(d). The variable capacitor formed by A_1 and the gate

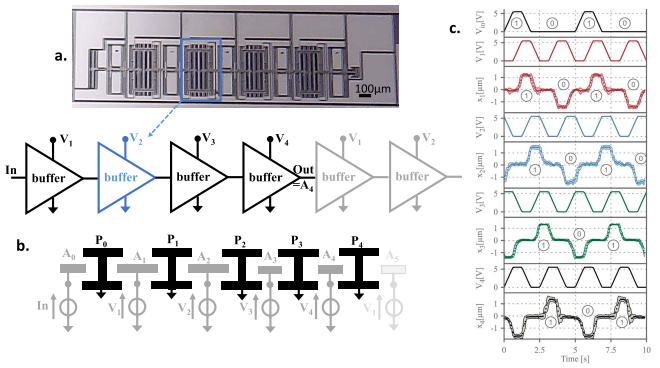


Fig. 6. (a) Optical picture of the whole pipeline composed of four cascaded buffer gates. (b) Schematic of the measured buffer chain. (c) Optical measured A_i position of each gate versus time, demonstrating the logic cascadability without attenuation through the gates.

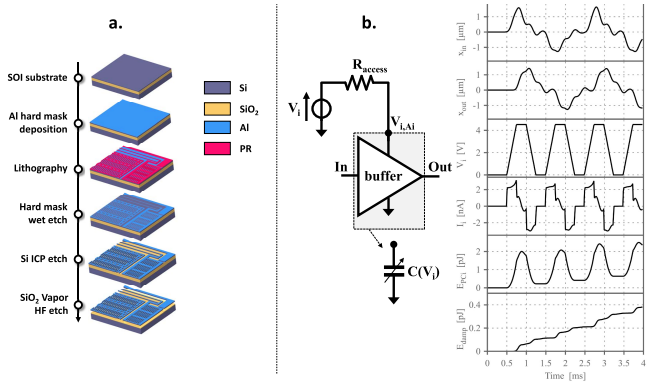


Fig. 7. (a) Microfabrication process flow. (b) Simulated energy dissipation during an input sequence "1010" in a buffer.

termination will create a charge redistribution to turn on/off the FET.

IV. Pipeline of Logic Gates

We designed and tested a pipeline composed of four cascaded buffer gates arranged in an Adiabatic Dynamic Logic (ADL) architecture [11] as shown in Fig. 6.

In our experimental setup, the logic gates are connected to the four-phase T-shifted trapezoidal power-clock V_1, V_2, V_3, and V_4 by a homemade probe station. These synchronized clock signals (in charge of supplying and synchronizing the gates) are generated by a programmable multichannel voltage source. For the sake of clarity, we will no longer show the position of input–output electrodes, but only focus on the position of the active electrode in each buffer (x_{A1}, xA_2, x_{A3}, xA_4). Fig. 6(c) depicts the measurements of power-clock signals, the input sequence injected in the pipeline, and its mechanical response with optical testing. We used a low-frequency clock (0.4 Hz) to allow real-time imaging of the electrode motion with a microscope camera. The logic states are distinguishable from the positions of the electrodes, with amplitudes of motion in the micrometer range. We emphasize that there is no attenuation of the signal through the pipeline, proving the cascadability of our hardware implementation. The bits are delayed by T from gate to gate due to the ADL clocking scheme [12].

The amplitude of motion is controlled by the clock peak-to-peak voltage V_{pp}: higher V_{pp}, higher the displacements. However, if $V_{pp} < 4.5$ V the "1" states cannot be triggered and are converted in "0" through the pipeline, so the cascadability is lost. On the other hand, there is an upper limit of V_{pp} due to electrostatic interactions between electrodes and the underneath silicon substrate, separated by a 5 μm air gap. If $V_{pp} > 7$ V, the active electrodes are actuated downward and collapse on the substrate (out-of-plane pull-in).

V. Fabrication Flow

Other MEMS designs for performing contactless operation have already been discussed [7]–[9] but they need an insulating mechanical link in the mobile part to obtain four-electrode devices. Our design avoids the insulating link and thus drastically reduces the fabrication complexity.

Starting from a silicon-on-insulator (SOI) substrate, we fabricated electromechanical logic gates by means of laser lithography, Si etching, and removal of the buried oxide. Fig. 7(a) illustrates the key steps of the fabrication process. The substrate is an SOI wafer with a low-doped 1.75 μm-thick Si layer on the top of 5.11 μm of SiO_2. Prior to patterning, a 30-nm-hard-mask of aluminum is deposited over the sample by e-beam evaporation. The sample is then coated with a positive AZ1512HS photoresist and baked at 100 °C for 60 s. Lithography was performed with a laser power of 12 mW at a wavelength of 405 nm. Samples were developed with AZ developer for 30 s, and then in MF21 for 60 s to etch the hard mask. The top silicon layer is dry-etched for 90 s by a plasma of SF_6 and CH_2F_2. Electrodes are then released by removing the SOI buried oxide with vapors of fluorhydric acid for 90 min.

VI. Discussion

Our experimental results prove the ability of contact-free MEMS to perform logic operations in series. This demonstration is the first step toward a competitive hardware solution in terms of operating frequency, footprint, energy-saving, and reliability.

Unlike capacitive switches [16], EMAC does not require a high capacitive ratio because logic states are encoded by the position of the electrodes (i.e., tilt to the right or the left) instead of a voltage value. This particularity reduces the need for high capacitive contrast, unlike capacitive switches.

A. Reliability

Contact-free operation avoids the mechanical contact between electrodes like for certain RF MEMS capacitive switches with high reliability over cycling [17]. As the dissipation in EMAC logic gates is in the order of 0.1 pJ/op (cf., Section VI-C), no significant heating of the devices is expected. Therefore, we consider the contribution of the thermal effect [18] to the reliability negligible.

In EMAC, each logic state is associated with a motion, minimizing the mechanical degradation since all springs stiffnesses will drift simultaneously in time. Because EMAC does not use any dielectric solid material, it will not be affected by effects

TABLE II
EFFECT OF A FORM FACTOR ON THE PROPERTIES OF EMAC LOGIC GATES

Property	Scaling effect*
Gate footprint	$1/\alpha^2$
Voltage operation	$1/\alpha$
Operation frequency	α
Energy dissipation	$1/\alpha^3$

** hyp: all dimension shrunk by a α factor (constant form factor)*

such as dielectric charging observed in RF switches [19]. During our experiments in the hertz range, we have not observed any failure for days.

EMAC is not a dynamic logic family as [7]–[9] because all electrical nodes are always set. But the gate-to-gate interconnection is limited by the mechanical nature of the logic coding i.e., the displacement must be transmitted, not only the electrical polarization.

B. Operating Voltage/Frequency and Gate Footprint

Like any mechanical-based logic family, EMAC is limited by the mechanical time constant which caps the highest operating frequency. By stroboscopic imaging, we observed a correct operation (without logic errors) up to 2.5 kHz, corresponding to 80% of the frequency of the first mechanical mode of the buffers. Downscaling this proof-of-concept can increase the operating frequency, as demonstrated in nanoelectromechanical system (NEMS) relays (e.g., 15 ns switching time reported in [4]). If all dimensions are shrunk by a factor α, the frequency of operation is boosted by α (Table II).

An α downscaling factor reduces the surface of the gate by α^2. Although the buffer covers a large area of $200 \times 400\ \mu m^2$, improvements of the lithography process and the use of higher operating voltages will reduce this footprint and allow the realization of more complex circuits.

Assuming state-of-the-art microfabrication can downscale our MEMS gates by a factor of 100, we expect an operating frequency of 250 kHz under a 45 mV power supply with a gate footprint of only 8 μm^2. By considering alternative MEMS designs such as vertical actuation, liquid gap, or soft spring, the performance can be increased further.

C. Power Consumption Contact-Free

Operation avoids leakage losses as long as the MEMS dimensions remain high enough for avoiding quantum effects, such as tunneling currents between electrodes. Energy losses in our pipeline are mostly due to mechanical damping in the air, and to dynamic dissipation within the access resistors made by the long silicon springs that bear the electrodes. This dissipation almost vanishes for lower frequencies of operation. Due to technical limitations, we have not been able to measure the dissipation in our devices as it would have involved challenging measurements of low-frequency ac currents in the pA range. As the position given by our simulation shows a good correlation with experiments, we estimate the energy loss on the basis of numerical simulations of electrostatically coupled mass-spring damped oscillators (see [10] for modeling details). Fig. 7(b) shows a simulation output computed with experimental Q-factor and access resistors, and applied voltages), assuming a lossless fully reversible power supply. The dissipated energy per logic operation is 0.1 pJ/op at 2.5 kHz. Since the dissipation is proportional to kg^2 [10], it can be reduced by orders of magnitudes by downscaling the system. Because the circuit involves only reversible mechanical motions (no hysteresis, no pull-in), the dissipated energy/cycle of EMAC scales down with the operating frequency, like in other true-adiabatic architectures [11]. After scaling down all dimensions by 100, the circuit is expected to dissipate only 0.1 aJ/op (24 k_BT) at 250 kHz under a 45 mV power supply. This accounts only for the dissipation occurring within the logic gates and ignores the losses in the power clock. For this proof of concept, we used conventional waveform generators that are not able to recycle the energy of the gates. Further implementations will take advantage of resonant inductive clocks to address that issue.

TABLE III
COMPARISON OF THE PROPOSED LOGIC (EMAC) TO OTHERS LOGICS

	FET-based logic	Relay-based logic	Contact-free logic (EMAC)
Logic state coding	charge	charge	position *{x>0~"0" ; x<0~"1"}*
Cascadability	**Y**	**Y**	**Y**
Leakage-free	N	**Y**	**Y**
Energy Reversibility	N (V_{TH} limited)	N (Pull-in limited)	**Y** (Hysteresis-free)
Dynamic loss	Y	Y	**$1/F_{op}$***
Electrical contact	Y	Y	N
Mechanical contact	N/A	Y	**N****
Reliability after Billions of cycle	**high**	low	**high**
Footprint	**small**	large	large
Operation Frequency range	**GHz**	10's MHz	kHz***
Maximal temperature rating	~<200°C	500°C [8]	170°C (proven) >500°C (expected)

** scale-down with the operation frequency (adiabatic attribute), ** no deal with adhesion force or ON-state conductance, *** MHz could be envisaged with device scaling*

D. Temperature Robustness

Since our system relies on electrostatic interactions and mechanical motions, it is very robust against thermal changes. The logic state is encoded mechanically instead of electrically, reducing the effect of electrical noise. Our pipeline is operational up to 170 °C (similar results as in Fig. 6), corresponding to the upper limit of our sample-holder heater capability. Therefore, EMAC can withstand high temperatures where transistors are inherently limited, and where relays are facing oxidation of electrical contacts [15].

Table III summarizes the properties of EMAC circuits with respect to other computing paradigms.

VII. CONCLUSION

We demonstrated experimentally the proof of concept of a *contact-free* electromechanical pipeline in adiabatic operation.

The design is based on comb-drive actuators, which are reliable structures widely used in industrial-grade sensors. Contactless operation overcomes the reliability limitation of MEMS relays, avoids uncontrolled adhesion force, and solves the problem of the ON-state resistance. Electrostatic interactions, mechanical bits encoding, and reversibility of mechanical motion provide the upscaling capability, wide operating temperature range, and compatibility with adiabatic architectures. These results open new perspectives for low-power digital IC at the edge of the cloud, or for certain niche applications at high temperatures.

REFERENCES

[1] R. Landauer, "Irreversibility and heat generation in the computing process," *IBM J. Res. Dev.*, vol. 5, no. 3, pp. 183–191, Jul. 1961, doi: 10.1147/rd.53.0183.

[2] S. Houri, G. Billiot, M. Belleville, A. Valentian, and H. Fanet, "Limits of CMOS technology and interest of NEMS relays for adiabatic logic applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1546–1554, Jun. 2015, doi: 10.1109/TCSI.2015.2415177.

[3] M. L. Roukes, "Mechanical compution, redux?" in *IEDM Tech. Dig.*, Dec. 2004, pp. 539–542, doi: 10.1109/IEDM.2004.1419213.

[4] S. Saha, M. S. Baghini, M. Goel, and V. R. Rao, "Sub-50-mV nanoelectromechanical switch without body bias," *IEEE Trans. Electron Devices*, vol. 67, no. 9, pp. 3894–3897, Sep. 2020, doi: 10.1109/TED.2019.2951615.

[5] Z. A. Ye *et al.*, "Demonstration of 50-mV digital integrated circuits with microelectromechanical relays," in *IEDM Tech. Dig.*, Dec. 2018, pp. 411–414, doi: 10.1109/IEDM.2018.8614663.

[6] Y. Chen, R. Nathanael, J. Jeon, J. Yaung, L. Hutin, and T.-J.-K. Liu, "Characterization of contact resistance stability in MEM relays with tungsten electrodes," *J. Microelectromech. Syst.*, vol. 21, no. 3, pp. 511–513, Jun. 2012, doi: 10.1109/JMEMS.2012.2186282.

[7] G. Pillonnet, H. Fanet, and S. Houri, "Adiabatic capacitive logic: A paradigm for low-power logic," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4, doi: 10.1109/ISCAS.2017.8050996.

[8] H. Samaali, Y. Perrin, A. Galisultanov, H. Fanet, G. Pillonnet, and P. Basset, "MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation," *Nano Energy*, vol. 55, pp. 277–287, Jan. 2019, doi: 10.1016/j.nanoen.2018.10.059.

[9] R. Celis-Cordova, A. O. Orlov, and G. L. Snider, "Adiabatic capacitive logic using voltage-controlled variable capacitors," in *Proc. IEEE Silicon Nanoelectronics Workshop (SNW)*, Jun. 2020, pp. 115–116, doi: 10.1109/SNW50361.2020.9131626.

[10] Y. Perrin, A. Galisultanov, H. Fanet, and G. Pillonnet, "Electromechanical adiabatic computing: Towards attojoule operation," in *Proc. IEEE Int. Conf. Rebooting Comput. (ICRC)*, Nov. 2017, pp. 1–8, doi: 10.1109/ICRC.2017.8123660.

[11] P. Teichmann, *Adiabatic Logic: Future Trend and System Level Perspective*. Berlin, Germany: Springer, 2012, doi: 10.1007/978-94-007-2345-0.

[12] H. Fanet, *Ultra Low Power Electronics and Adiabatic Solutions*. Hoboken, NJ, USA: Wiley, 2016, doi: 10.1002/9781119006541.

[13] M. López-Suárez, I. Neri, and L. Gammaitoni, "Sub-kBT microelectromechanical irreversible logic gate," *Nature Commun.*, vol. 7, no. 1, pp. 1–6, Nov. 2016, doi: 10.1038/ncomms12068.

[14] J.-S. Wenzler, T. Dunn, T. Toffoli, and P. Mohanty, "A nanomechanical Fredkin gate," *Nano Lett.*, vol. 14, no. 1, pp. 89–93, Jan. 2014, doi: 10.1021/nl403268b.

[15] T.-H. Lee, S. Bhunia, and M. Mehregany, "Electromechanical computing at 500 °C with silicon carbide," *Science*, vol. 329, no. 5997, pp. 1316–1318, Sep. 2010, doi: 10.1126/science.1192511.

[16] L. Guan, J. K. O. Sin, H. Liu, and Z. Xiong, "A fully integrated SOI RF MEMS technology for system-on-a-chip applications," *IEEE Trans. Electron Devices*, vol. 53, no. 1, pp. 167–172, Jan. 2006, doi: 10.1109/TED.2005.860638.

[17] B. Lakshminarayanan, D. Mercier, and G. M. Rebeiz, "High-reliability miniature RF-MEMS switched capacitors," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 4, pp. 971–981, Apr. 2008, doi: 10.1109/TMTT.2008.919076.

[18] R. W. Herfst, P. G. Steeneken, and J. Schmitz, "Identifying degradation mechanisms in RF MEMS capacitive switches," in *Proc. IEEE 21st Int. Conf. Micro Electro Mech. Syst.*, Jan. 2008, pp. 168–171, doi: 10.1109/MEMSYS.2008.4443619.

[19] G. Li, W. Zhang, P. Li, S. Sang, J. Hu, and X. Chen, "Investigation of charge injection and relaxation in multilayer dielectric stacks for capacitive RF MEMS switch application," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2379–2387, Jul. 2013, doi: 10.1109/TED.2013.2263252.