Low-noise high-resolution BAW-based high-frequency oscillator

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The design of a 500 MHz oscillator in a 65 nm CMOS process using a 2 GHz bulk acoustic wave (BAW) resonator is presented. A digital frequency control is implemented using a switched capacitor bank in parallel to the resonator. The tuning range is up to 500 kHz with a minimum step of 200 Hz. The oscillator core uses a differential topology and is designed for low phase noise (−128 dBc/Hz at 100 kHz offset) at low power consumption (0.9 mW). It is followed by a low-noise divider, which provides a 500 MHz output with a phase noise of −139 dBc/Hz at 100 kHz offset from the carrier.

Introduction: Modern communication systems require high-performance oscillators for frequency conversion, synchronisation and sampling purposes. Applications requiring accurate, stable and low-cost circuits may profit from new integrated solutions on silicon to reduce the bill of materials. Low-frequency (26 MHz typically) crystal oscillators are used to create reference signals in RF. Silicon-integrated LC-oscillators would be a cheap solution for delivering direct high-frequency signals but they have poor frequency stability and high phase noise. A promising alternative is the use of bulk acoustic wave (BAW) resonators into the oscillator. Thanks to their high quality factor and high resonant frequency, RF oscillators with high spectral purity, equivalent to crystal oscillators, can be achieved [1]. The BAW resonators enable integration into a single chip or into a single package together with the RF transceiver.

Oscillator core: The oscillator Fig. 1 has a differential topology to facilitate its integration into a complete transceiver. It consists of a cross-coupled NMOS pair implementing a negative conductance. The frequency is set by the BAW resonator placed between the drains of the NMOS transistors. Each branch of the NMOS pair is supplied independently by a current source. To minimise frequency pushing and to achieve high-frequency stability with temperature, the supply current is stabilised relatively to supply voltage and temperature variations. To prevent a latch effect, positive feedback in this cross-coupled pair is suppressed at low-frequencies by a low-frequency filter [2].
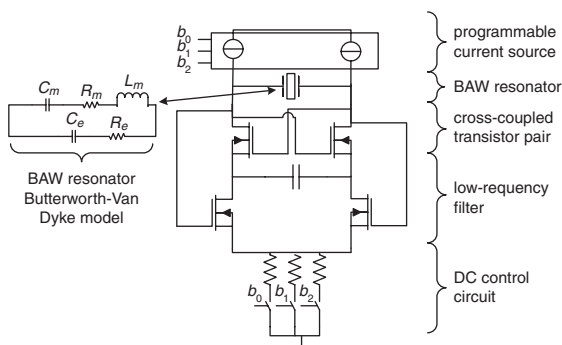

Fig. 1 *Oscillator core and BAW resonator using Butterworth-Van Dyke model schematic*

Frequency tuning consideration: Any BAW resonator consists of a piezoelectric layer enclosed between two electrodes. The particularity of solid mounted resonators is that the acoustic wave is confined into the resonator by a Bragg reflector [3]. The resonator can be modelled by the Butterworth-Van Dyke model as presented in Fig. 1. From this model, we can define the coupling factor between the acoustic and the electric waves in the resonator as follows:

$$k' = \sqrt{C_m/C_e} \tag{1}$$

where C_m and C_e are, respectively, the motional and electrostatic capacitances of the resonator.

The circuit oscillates at the parallel resonant frequency of the resonator loaded by the active circuit. The oscillation frequency lies between the series and the parallel resonant frequencies of the stand-alone BAW resonator [4]. The oscillator is divided into the resonator part and the active part for the analysis purpose. Each part is described by its admittance:

- $Y_{resonator} = G_{resonator} + j*B_{resonator}$, which is the admittance of the BAW resonator
- $Y_{osc} = G_{osc} + j*B_{osc}$, that of the active circuit

With this in mind, we can define the effective coupling factor of the circuit as

$$k' = \sqrt{C_m/(C_e + C_{osc})} \tag{2}$$

where C_{osc} is the capacitance presented by the active circuit to the resonator.

The oscillation frequency f_{osc} is determined from the solution of: $B_{resonator}(f_{osc}) + B_{osc}(f_{osc}) = 0$. It follows that:

$$f_{osc} = f_m\sqrt{1 + k'^2} \tag{3}$$

where $f_m = 1/\sqrt{L_m C_m}$ is the series resonant frequency of the motional branch. Because of the intrinsic capacitance of the active circuit, the effective coupling factor is always lower than the coupling factor of the resonator. This sets the upper limit of the oscillation frequency. By increasing the capacitance added in parallel to the BAW resonator, the effective coupling factor k' and the frequency decrease. This is the principle used for tuning the oscillator frequency. However, (4) shows that losses increase dramatically when the oscillation frequency gets closer to the series-resonant frequency:

$$G_m = \frac{1}{R_m + R_m Q_m^2 k'^4/(1 + k'^2)} \tag{4}$$

where $Q_m = \frac{1}{R_m}\sqrt{\frac{L_m}{C_m}}$ is the quality factor of the BAW motional branch. Consequently, at some point, the oscillation startup condition $G_{resonator}(f_{osc}) + G_{osc}(f_{osc}) < 0$ is not met anymore. This effect sets a lower limit to the oscillator frequency. The frequency tuning characteristics are illustrated in Fig. 2, which presents the normalised frequency and losses of the system as a function of the effective coupling coefficient.
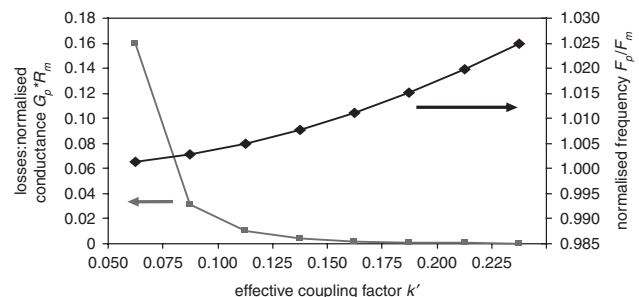

Fig. 2 *Normalised losses and frequency of oscillator*

The oscillator frequency can be precisely adjusted over the tuning range by means of two tuning banks. The coarse bank has a tuning range of 1024 ppm with 32 ppm steps. Its tuning range is wide enough to correct the BAW resonator process variation [5]. The fine bank has 50 ppm tuning range with very fine 0.2 ppm steps. The two banks are implemented using fringe capacitors. They are smaller than MOS capacitors and have a lower process spread than plate capacitors.

Measurement results: The oscillator has been implemented in a 65 nm CMOS process in order to facilitate its integration in a complete SOC. The measured performances of the BAW resonator are a parallel resonant frequency of 1.95 GHz, a quality factor $Q_m = 1000$ and a coupling factor $k = 0.17$. The active die and the BAW resonator are connected on a PCB by wire bonds, as shown in Fig. 3.

A divide by 4 is used at the output of the oscillator in order to directly provide the signal in the application at 500 MHz. Fig. 4 shows the phase noise variations according to the offset frequency from the 500 MHz carrier. This result is obtained thanks to the high quality factor of the BAW resonator, which filters a part of the noise generated by the oscillator core. The accuracy of the circuit is provided by the tuning banks. Fig. 5 shows that the frequency variation of our oscillator (after the

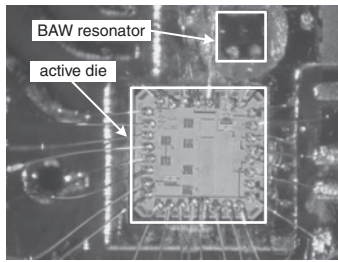divider) is linear. An accuracy of 200 Hz (0.4 ppm) on a 500 MHz signal is achieved.
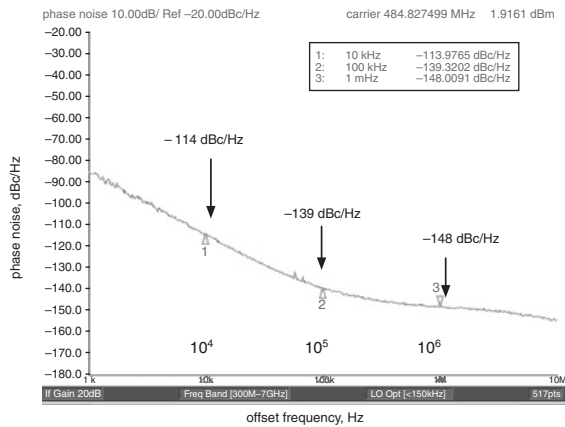

Fig. 3 *PCB photography*

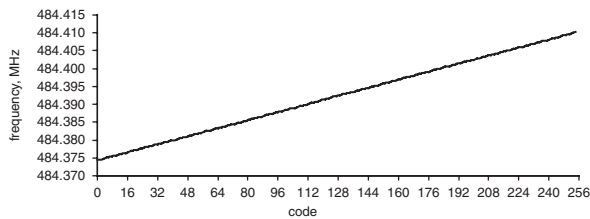**Fig. 4** *Measured phase noise after divider*

Fig. 5 *Measured oscillation frequency against 256 codes from fine bank*

The comparison with recent BAW oscillators given in Table 1 shows the aptness of our work. This Table demonstrates the importance of the differential structure and of the BAW resonator quality factor to achieve good performances. To our knowledge, we comment that other works do not include precise frequency tuning capabilities.

Table 1: BAW oscillator comparison

Ref.	Type	F_{osc} (GHz)	Power (mW)	Phase noise at 2 GHz (dBc/Hz)	Technology
[6]	Pierce (single)	1.9	0.3	−112 at 10 kHz	BiCMOS
[1]	Butler (single)	2	4	−120 at 100 kHz	BiCMOS
[7]	Colpitts (single)	2	6.8	−118 at 100 kHz	SiGe BiCMOS
[2]	Diff.	2.1	0.6	−122 at 100 kHz	CMOS 0.13μ
This work	**Diff.**	**2**	**0.9**	**−128 at 100 kHz**	**CMOS 65 nm**

Conclusions: We have implemented a new digitally-tuned BAW-based oscillator in a 65 nm CMOS process. The circuit presents a high spectral purity (−128 dBc/Hz before the divider and −139 dBc/Hz after 100 kHz from the carrier frequency). Low power consumption (0.9 mW) is achieved. The oscillator frequency is digitally tunable over a 500 kHz tuning range in 200 Hz steps. With its high spectral purity and its fine tuning capability, this new type of oscillator offers a solution for silicon-based SOC integration for many applications where low power consumption, accuracy and stability are required.

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