TC5747 Datasheet

Single Chip CMOS Imager with Integrated Image Signal Processor and JPEG Codec

Version 1.8 **07 December 2005**

Revision Log

Revision	Description	Date
0.1	Initial Version	21 August, 2003
0.2	Updated lens specifications	9 September, 2003
0.3	Corrected description of power down modes	18 September, 2003
0.4	Added description of PLL operation, startup timing and control signals for host access to LCD.	23 October, 2003
0.5	Revised section 5 order and added info regarding the host and LCD interfaces. Added 24-pin optional package.	29 October, 2003
0.6	Included two module package dimensions for packaging with and without CSP.	11 November 2003
0.7	Added initial mechanical drawing of 60-pin module with detailed pin list.	23 November, 2003
0.8	Corrected module dimensions.	27 November, 2003
0.9	Added 39-pin and 51-pin options.	29 January, 2004
1.0	Updated power down pins functionality	11 March, 2004
1.1	Updated 39-pin diagram. Reversed pins 3, 4 in 39-pin option.	18 April, 2004
1.2	Update 24-pin list and lens specifications	22 April, 2004
1.3	Changed program memory from 32K to 48K, changed I2C address.	2 June, 2004
1.4	Changed FOV in Lens Specification, removed Char. Results, removed RGB888 and changed PS1/PS2 #10 to Reserved.	13 June, 2004
1.5	Updated template.	7 March, 2005
1.6	Updates.	15th May, 2005
1.7	Remove “Preliminary Data Sheet”	01 August 2005
1.8	Changed 36 MHz to 32 MHz. Updated PLL configuration parameters.	07 December 2005

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1. Introduction

The TC5747 is a single chip VGA (640 lines over 480 pixels) color CMOS sensor with an integrated color processing and JPEG codec. It is designed to meet the requirements of cellular devices with low power consumption and miniature size. An embedded programmable core with dedicated hardware performs the extensive color processing. An embedded real-time JPEG encoder and compressed frames SRAM store JPEG images on chip. The TC5747 has flexible interfaces and supports multiple video output formats for easy integration into cellular phones. It supports a 16-bit host interface for fast data access and control.

1.1 Features

The TC5747 features a state-of-the-art architecture, allowing extremely low power consumption and miniature size. The following are the product highlights.

- Sensor Array
  - 1/4" optical format
  - VGA resolution 640x480
  - 5µm x 5µm square pixels
  - Integrated 10 Bit ADC
  - RGB mosaic with micro-lens for high sensitivity
  - Double sampling for fixed pattern noise reduction
  - Separate gains for R, G and B
  - Programmable frame rate up to 20 fps VGA and 40 fps QVGA
  - Programmable window size and filtered-option sub-sampling
- Image processing
  - Embedded Image Signal Processor (ISP)
  - Embedded micro controller with 32 Kbytes program memory
  - Faulty pixel mechanism
  - Loadable gamma correction tables
  - Automatic white balance
  - Automatic exposure control
  - Despeckle function
  - Enhanced dynamic range for backlight illumination
  - Programmable 3x3 color correction matrix
  - Programmable 3x3 sharpening or blurring matrix
  - Anti flicker for 50Hz and 60 Hz
  - Horizontal and vertical inversion
  - Digital zoom of 4X, 2X
  - Color adjustments such as: brightness, contrast, saturation
  - Digital effects, such as monochrome, negative, sepia
  - Frame or stamp overlay on the captured image (up to 320x240)
  - Down sampling by 2x, 3x, 4x, 5x, 6x, 7x, 8x

- JPEG Codec
  - Real-time JPEG encoder and decoder for still images and M-JPEG for motion video
  - Compression of up to VGA YUV 422 format images
  - Decompression of up to VGA resolution, 4:2:2, 4:1:1, 4:2:0 format images
  - Programmable compression ratio, up to 1.8 bits/pixel for VGA image
  - JPEG compression is done in parallel with preview of the video on the LCD
  - Thumbnail image support
  - Portrait images for phone book
  - Compression and decompression from the internal memory
  - Compression can be done after scaling and overlay of frame and stamp data
  - Decompressed image can be resized and re-compressed
- On screen display
  - On screen display overlay of up to QVGA (320x240) resolution, 4-bit OSD data color table
  - Support of up to two layers of OSD data. The first layer can be used to add frame of stamp to the captured image. The second layer can be composed of one or two non-overlapping regions of OSD for switching messages and icons. Each OSD window has its own 4-bit color table.
  - Support of 32x32 pixel cursor with 4-bit color table
  - Rotation of JPEG images display by 90^0 or 270^0
- Video Interface
  - Flexible output formats including: Bayer, RGB (666, 565, 444), YUV/YCrCb 4:2:2 and JPEG
  - 18 bits direct interface to LCD: supports 8/9/16/18 bit output
  - Chip select for two LCD (main and sub)
  - Camera standby mode for host access to the LCD
  - Optional configuration of 8 bits camera interface
  - Horizontal and vertical sync signals
  - CCIR656 compatible signaling markers
  - Optional high-speed bi-directional serial interface
  - Support of two simultaneous video output streams
- Host Interface
  - 8/16bit bi-directional I80 and M68 access types host interface
  - Optional I^2C or UART interface for programming and control
- Easy to use software API
- Input clock frequency: 3.6MHz to 32MHz
- Power consumption, VGA@ 15 FPS is 85 mW.
- Power management to support low power modes
- Operation voltage 2.8 +/- 10%
- Technology: 0.25 um s
- Operation temperature: -10 to 60 degrees Celsius
- Packaging types: module with lens. Module can have either flex cable or board-to-board connector. Several pin-out options will be supported to provide selected interface functionality.
- Module size is 9.8mm x 9.45mm x 5.5mm

1.2 Optimized Interfaces

The TC5747 has both a parallel and serial video interface, which allows the output of two simultaneous video streams to the host. This concept is shown in Figure 1. One interface allows direct parallel display-ready RGB interface to the LCD with no glue logic for preview. The second interface allows connection to the base-band or application processor for a compressed image or video stream.

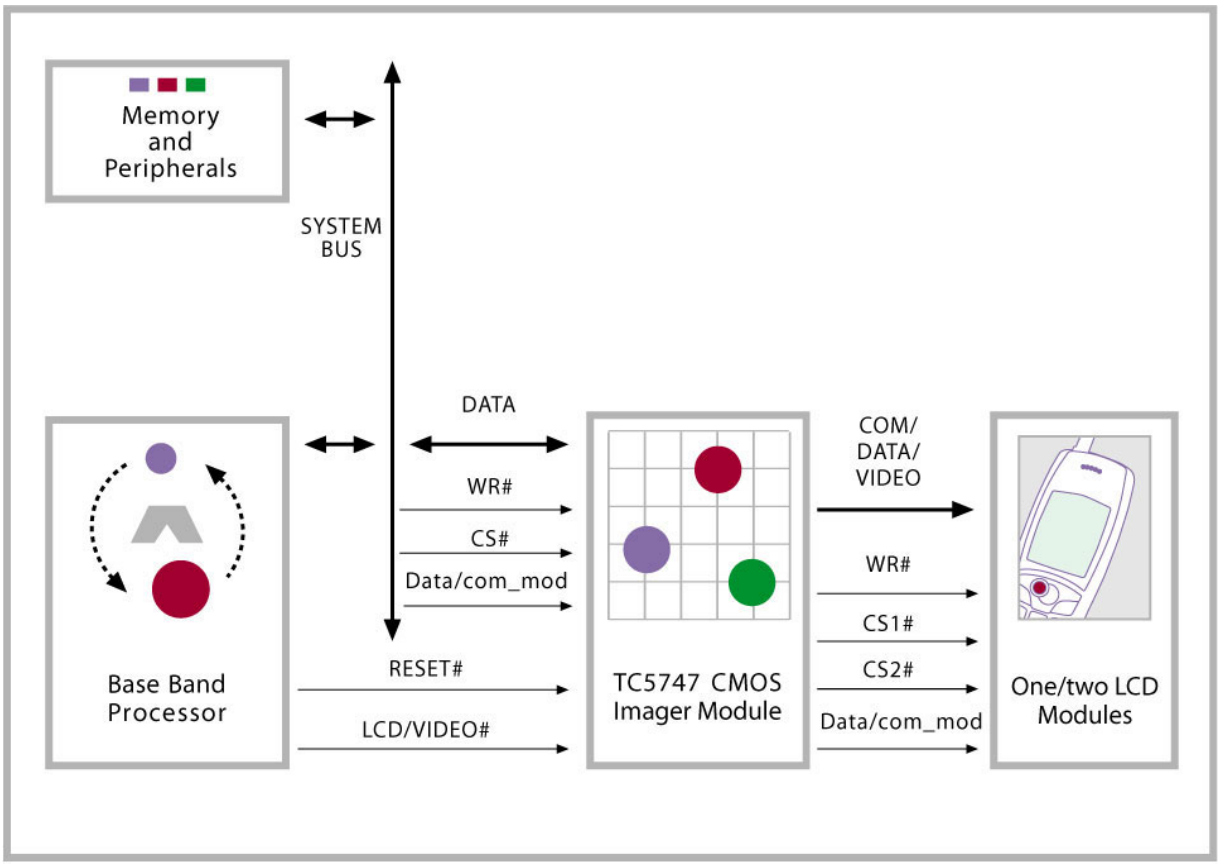


Figure 1: Host and LCD Interfaces

1.3 Specifications

Feature	Description
Array format	VGA - 656x524 physical pixel, 648x492 active pixels for 1/4" optics
Capture size	Configurable window size
Pixel size	5µ x 5µ
Color filter	RGB Mosaic with micro lens
Supply Voltage	2.8V ±10%, internal regulators for digital and analog supplies
Power consumption	85mW at 15 fps (including color processing)
Power save modes	Sleep mode with maximum of 100µA current and wake up of less than 100msec. Power down mode with up to 10µA current.
Input clock frequency	Internal PLL supports input clocks of 3.6MHz – 32MHz.
A/D converter	10 bit ADC
Down sampling	Down sampling with filter by 2X to 8X in both dimensions.
Video output format	YCrCb422 / YUV422 / RGB444 / RGB565 / RGB666 / Raw / JPEG;
Video output interface	8/9/10-bit parallel camera interface or 8/9/16/18 LCD controller data interface
Video synchronization	Horizontal and vertical sync signals and/or CCIR656 header
Control interface	▪ 6-bit host bus interface ▪ I^2C compatible interface ▪ UART ▪ Used also to read JPEG images
Frame rate	Variable up to 20 fps for VGA or 40 fps for QVGA
JPEG	HW JPEG encoder/decoder acceleration
JPEG frames memory	On-chip 64Kbyte SRAM to store compressed images
Program memory	On-chip 48Kbyte SRAM to store firmware for the ISP
Readout control	Progressive readout; vertical and horizontal inversion options
Exposure control	From one line to one frame duration with 250ns granularity.
AGC	Separate gain for each of the three color components R,G and B
Dynamic range control	Enhanced dynamic range
Image enhancement	Black level, faulty pixel correction, color correction, auto white balance, auto exposure, anti-flicker, gamma correction, color suppression.
Anti shading	Lens shading correction
Zoom	Digital zoom by 2X, 4X.
Image controls	Contrast, brightness, saturation, sharpening, windowing, lookup table
Camera module	Camera module package with lens, optional flex cable or board-to-board connector
SNR	TBD
Sensitivity	4V/lux-sec (including gain)

Table 1: TC5747 Specifications

2. TC5747 Output Connections

TransChip TC5747 camera module will be available in several configurations, each offering different interfacing options. The planned configurations are:

- 51-pin camera module –a connector module that supports 16-bit host interface and 16-bit glue-less LCD interface.
- 39-pin camera module – a smaller connector that supports 8-bit host interface and 8-bit glueless LCD interface.
- 24-pin camera module – a backward compatible module with TC5740, with control done via I^2C for control and 8-bit LCD interface.

TransChip can design other customized module connector pins.

2.1 Compact 51-pin Camera Module

The 51-pin camera module option uses a 16-bit parallel host interface for control and a 16-bit glue-less interface to the LCD.

Pin	#	I/O	Description
RESET_N	1	I	Asynchronous reset input signal; active low
CLK_IN	2	I	16-32 MHz clock input or crystal input
AGND	3	I	Analog circuits ground.
AVDD28	4	I	2.8V supply for analog circuits.
HLCDD[15:0]	5-20	I/O	Data input from host for both TC5747 and LCD
DGND	21	I	Digital circuits ground.
HADD / HLCD_RS	22	I	Address input from host to TC5747 / Host select between register and data in LCD
HCS_N	23	I	Chip-select signal from system host to TC5747
HWR_N	24	I	Write signal from system host.
HRD_N	25	I	Read signal from system host.
HLCD_CS_N	26	I	Host control over DOUT and HVALID pins
LCD_WR_N	27	O	Write to LCD – active low
LCD_CS1	28	O	Chip-Select to LCD #1
LCD_CS2	29	O	Chip-Select to LCD #2
LCD_RS	30	O	Register/address select input to LCD
Shield	31	-	Module noise shield
DOUT[17:10][8:1]	32-47	I/O	16-bit output video data to LCD. The 16-bit data is composed out of the internal 18-bit data accuracy.
DVDD28	48	I	2.8V for digital circuits
LED control	49	O	GPO pin, Activates the white LED for low light condition
PS1	50	I	Chip operation modes [PS1, PS2]: 00 – Startup 01 – Full operation 11 – Sleep 10 – Power down
PS2	51	I	

Table 2: 51-pin Module – Pin List

2.2 Compact 39-pin Camera Module

The 39-pin camera module uses I^2C for control and an 8-bit host interface to write to the LCD.

Pin	#	I/O	Description
Reserved	1	-	Not connected
Reserved	2	-	Not connected
PS2	3	I	Chip operation modes [**PS1, PS2**]:
PS1	4	I	00 – Startup 01 – Full operation 11 – Sleep 10 – Power down
LED control	5	O	GPO pin, Activates the white LED for low light condition
DVDD28	6	I	2.8V supply for digital circuits.
DOUT[1:8]	7-14	I/O	8-bit output video data to LCD
Shield	15	-	Module noise shield
LCD_RS	16	O	Register/address select input to LCD
LCD_CS2	17	O	Chip-Select to LCD #2
LCD_CS1	18	O	Chip-Select to LCD #1
LCD_WR_N	19	O	Write to LCD – active low
HRD_N	20	I	Read signal from system host.
HLCD_CS_N	21	I	Host control over DOUT and HVALID pins
HWR_N	22	I	Write signal from system host.
HCS_N	23	I	Chip-select signal from system host to TC5747
HADD / HLCD_RS	24	I	Address input from host to TC5747 / Host select between register and data in LCD
DGND	25	I	Digital circuits ground.
CLK_IN	26		16-32 MHz clock input or crystal input
RESET#	27		Asynchronous reset input signal; active low
HLCDD[0:7]	28-35	I/O	**HLCDD[0:7]** - Data input from host for both TC5747 and LCD
AVDD28	36	I	2.8V supply for analog circuits.
AGND	37	I	Analog circuits ground.
SDIN	38	I/O	I^2C compatible bi-directional data signal. Open-drain type. For Parallel Host access: Sampled during RESET#: Selects between two types of host interface: 0 – **M68** Type 1 – **I80** type
SCLK	39	I	I^2C-compatible input clock signal generated by the I^2C master

Table 3: 39-pin Module Pin List

2.3 Compact 24-pin Camera Module

The 24-pin camera module option uses I^2C instead of the parallel host interface for control and it uses an 8/9-bit parallel interface instead of 16/18-bit glue-less interface to the LCD. This option is offered for backward compatibility with TC5740, TransChip's first generation VGA imager.

Pin Name	#	I/O	Description
SCLK	1	I	I^2C-compatible input clock signal generated by the I^2C master.
AGND	2	I	Analog circuits ground.
AVDD28	3	I	2.8V supply for analog circuits.
RESET#	4	I	Asynchronous reset input signal; active low
CLK_IN	5	I	16-32 MHz clock input or crystal input
DGND	6	I	Digital circuits ground.
DOUT[1]/CSDAT# *	7	I/O	9th bit data /External Chip Select for data bus; active low
DYUV[0]	8		Output video data
DYUV[1]	9	I/O	Output video data
DYUV[2]	10	I/O	Output video data
DYUV[3]	11	I/O	Output video data
DYUV[4]	12	I/O	Output video data
DYUV[5]	13		Output video data / i2c_toggle - Selects between two I^2C addresses during RESET#
DYUV[6]	14	I/O	Output video data
DYUV[7] / DSDAT	15	I/O	Output video data / Serial Output Data signal
VCLKOUT/ DSCLK	16	O	Parallel video interface clock output/ Serial output clock
VALIDH / WR# / DSFRM	17	O	Horizontal VALID output / Write to LCD – active low Serial Output Frame signal
VALIDV	18	O	Vertical VALID output signal or interrupt output on Frame start
DVDD28	19	I	2.8V for digital circuits
SDIN	20	I/O	I^2C -compatible bi-directional data signal. Open-drain type.
PS1	21	I	Chip operation modes [PS1, PS2]:
PS2	22	I	00 – Reset 01 – Full operation 11 – Reserved 10 – Reserved
Reserved	23	-	Module noise shield
LED control	24	O	GPO pin, Activates the white LED for low light condition

- 9th bit output or chip select options are selected through wire bonding

Table 4: 24-pin Module Pin List

3. Functional Description

The figure below shows the main functional blocks of the TC5747 and the basic signal flow.

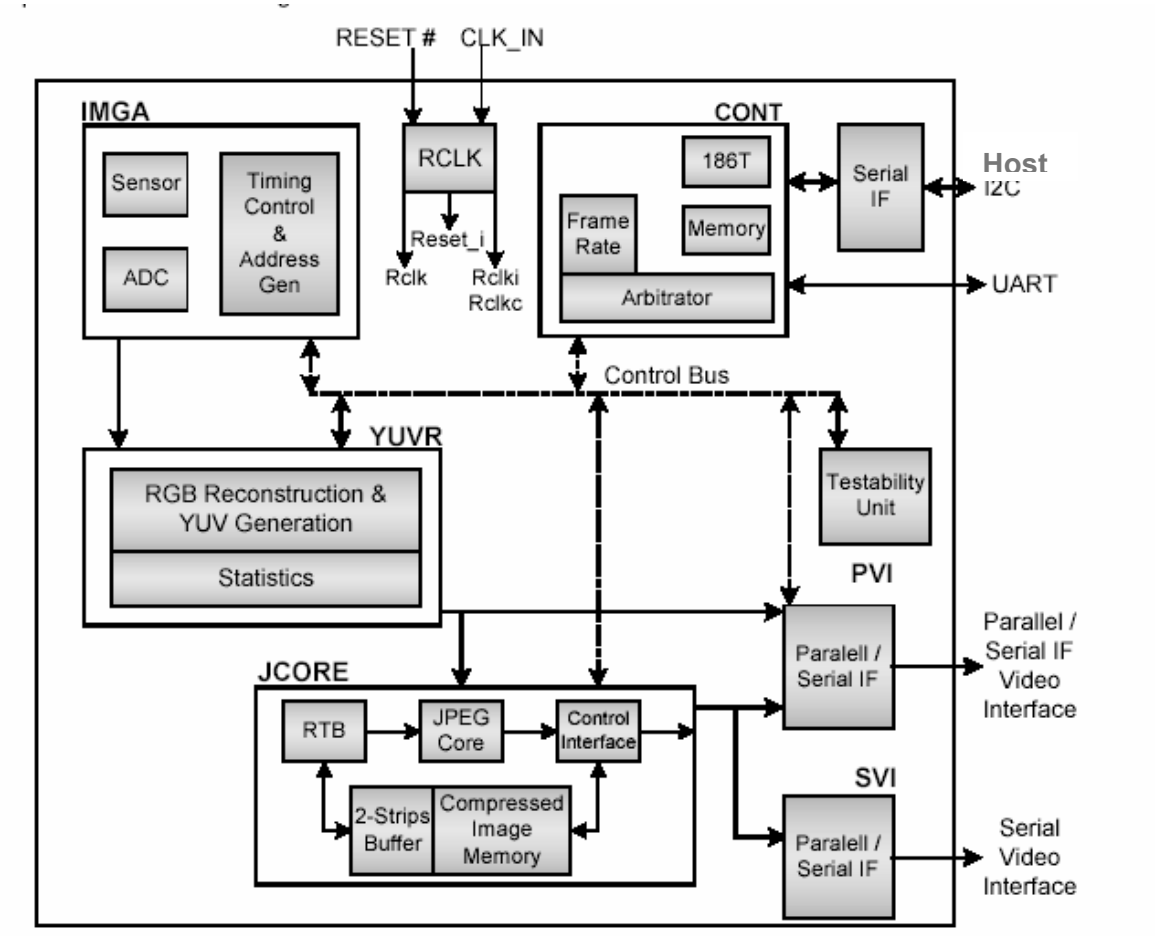


Figure 2: TC5747 Functional Block Diagram

3.1 CONT

The **CONT** unit controls the TC5747 units via a central programming bus. Its operation is synchronized with the frame image sequence through several interrupt sources. It is directly accessed by the serial interfaces

3.2 RCLK

The **RCLK** unit generates the **RESET** and **CLOCK** signals to the various units.

3.3 IMGA

The **IMGA** unit controls the image array and the analog processing unit. It produces the various timing controls, performs the "Mirror" transformations and the "Fixed Pattern Noise" corrections. After receiving the array pixels (the **ADC** output) and performing the required corrections and offsets, the data is sent to the **YUVR** unit for processing, or to the **PVI** or **SVI** unit for Bayer output.

3.4 YUVR

The **YUVR** unit transforms the Bayer data received from the **IMGA** unit into **YUV** or **RGB** data by applying several image reconstruction and correction algorithms. Demosaicing, dynamic range enhancement, digital gain, filter downscaling, sharpening or blurring, color correction, gamma correction, **RGB** to **YUV** conversion, **YUV**-to-**RGB** conversion and cropping for display are all performed in the **YUVR** unit. Resizing of the image can be done by 2X – 8X to achieve target LCD screen size with full field of view.

3.5 JPEG

The **JPEG** unit performs encoding or decoding of **JPEG** images. In encode mode it receives **YUV 4:2:2** data, and compresses the image into a **JPEG** stream. The **JPEG** compressed image is stored in RAM that is accessible to the **CONT** unit core and to the I^2C interface. The **JPEG** unit can also be configured to send out the RAM content to one of the output units, with optional ancillary data header and checksum.

In decode mode, the compressed code is written to the Code memory, and the JPEG unit decodes it into **YUV 4:2:2**, 4:2:0 or **4:1:1** data.

4:2:0 and **4:1:1** formats are interpolated into **4:2:2** format. **YUV** data are then sent to the **YUVR** unit for resizing and cropping. From the **YUVR** unit the decoded image is sent to the Parallel Video Interface unit for display.

Compression of a display ready image, after scaling and overlay of screen bitmap is also supported.

The **JPEG** unit can also output a thumbnail image.

3.6 PVI and SVI

The Parallel Video Interface (**PVI**) and Serial Video Interface (**SVI**) units are the output interfaces of the TC5747 device. Each interface can be configured to output one of several streams (**Bayer**, **YUV 4:2:2**, **RGB**, **JPEG**). The **PVI** can be configured as a parallel video interface or as a serial output interface.

3.7 Imager and Address Generator

The imager includes a VGA size pixel array, gain, double sampling, black pixel and readout circuits and ADC. The address generator receives timing signals from the control unit and produces the sequence signals to the pixel array for exposure control, read and reset operations. There are several modes of reading the array content, enabling various image resolutions by windowing and by down sampling. At different modes, various modes of power saving are used. VGA sized images can be read at a rate of up to 20 frames per second. For smaller images at higher frame-rates, several working modes are implemented.

3.8 Pixel Array Configuration

The pixel array is 648 by 487 active pixels, surrounded by four black columns on each side and 13 black lines above and 14 black lines below the active image array. This results in a total of 656 by 514 pixels.

3.9 Bayer Grid Configuration

Each pixel in the array is covered by a color filter, to create a Bayer grid format:

The sensor operates in rolling mode, in which the exposure and readout processes are linked. The sampling of each row data is performed at the end of the integration time. After sampling the selected-row data, the row is reset. The row is sampled again after the reset for the double-sampling procedure. The integration of that row starts again according to the exposure parameters.

A set of registers defines the total size of the frame and the size of the array that is read out and sent to the **YUVR** unit for further processing. Another set of registers defines the exposure time that is required for the array.

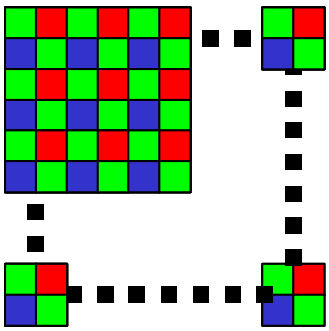


Figure 3: Bayer Grid Configuration

3.10 Resolutions and Frame Rates

The following table summarizes the possible resolutions and frame rates that the TC5747 can produce. The calculation for modes 1, 2 and 3 assume an input and color-processing clock of 32MHz. For mode 4, a 16MHz clock is assumed. The analog clock rate varies according to mode.

	MODE 1 (Full resolution)	**MODE 2** (MODE1with window)	**MODE 3** (down-sample, only 1 ADC is used)	**MODE 4** (down-sample with speed-up)
	32MHz **rclk**	32MHz **rclk**	32MHz **rclk**	16MHz **rclk**
	8MHz pixel clock	8MHz pixel clock	8MHz pixel clock	4MHz pixel clock
	8 **rclk** cycles/pix	8 **rclk** cycles/pix	8 **rclk** cycles/pix	4 **rclk** cycles/pix
	Full power	Full power	Slightly reduced power	Significantly reduced power
VGA	20 fps			
QVGA– no down sample		40 fps (reduced field of view)	40 fps (full field of view)	40 fps (reduced field of view)
QVGA–down sample	20 fps			

Table 5: Analog Clock Rate Modes

3.11 Analog Processing

Analog processing includes a separate gain control for each color filtered pixel, dark pixel correction for each color separately, dark and black-offset correction, faulty pixel replacement and 10-bit ADC.

3.12 On-chip Micro Controller

The TC5747 is fully controlled by the embedded microcontroller. Once the firmware, which is supplied by TransChip, is loaded, the embedded microcontroller sets the appropriate registers, and runs the automatic image processing algorithms. An external host does not need to access TC5747 registers and set values, nor does it need to run any algorithm. An easy to use API (Application Programming Interface) is provided to set or adjust various camera controls. The API is performed via a small set of host commands, which are sent over the serial interface (I^2C or UART), and are interpreted by the embedded microcontroller, to perform specific camera control, or any other defined internal task.

The set of host commands include:

- Color adjustments (Brightness, contrast, saturation, etc)
- Image Format (size, mirror x and y, etc)
- Automatic algorithm enable and parameters (Auto Exposure, AWB, Auto Flicker detection and cancellation)

The concept of host commands makes it very useful, as it is going to be forward compatible with any of TransChip sensor, since it is not hardware dependent (namely no need to use specific hardware registers.

TransChip supplies sample C code, which shows how to upload the firmware and use the host commands (software API). The sample includes all the needed C header files. The supplied firmware comes with preset default values for the various controls. Thus even if no single host commands is performed the firmware ensures that the sensor is running properly according to a preset default set.

TransChip also supplies a released version of the firmware.

The host commands are fully detailed in a separate document.

3.13 Bayer to YUV Translation Unit (YUVR)

The **YUVR** is the color-processing unit. The unit's parameters and mode registers are loaded through the control bus. The Bayer image is received from the **IMGA** unit, processed by the **YUVR** unit, and transferred to the PVI unit for output out of the device. While processing the image, statistics are calculated by the **YUVR** unit. After completing the processing of an image, the **YUVR** unit produces an interrupt to the **CONT** unit. The **YUVR** thus signifies to the **CONT** that the statistics for the current image are ready, and the **CONT** may read the results through the main control bus.

The **YUVR** unit receives the **Bayer** grid as input. For each pixel, two color values are missing and need to be reconstructed. The input accuracy is 10 bits. The **YUVR** unit reconstructs the **RGB** per pixel, performs correction algorithms and generates the **YUV** representation of the image.

Digital color processing includes: demosaicing, dynamic range enhancement, digital gain, filter downscaling, sharpening or blurring, flicker detection and removal, color and white balance correction, gamma correction, color suppression, zoom by 2X or 4X, **RGB** to **YUV** conversion, **YUV**-to-**RGB** conversion, down sample and cropping of **RGB** for display, **RGB** formatting (**6:6:6, 5:6:5, 4:4:4**) are all performed in the **YUVR** unit.

Zoom is performed by creating a full resolution image from a small region in the center of the image. The small region is blown up by 2X or by 4X to the target image size. The missing pixels are interpolated from the original pixels using a filter to provide a smooth appearance.

3.13.1 OSD and Cursor Overlay

A bitmap image can be overlaid over the sensor image. This feature, called OSD (On Screen Display), is used to create a display image that is a combination of the sensor image, icons or graphics, and a cursor image.

The TC5747 supports two OSD planes for up to QVGA size, with 4 bits per pixel representation. The 0x0 value is reserved for transparent bit, while 0x1 to 0xF values are translated into 15 different colors using a color table of YUV values. The first layer can be used to add a stamp frame to the captured image. The second layer can be composed of one or two non-overlapping regions of OSD for switching messages and icons. Each OSD window has is own 4-bit color table. The definition of two regions in the second plane makes it possible to save memory space by storing the icon bar separately from the OSD image that covers most of the display. It is possible to store several different notices or graphics in the memory, and switch between them by a single host-command.

A cursor is superimposed on top of the resulting image (after overlay of the two OSD planes). The 32x32 pixel cursor has a 4-bit color table with the same format as the OSD color table.

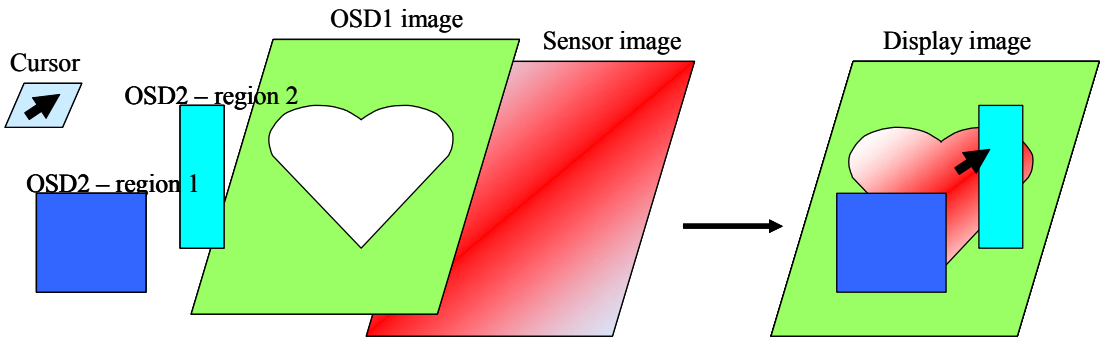


Figure 4: Two OSD Layers And Cursor

3.14 JPEG Compression Unit (JCOR)

The **JPEG** unit receives the **YUV 4:2:2** image data from the **YUVR** unit, and performs real-time **JPEG** compression. A 25K Byte memory is used for the **JPEG** compression process. The memory is divided into a Raster-to-Block operation buffer and a **JPEG**-code memory section. The 64K Bytes of memory can hold a full VGA-sized compressed image at a compression ratio of up to 1.7 bits per pixel.

The partition of the memory is fully configurable.

- When a higher compression ratio is used, several images can be stored in the memory. For example, when capturing a VGA-sized image, three compressed images of 0.5 bits per pixel can be stored in the 64K Byte **JPEG**-code memory section.
- When capturing a smaller image, a smaller buffer is required for the Raster-to-Block operation. Therefore a larger **JPEG**-code memory section can be allocated for support of a lower compression ratio.

The **JPEG**-compressed image can be transmitted either on the parallel video output interface or on the serial video output interface. Alternatively, the host can read the **JPEG**-compressed image from the on-chip **JPEG**-code memory via the I^2C interface.

The **JPEG** unit can optionally create also a thumbnail image for the full resolution compressed image.

The **JPEG** unit can also be configured to send out RAM contents to one of the output units, with optional ancillary data header and checksum.

The **JPEG** unit can also be activated in decompression mode. The compressed code is written to the Code memory, and the **JPEG** unit decodes it into **YUV 4:2:2** data. The **YUV** data is then sent to the **YUVR** unit for resizing and cropping. From the **YUVR** unit the decoded image is sent to the Parallel Video Interface unit for display.

4. Reset and Clock

4.1 Low Power Modes

The chip operation is controlled by two bits [**PS1, PS2**]:

Chip operation modes [**PS1, PS2**]:

- **00** – Startup
- **01** – Full operation
- **11** – Sleep
- **10** – Power down

4.1.1 Startup

The camera powers up at start up mode "**00**". Then it moves to full operation mode "**01**".

4.1.2 Bypass

To enter bypass mode, send a host command for power save, then provide standby mode "**11**" or switch off the input clock. Bypass mode power consumption is 60µA. This minimum power is consumed by a minimal power-supply digital regulator. Contents of memories and registers are maintained. The host can access the LCD during bypass mode.

To return to full operation from standby mode, switch on the input clock and wait for clock stability, then send a host command for full operation.

4.1.3 Power Down

To enter power down mode, send a host command for power down, and then provide power down mode "**10**". Power down mode consumes less than 10µA.

To return to full operation from power down mode: provide full operation mode "**01**", wait for clock stability, then send a host command for full operation and load the camera program.

4.2 PLL Configurations

An on-chip PLL is configured to supply the internal working clock signal in several modes:

- Bypass mode – internal clock is identical in frequency to input clock.
- **PLL** mode, for support of an internal clock in the range of 24-32MHx
  - 8x – internal clock is 8x the input clock, for support of low frequency input (3-4MHz input)
  - 4x – internal clock is 4x the input clock, for support of low frequency input (8MHz input)
  - 2x - internal clock is 2x the input clock, for support of medium frequency input (13-16MHz input)
  - 1.5x - internal clock is 1.5x the input clock, for support of high frequency input (20-21MHz input)

Each of the two output units, the **PVI** and **SVI** have a serial clock whose frequency is a multiple of the input clock. Each clock, **rclkp** and **rclks** is configured separately.

4.3 Device Initialization Sequence

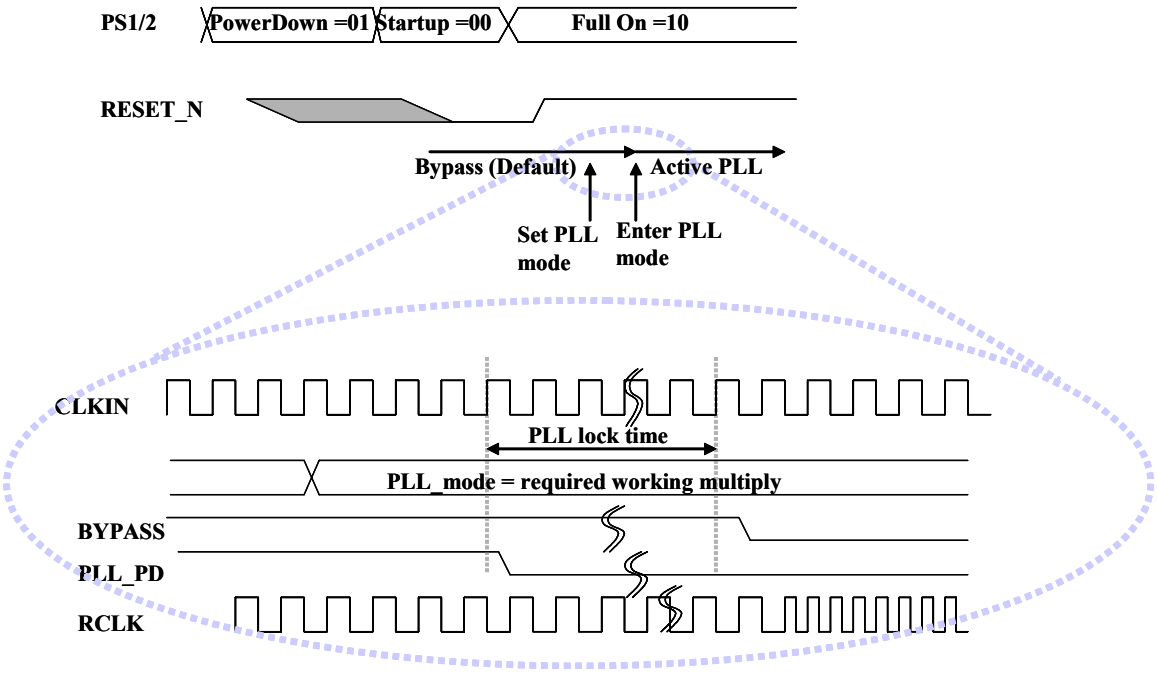


Figure 5: Initialization Sequence

The Initialization sequence includes the following steps:

1. After system power-up, the Power Save pins should be put into Startup mode.
2. Clock input and **RESET_N** should be activated.
3. After the Regulators' wake up time, the Power Save pins should be put into Full-on mode.
4. **RESET_N** is deactivated.
5. **PLL** mode should be set.
6. After **PLL** lock time, Bypass mode may be deactivated.

When working in Bypass mode, steps 5 and 6 may be skipped.

5. TC5747 Interfaces

The TC5747 chip has the following interfaces:

- LCD interface
- Host interface
- In addition it supports other configurations:
- Parallel Video Interface (PVI)
- Serial Video Interface (SVI)
- I^2C or UART control interface

The TC5747 is capable of providing two video streams at its output.

5.1 LCD Interface

A regular system that includes a host processor, LCD module and camera module is implemented by connecting the image sensor to the host controller using a camera interface and connecting the host controller to the LCD using the system bus. The drawbacks of this approach are that the host controller is loaded by processing the image data and that the system bus is loaded with transferring the image data.

A second approach is to remove the image data overhead from the host during camera operation and send the image data directly to the LCD. In this approach, the camera drives the image data directly to the LCD and the host controller accesses the LCD when the sensor is not active. While the camera operates there is a pass-through of the host control to the LCD through the TC5747. The TC5747 interfaces to the LCD with 8, 9, 16 or 18 bit data. Write, Read, Address and Chip-select (for 2 LCDs) controls provide full control over the LCD. For the RGB data configurations please see section 5.2.6.

Two LCD devices are supported by the TC5747. When the host performs a read access from the LCD, the chip-select pin of the selected LCD is activated using the LCD_CS1/2 output controls. The Host access to LCD should include random logic only, so that Host access is still supported while the TC5747 is in bypass mode.

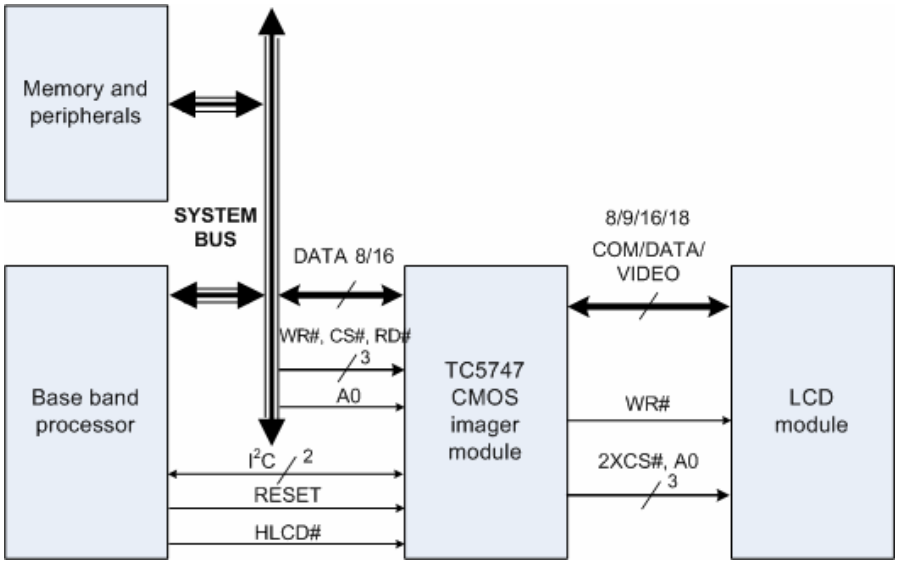


Figure 6: Direct Stream Through to LCD

5.1.1 Direct Host access to Camera interface

The TC5747 supports a system configuration where the LCD controller device is connected directly to the PVI pins. The system Host may access the LCD controller through the TC5747. Only Host- Write access is supported.

The Host interface includes 8 data input pins and 3 control pins. The Control pins are:

- **HLCD_BB#** –Selects data source to **HVALID** signal and **DOUT** bus.

The input signal selects one of the following:

'0' - Drive Base-Band data to LCD via **DOUT[9:2]**, Write pulse to **HVALID**

'1' - TC5747 data to LCD via **DOUT[9:2]** and to **HVALID**.

- **HLCD_WR#** – Write signal from system Host. It may not be exclusively for the LCD so the hlcd_cs_n needs to be taken into account when outputting the write signal to the LCD.
- **HLCD_CS#** – LCD chip select from system Host. Only **HLCD_WR#** pulses qualified by **HLCD_CS#** are passed on to the **HVALID** pin as Write pulse. It cannot be used instead of **hlcd_bb_n** since its hold timing may not be enough for data hold.

If there is a need to put the **DOUT** bus and the **HVALID** pin in tristate mode, the External-chip-select mode may be selected (in the **cs_mode** register of the CONT unit, address 0x108), where **DOUT[0]** pin is used as a chip-select input. Alternatively, the **enable_out_pvi** bit of the same register may be used to tri-state the interface pins on an image frame boundary.

In **CS#** mode (when the chip_select register is enabled) **HLCD_BB#** selects between:

- '**0**' - Drive TC data to output.
- '**s**' - Tri-State data output.

The chip_select register should be set before enabling the **PVI** output since there could be a contention if the chip drives a value on **DOUT** and the host drives another value.

5.1.2 VALIDH Functionality as Qualified Clock

The **VALIDH** pin may be configured to work as a **WRITE#** signal. In this mode, the qualify signal is multiplied by the clock signal. The polarity is programmable. The data is marked as valid only when the **VALIDV** pin is active. The data should be sampled on the trailing edge of the **VALIDH** pin.

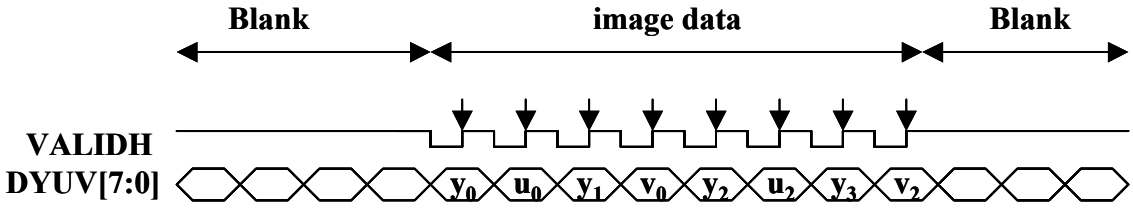


Figure 7: VALIDH as Qualified Clock, Active Low

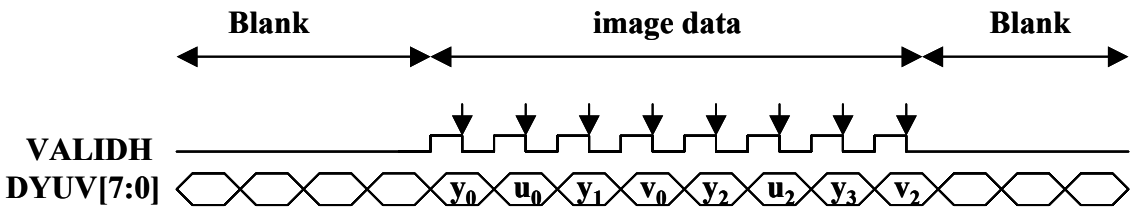


Figure 8: VALIDH as Qualified Clock, Active High

When working in this mode, two options are supported:

- **VALIDH** is the qualified clock signal; the **VCLKOUT** pin is stuck at zero.
- The qualified clock signal for "even" (0,2,4…) bytes is the **VCLKOUT** pin, **VALIDH** for "odd" (1,3,5…) bytes.

The second mode may be used when directly accessing an LCD controller via a 16-bit interface. The first qualify signal is used to latch the data on an on-board register, the second qualify signal is used as a "Write" signal for the LCD controller.

5.2 Host Interface

The System Host can perform read and write accesses to the TC5747 via a 16-bit parallel interface. A 16 bit parallel Host interface will enable high speed access by Base band host to the TC5747. Duration of program loading time and JPEG code reading and writing, two very high data volume processes, will be significantly shorter.

The parallel host interface operates in both I80 and M68 modes of operation.

5.2.1 Host Interface Operation

The host interface translates an external host access into four types of internal operation:

1. Internal write of register or memory
2. Internal read of register or memory content
3. Write to LCD via LCD interface
4. Read from LCD

The first two, internal write or read, produce internal 16-bit data, 12-bit address and a 1-cycle pulse of read/write signals.

The LCD access is translated into control signals to the **PVI** unit for direct interface with the LCD.

5.2.2 Host Interface Pins

The interface signals are listed in the table below:

Signal name	IO	Description
HDAT[15:0]	IO	Host Data for Write and Read operations
HADD / HLCD_RS	I	Address/Data select for TC5747 Register/Data select input to LCD, used when Host directly accesses the LCD
HWR_N / HSTROBE_N	I	Host Write signal for accessing the TC5747
HRD_N / HRDWR_N	I	Host Read signal for accessing the TC5747
HCS_N	I	Host Chip-select signal for accessing the TC5747
HLCD_CS_N	I	Host Chip-select signal for accessing the LCD

Table 6: Interface Signals

5.2.3 Host Protocol

5.2.3.1 Host Write Access

The 1 bit address differentiates between Address and Data. When a Write cycle is identified, and **HLCD_RS** is sampled low, the Host is loading the address register in the interface unit. This access is not translated into an access on the internal control bus. The sampled address is kept in the Host-interface unit until a write data cycle is received.

When a Write cycle is identified, and **HLCD_RS** is sampled high, the access is identified as a Host-Write access to one of the internal registers or memories, according to the internal address mapping.

At the end of the Host-Write access a write signal is activated for one clock cycle, along with the address (loaded with **HLCD_RS** sampled low and saved in an address register) and acquired data. The address register is incremented for support of auto-increment. If a data Write or Read cycle follows, the incremented address is used in the following access. The address is NOT incremented only if its 4 MS bits (bits [11:8]) are equal to the Memory-section prefix in the address mapping of the TC5747.

5.2.3.2 Host Read Access

A Host read access uses the last address that was written by the host, or incremented in a previous Host access.

The **HLCD_RS** pin is not sampled during a Host-Read access. A Read access with **HLCD_RS** sampled low is forbidden. A Host-Read access is always assumed to be a Host-Read access of an internal register or memory.

Two modes of Host-Read are supported. The **host_preread** bit in the TBD register selects between pre-read mode and normal read mode.

5.2.3.3 Normal Read Mode

When a **Host-Data-Read-access** is identified, an internal Register or Memory Read cycle is performed, and the resulting data is sent out on the Host bus data pins. See timing diagrams below.

5.2.3.4 Pre-Read Mode

At the end of a cycle of **Host-Address-Write-access**, the Host interface unit initiates a Register or Memory Read cycle. The data retrieved is saved in a register in the Host interface unit, and forced on the bus in any consecutive Host-Data-Read-access. An incoming Host-data-read-access initiates another Register or Memory Read cycle on the internal bus, predicting a following **Host-Data-Read-access**. This method allows for a very fast Host-interface access. However, care should be taken as the registers and memories actual Read cycle timing is a derivative of the actual Host Read access of the previous Host access. The Host should always initiate a **Host-Address-Write-access** before the first Host-Data-Read-access after Host-Data-Write-accesses.

LCD Access

Two LCD devices are supported by the TC5747-D0. The selection is done through the LCD_select register in the **CONT** unit. When the host performs a read access from the LCD, the Chip-select pin of the selected LCD is activated using the **LCD_CS1/2** output controls.

The Host access to LCD should include random logic only, so that Host access is still supported while the TC5747 clock is shut down when not in operation.

5.2.4 I80-type WRITE and READ access

The parallel host interface READ and WRITE accesses are described in Parallel Host interface AC Characteristics.

5.2.5 Host Access to LCD – Control Signals

When the Host accesses the LCD by activating the **HLCD_CS_N** input signal, the Host control, data and address (RS) pins are transferred to the LCD control interface asynchronously. The host is responsible for correct sequence for writing to, or reading from, the LCD. It is also the Host's responsibility to provide sufficient setup and hold of address and data to WRITE or READ signals for correct LCD access.

5.2.5.1 LCD Control Signal Configuration

The selected LCD is configured in the LCD_select register in the CONT unit.

Signal	Value							
		I80			M68			
HLCD_CS_N	1	0	0	0	0	0	0	0
HLCD_WR_N	X*	1	0	1	1	0	0	0
HLCD_RD_N	X*	1	1	0	1	1	0	1
HLCD_RS	X*	A	A	A	A	A	A	A
HLCDD[15:0]	X*	X*	Input = H2L	Output = L2H	Tri-state	x	Input = H2L	Output = L2H
LCD_CS#_N	LCD controls determined by TC5740	0	0	0	0	0	0	0
LCD_WR_N (VALIDH)		1	0	1	1	1	0	0
LCD_RD		1	1	0	1	1	0	1
DOUT[17:0]		Tri-state	Outp = H2L	Int = L2H	X*	Tri-state	Out = H2L	Int = L2H
LCD_RS	1	A	A	A	A	A	A	A
Notes			Host WR	Host RD			Host WR	Host RD

X* = Enter any value

Table 7: LCD Control Signal Configuration

For host Write, the Host data **HLCDD** is forced on the **DOUT** bus according to the LCD data configuration.

For host Read, the **DOUT** bus content is forced on the Host data HLCDD bus according to configuration.

When the Host does not access the LCD, the LCD_RS signal is controlled by the TC5747.

5.2.6 Host Access to LCD – Data formats

Several Data formats are supported for Host to LCD access.

5.2.6.1 18-bit LCD Access

The Host interface is 16-bits wide, while the LCD may be operating in 18-bit mode. There are two modes of conversion for command-type access to the LCD for support of different LCD devices. 16-bit data from the host (**RGB565**) is translated into 18 bit data (**RGB666**). TC5747 **RGB666** data is transferred directly to the LCD on **DOUT[17:0]**.

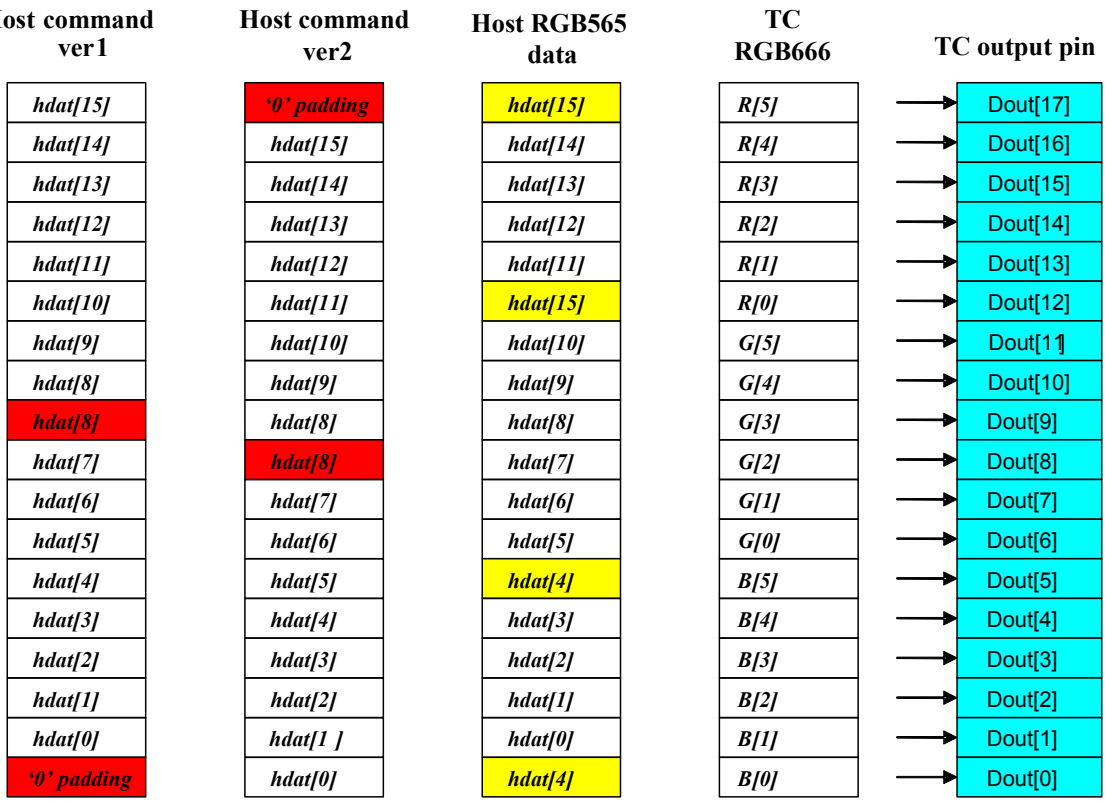


Figure 9: 18 Bit LCD Access

5.2.6.2 16-bit LCD Access

For 16 bit access to LCD, the Host 16-bit data is transferred directly to the LCD on **DOUT[17:10]** and **DOUT[8:0]**. **DOUT_9** and **DOUT_0** pins of the TC5747 are ignored.

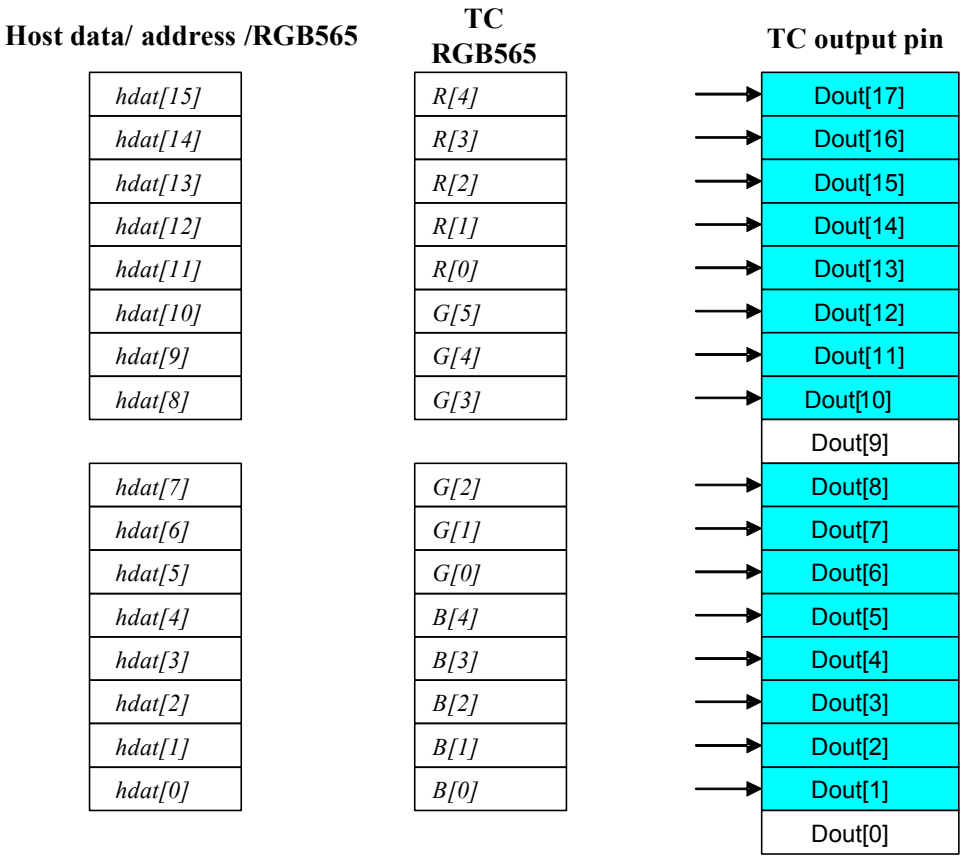


Figure 10: 16 Bit LCD Access

5.2.6.3 9-bit LCD access

For 9-bit LCD access, the host is responsible to send only 9-bit words to the LCD. TC5747 18-bit **RGB666** data is sent on two consecutive cycles on the **DOUT[8:0]** bus.

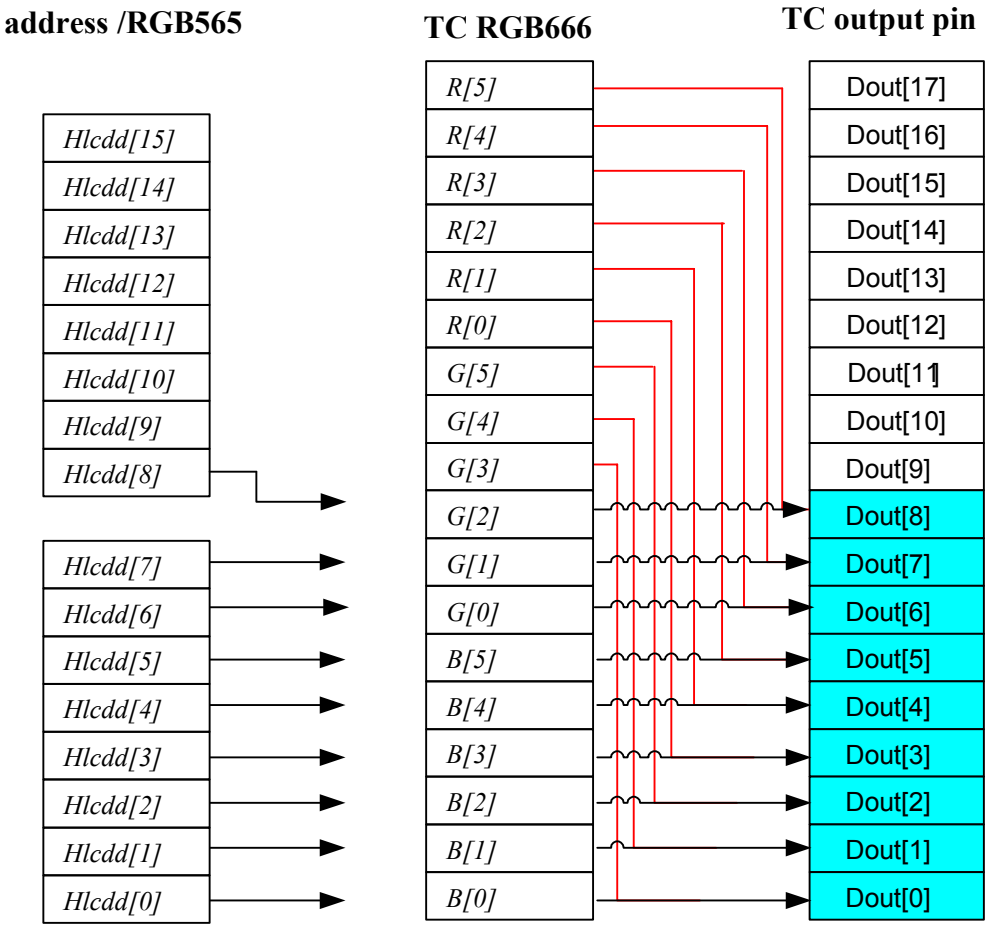


Figure 11: 9 Bit LCD Access

5.2.6.4 8 bit LCD access

For 8-bit LCD access, the host is responsible to send only 8-bit words to the LCD. TC5747 18-bit **RGB565** data is sent on two consecutive cycles on the **DOUT[8:1]** bus.

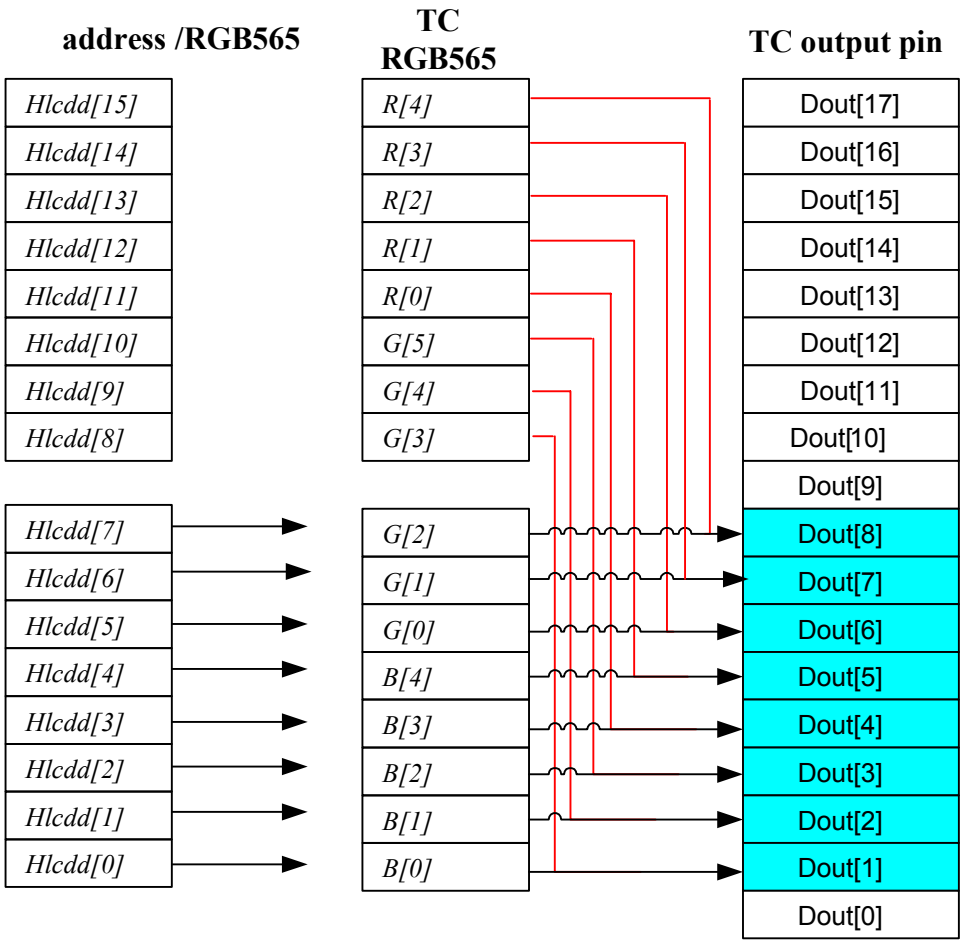


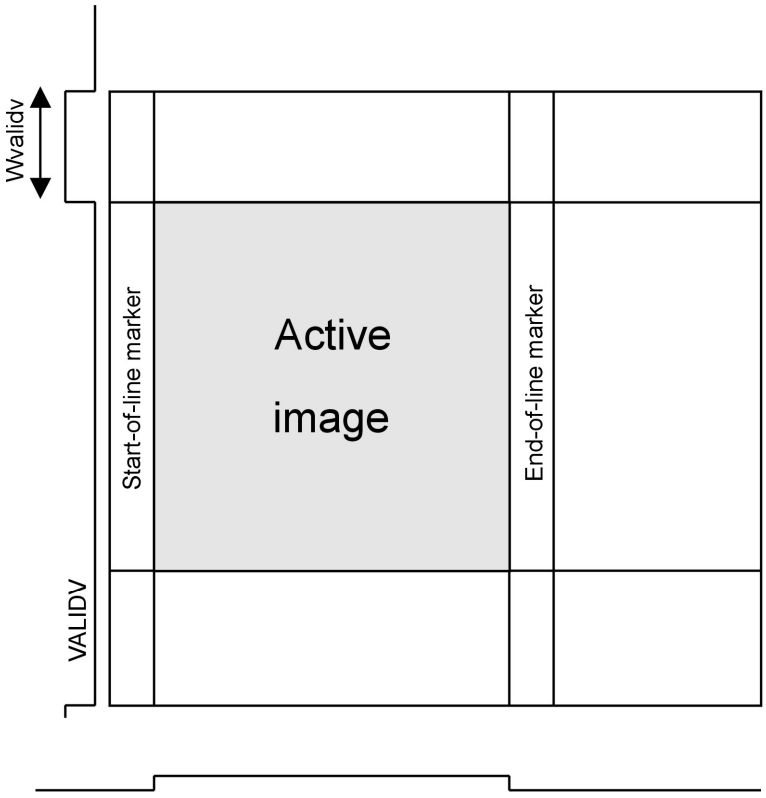
Figure 12: 8 Bit LCD Access

5.3 Parallel Video Interface (PVI)

The PVI generates the video output of the TC5747. The interface consists of a vertical frame-start signal and a 10-bit parallel data bus with clock and qualify signals. It supports parallel and serial modes of operation.

5.3.1 Parallel Mode of Operation

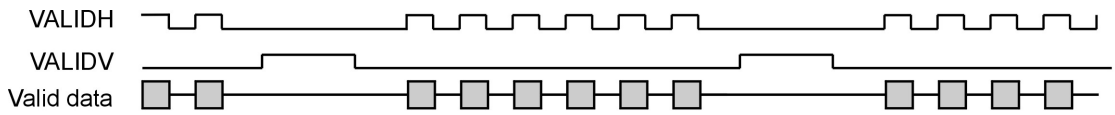
The PVI produces a clock signal (the **CLK_OUT** pin), a 10-bit data bus, **DOUT[9:0]** and qualifying signals that are synchronous to that clock. On each determining edge of **CLK_OUT**, a single data byte is transferred on the data bus, if qualified by the **VALIDH** signal.



Note: VALIDH is active during the shaded region

Figure 13: PVI Qualification Signal Timing

Valid data are qualified by the **VALIDH** signal. The **VALIDH** signal is activated only when image data is sent out on the parallel interface. It is inactive when dark lines are read, or during the vertical blank period. The **VALIDH** signal can be configured to qualify only the valid image data, or to qualify optional Start-of-line and End-of-line markers.



Note: Duration and polarity of VALIDV signal is programmable

Figure 14: Vertical and Horizontal Qualify Signals

The **DOUT[9:0]** bus carries either the Bayer grid data, the **YUV 4:2:2** output data, the **RGB** data (**RGB565**, **RGB666** or **RGB444**) or **JPEG** code according to the **TCIF_OUTPUT_FORMAT** host command.

- Bayer Grid data is left-justified.
  - 10-bit Bayer resides on **DOUT[9:0]**
  - 9-bit Bayer resides on **DOUT[9:1]**
  - 8-bit Bayer resides on **DOUT[9:2]**
- The 8-bit YUV data resides on the **DOUT[9:2]** output pads, annotated **DYUV[7:0]**.
- The 8-bit **RGB565** or **RGB444** data resides on the **DOUT[9:2]** output pads.
- The 9-bit **RGB666** data resides on the **DOUT[9:1]** output pads.

RGB666 can also be transmitted using 3 clock cycles on the **DOUT** bus

- The 6-bit **RGB666** (3-word mode) data resides on the **DOUT[9:4]** output pads.
- The 8-bit JPEG data resides on the **DOUT[9:2]** output pads.

For 2-word output formats, **RGB444**, **565** and **666**, the data is packed into 2 words:

- **RGB444**: {Red[3:0],Green[3:0]}
  {Blue[3:0], 0x0}
- **RGB565**: {Red[4:0], Green[5:3]}
  {Green[2:0], Blue[4:0]}
- **RGB666**: {Red[5:0], Green[5:3]}
  {Green[2:0], Blue[5:0]}

For 3-word RGB 666 output formats, the data is sent out as 3 words:

- **RGB666**: Red[5:0],
  Green[5:0]
  Blue[5:0]

The active line timing is depicted in the diagrams below. The diagram below shows the active data line where the optional Start-of-line and End-of-line markers are omitted:

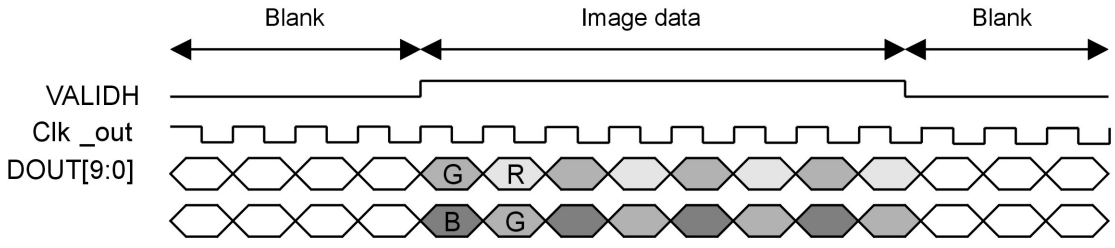
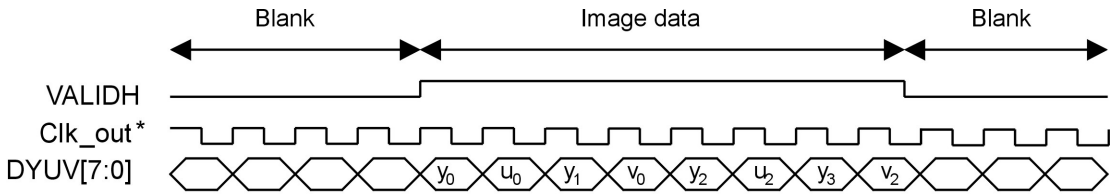


Figure 15: PVI Bayer Output Format



Note: For YUV output format, the Clk_out* rate is double the rate of the Bayer output format

Figure 16: PVI YUV Output Format

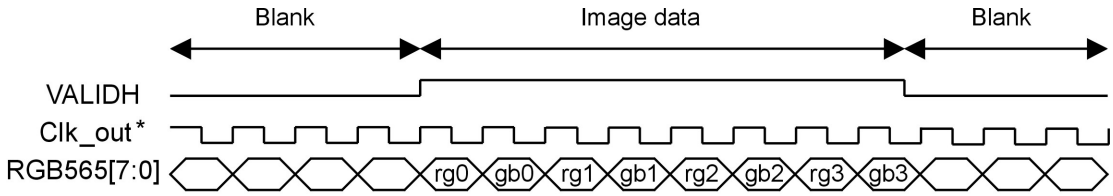


Figure 17: RGB 565 Output on Parallel Video Output Interface

The output clock rate for **YUV** or 2-word RGB output is double the output clock rate for Bayer output. The output clock rate for 3-word **RGB666** is double the output clock rate for **YUV** output.

When sending out the data in Bayer-grid format, a “RED” line will always be the first line in the frame.

5.3.2 External Chip-Select

A mode may be selected where the data bus may be floated or driven according to an external chip-select input controlled by the **CSDAT#** pin. The **CSDAT#** pin is active-low, i.e. when low the **DOUT[9:1]** or **DYUV[7:0]** bus pins are driven, and when **CSDAT#** is high these outputs are put in a tri-state position. The **VALIDH**, **VALIDV** and **VCLKOUT** pins are not affected by the **CSDAT#** pin.

5.3.3 Qualified Clock Mode

The TC5747 supports a mode where the **VCLKOUT** pin is not active when there is no active data on the parallel interface.

5.3.4 VALIDH Configured as WR#

The **VALIDH** pin may be configured to work as a WRITE signal for applications requiring that the video data is being written into a device. The polarity is programmable. The data is marked as valid only when the **VALIDV** pin is active. The data should be sampled on the trailing edge of the **VALIDH** pin.

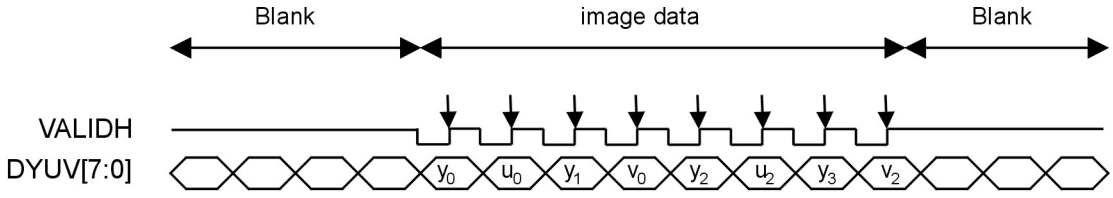


Figure 18: VALIDH as a Write signal, Active Low

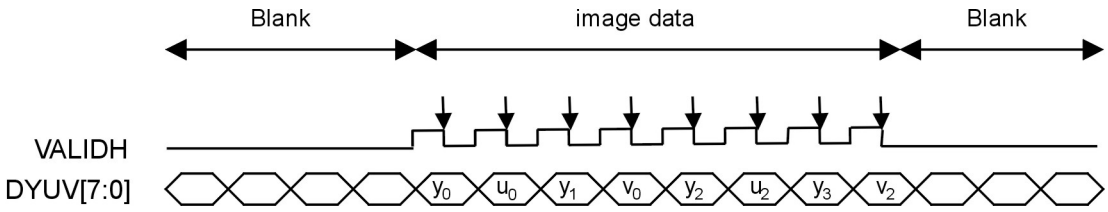


Figure 19: VALIDH as a Write Signal, Active High

5.3.5 Frame-Rate Control

The CONT unit uses the **c_outframe** signal to control the frame rate. It enables or disables the output of a full frame. When output is disabled, the **VALIDH** and **VALIDV** output signals are stuck at an inactive state. The data output bus holds the background value throughout the disabled frame time.

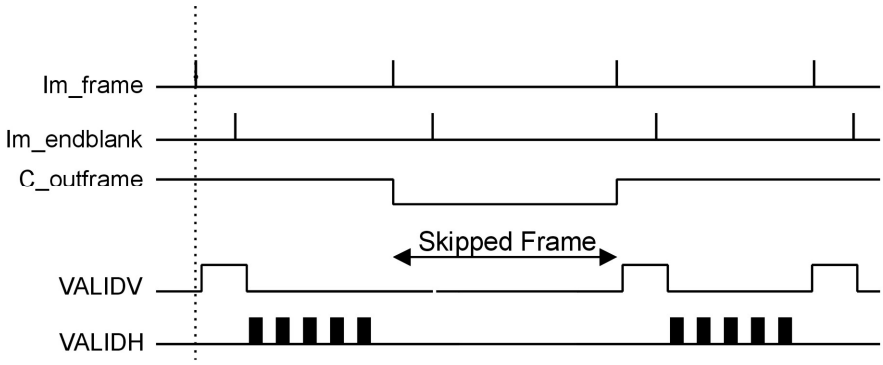


Figure 20: Frame Rate Control

The **c_outframe** signal changes on **im_frame**. The decision if to send or skip the new frame is made on the clock cycle that follows the **im_frame signal**.

5.3.6 Data

5.3.6.1 General

The type of data (**Bayer, RGB, YCrCb 4:2:2** or **JPEG**) output from the TC5747 is programmable through the TC5747 programming registers, using host commands. The type of data also defines the frequency of the TC5747's output clock signal.

5.3.6.2 Bayer Output

When **Bayer** output is selected, the data volume is one byte per pixel.

If Data-Markers are added, 8 more bytes per line must be taken into consideration in the image buffer that is allocated for the application.

There are two types of **Bayer** data lines:

- "RED" lines - lines that carry Green and Red Bayer components. The Green and Red data bytes are interleaved. The even numbered bytes (0, 2 to 2n) are Green, the odd numbered bytes (1,3 to 2n+1) are Red.
- "BLUE" lines - lines that carry Blue and Green Bayer components. The Green and Blue data bytes are interleaved. The even numbered bytes (0, 2 to 2n) are Blue, the odd numbered bytes (1,3 to 2n+1) are Green.

When sending out the data in **Bayer**-grid format, a "RED" line will always be the first line in the frame.

5.3.6.3 YCrCb 4:2:2 Output

When **YCrCb 4:2:2** output is selected, the data volume is two bytes per pixel. If Data-Markers are added, 8 more bytes per line must be taken into consideration in the image buffer that is allocated for the application.

The data in the **YCrCb 4:2:2** output format is ordered in several configurations, according to the setting in the **Color_order** bits in the video output control registers:

00 - SOL, Y_0, U_0, Y_1, V_0, Y_2, U_2, Y_3, V_3, to Y_{n-2}, U_{n-2}, Y_{n-1}, V_{n-2}, EOL

01 - SOL, Y_0, V_0, Y_1, U_0, Y_2, V_2, Y_3, U_3, to Y_{n-2}, V_{n-2}, Y_{n-1}, U_{n-2}, EOL

10 - SOL, U_0, Y_0, V_0, Y_1, U_2, Y_2, V_3, Y_3, to U_{n-2}, Y_{n-2}, V_{n-2}, Y_{n-1}, EOL

11 - SOL, V_0, Y_0, U_0, Y_1, V_2, Y_2, U_3, Y_3, to V_{n-2}, Y_{n-2}, U_{n-2}, Y_{n-1}, EOL

5.3.6.4 RGB565 Output

When **RGB565** output is selected, the data volume is two bytes per pixel. Output data are transmitted in the same manner and frequency as the **YCrCb 4:2:2** output format, on **DOUT[9:2]**. The first byte of each pixel carries 5 bits of the Red color component, and the 3 MSB of the Green. The second byte carries the 3 LSB of the Green color component, and the 5 bits of the Blue color component.

5.3.6.5 RGB666 Output

When **RGB666** output is selected, the data volume is two 9-bit "words" per pixel. Two modes can be selected for **RGB666** data.

Two-transfers Mode

When **RGB666** output is selected, the data volume is two 9-bit "words" per pixel. No extra pixels are required beyond the **VGA/QVGA** size.

The output data is transmitted in the same manner and frequency as the **YCrCb 4:2:2** output format, on **DOUT[9:1]**. The first byte of each pixel carries 6 bits of the Red color component, and the 3 MSB of the Green. The second byte carries the 3 LSB of the Green color component, and the 6 bits of the Blue color component.

Three-transfers Mode

When three-transfer **RGB666** output is selected, the data volume is three 6-bit "words" per pixel. No extra pixels are required beyond the **VGA/QVGA** size.

The output data is transmitted on **DOUT[9:4]**. The order of transmission is Red, Green and Blue.

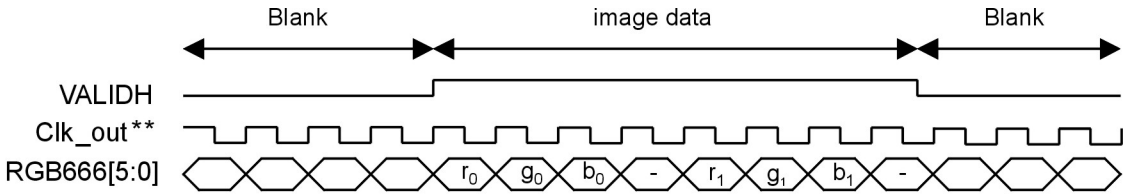


Figure 21: RGB666 Three-transfers Mode

The output data is transmitted in the double the frequency as the **YCrCb 4:2:2** output format, 3 consecutive clock cycles carry valid data, and the fourth clock cycle is skipped. No valid data is active on this clock cycle, and **VALIDH** is inactive.

5.3.6.6 RGB444 Output

When **RGB444** output is selected, the data volume is two bytes per pixel. The output data is transmitted in the same manner and frequency as the **YCrCb 4:2:2** output format, on **DOUT[9:2]**. The first byte of each pixel carries 4 bits of the Red color component, and the 4 bits of the Green. The second byte carries the 4 bits of the Blue color component on **DOUT[9:6]**, and is padded by 6 zeros on **DOUT[5:0]**.

5.3.6.7 JPEG Output

When **JPEG** output is selected, the compressed code is sent out on the parallel data bus, qualified by **VALIDH**. To support ancillary data format as defined in the **ITU 656** and **ITU 1364** standards, an optional ancillary data packet header may be added before each consecutive packet of bytes of **JPEG** code. A Checksum byte may be added following the data bytes. The last "packet" of **JPEG** code may contain less than packet number of bytes, and the "payload byte" in the packet header reflects the actual size.

5.3.7 Data Markers

Extra optional data markers are inserted at the beginning and end of each image line. The user may select between TransChip-specific markers, and markers that conform to the **ITU 656** standard.

5.3.7.1 TransChip Markers

A "Timing signal" or Marker is defined in the **ITU 656** standard as a sequence of four bytes, the first three bytes holding reserved values of **FF 00 00**, and the fourth byte composed of a collection of bits whose function is defined in the standard. The TransChip markers utilize the format of the markers as defined in the standard, but redefines two bits in the last marker byte.

There are four types of markers:

- Start of First Line marker – This marker precedes the data of the first line in a frame.
- Start of Line Marker - This marker precedes the data of each line in a frame, except for the first line. When Bayer output mode is selected, bit #5 of the marker content differentiates between a "red" line and a "blue" line (0 and 1 respectively).
- End of Last Line Marker - This marker immediately follows the data of the last line in a frame.
- End of Line Marker - This marker immediately follows the data of each line in a frame, except for the last line.

All markers are 4 bytes long. The first 3 bytes of all markers are identical, and annotate the marker header. The marker content is "**FF 00 00 xy**", where xy is different for each marker type.

Marker	Marker Header			Marker content DOUT[9:2] / DYUV[7:0]
SOFL	0xFF	0x00	0x00	0xC7
SOLR (**YCrCb** or "red" line)	0xFF	0x00	0x00	0x80
SOLB ("blue" line)	0xFF	0x00	0x00	0xAB
EOLL	0xFF	0x00	0x00	0xDA
EOL	0xFF	0x00	0x00	0x9D

Table 8: TransChip Markers

Bits [7:4] of the Marker-content byte carry the marker information:

- Bit [7] – Always 1 to avoid 0x00 code
- Bit [6] - Special frame markers (start-first-line/end-last-line)
- Bit [5] – For Bayer – line "color" (0 for Red, 1 for Blue)
- Bit [4] – End/Start bit, 0 for Start-of-line marker, 1 for End-of-line

Bits [3:0] of the Marker-content byte provide parity check capability, allowing for one-bit errors to be corrected, and two-bit errors to be detected, according to ITU-656-4 Standard.

5.3.7.2 ITU 656 Markers

A “Timing signal” or Marker is defined in the **ITU 656** standard as a sequence of four bytes, the first three bytes holding reserved values of **FF 00 00**, and the fourth byte composed of a collection of bits whose function is defined in the standard.

Bits [7:4] of the Marker-content byte carry the marker information:

- Bit [7] – Always 1 to avoid 0x00 code
- Bit [6] – F – field 0 or field 1
- Bit [5] – V - blank or active video line indication (0 for active, 1 for blank)
- Bit [4] – H - End/Start bit, 0 for Start-of-line marker, 1 for End-of-line

Bits [3:0] of the Marker-content byte provide parity check capability, allowing for one-bit errors to be corrected, and two-bit errors to be detected, according to **ITU-656-4** Standard.

When adhering to the bit-definition of the **ITU-656** standard, there is a need to distinguish between consecutive frames, either by inserting markers on at least one blank line between frames, or by toggling the field bit on every frame start.

The **PVI** supports the following options.

Marker	Field	Marker Header			Marker content DOUT[9:2] / DYUV[7:0]
SAV - active	0	0xFF	0x00	0x00	
SAV - blank	0	0xFF	0x00	0x00	
EAV - active	0	0xFF	0x00	0x00	
EAV - blank	0	0xFF	0x00	0x00	
SAV - active	1	0xFF	0x00	0x00	
SAV - blank	1	0xFF	0x00	0x00	
EAV - active	1	0xFF	0x00	0x00	
EAV - blank	1	0xFF	0x00	0x00	

Table 9: ITU 656 Markers

5.3.7.3 Avoiding Marker Emulation

When the Send-Markers mode is enabled, care has to be taken to avoid marker-emulation inside the data itself.

- When **YCrCb 4:2:2** output mode is selected, there is no contention between marker header contents and the transmitted data, because the Y data values are limited to the range of 16-235, and the **Cr** and **Cb** data values are limited to the 16-240 range. **0x00** and **0xFF** values never occur inside the image data values.
- When Bayer output is selected, the data has to be modified, so that 0xFF and **0x00** values are removed from the data content, and replaced by their nearest allowed values (0xFE and **0x01** respectively).
- When **RGB565** output is selected, the data has to be modified, as in the case of the Bayer output. **0xFF** and **0x00** values are removed from the data content, and replaced by their nearest allowed values.
  - The first byte of **RGB565** is replaced by **0xF7** or **0x08**.
  - The second byte of **RGB565** is replaced by **0xFE** or **0x01**.
- When **RGB666** output is selected, the data has to be modified, as in the case of the Bayer output. **0xFF** and **0x00** values are removed from the data content, and replaced by their nearest allowed values.
  - TBD
- When **RGB444** output is selected, the data has to be modified, as in the case of the Bayer output. **0xFF** and 0x00 values are removed from the data content, and replaced by their nearest allowed values.
  - The first byte of **RGB444** is replaced by **0xEF** or **0x10**.
  - The second byte of **RGB444** is replaced by **0xF0** or **0x01**.
- JPEG code cannot be modified. However, there is no need for any modification if Ancillary format is used for JPEG transmission.

5.3.8 Ancillary Data Format

The **ITU-1364** defines the ancillary data format that may be transmitted during blank lines of video, as defined in the **ITU 656** standard.

Immediately following a blank line “Timing signal”, an ancillary data packet may be added. If an ancillary data header is detected instead of the blank video data, as defined by the standard (a sequence of 0x80 0x10), ancillary data can be extracted.

An ancillary data header is defined as a sequence of 6 bytes:

0x00 0xFF 0xFF ID1 ID2 Data-SIZE/4

The header is followed by data (4 to 252 bytes).

A Check-sum byte follows the data as the last byte of the packet.

The ancillary header and checksum are optionally produced by the JPEG unit. The **PVI** does not differentiate between header and JPEG code.

5.3.9 Serial Output Mode

The Transmitted data size for Serial output mode is 8 bits per transmitted "word". Bayer output provides 8 bits per pixel, and **YUV** and **RGB** output provides 16 bits per pixel. The bytes are sent with the MSB first, LSB last. During continuous transfer, the MSB of byte N immediately follows the LSB of byte (N-1).

The TC5747 serial output interface can be configured to work in two different modes:

- Clock-qualify mode – A two wire interface with clock and output data signals. The TC5747 acts as a master of the interface. It activates the serial clock signal when there is valid data to be sent out.
- **SSI** mode – A three wire interface, with clock, output data and frame signals. The TC5747 acts as a master of the interface, producing all three signals.

5.3.9.1 Clock-Qualify Mode

The serial interface consists of two pins:

- DSCLK – Data Serial Clock output pin –1X or 2X the rate of the data output TC5747 generates DSCLK signal from its general clock input signal.
- **DSDAT** – Serial Data output pin.

The TC5747 acts as a master of the interface. It activates the serial clock signal when there are valid data to be sent out.

- Serial Clock Polarity – Clock is inactive at zero
- Serial Clock Phase – Drive data on positive edge of Serial clock signal (**DSCLK/2**), latch on negative edge

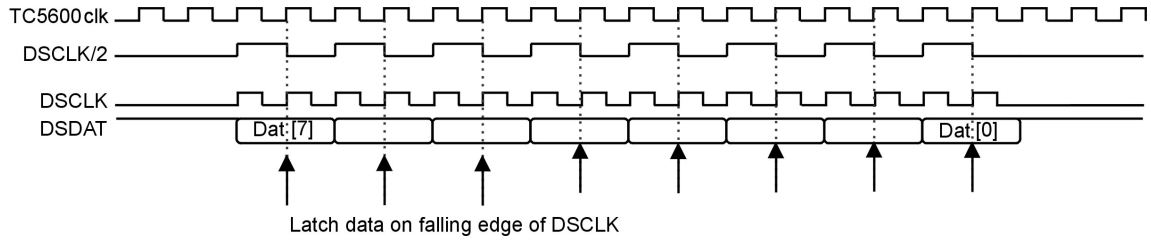


Figure 22: Serial Data-Out Interface – x2_clk_out = 1

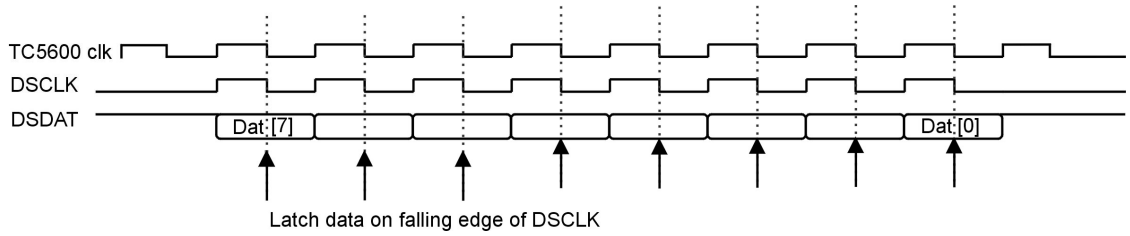


Figure 23: Serial Data-Out Interface – x2_clk_out = 0

5.3.9.2 SSI Mode

The serial interface consists of three pins:

- **DSCLK** – Data Serial Clock output pin
- **DSDAT** – Serial Data output pin.
- **DSFRM** – Frame signal in early-frame mode

The TC5747 acts as a master of the interface. It activates the Frame signal one clock period before there is valid data to be sent out. Transfer datum size configurable. There are three options:

- Transfer datum size is a single byte.
- Transfer datum size is a single line (size is according to output image size and output mode).
- Transfer datum size is a single image. This configuration can be used only in a mode that combines the **SSI**-mode with the clock-qualify mode.

DSFRM Signal

The **DSFRM** signal notifies of a transfer of a complete data unit. There are three configurations, as described below.

Single Byte Transfer Mode

The 8 bits of the transfer byte are sent out on the eight following effective edges of the **DSCLK** signal. When the last bit of the byte is sent out, the **DSFRM** signal may be active again. If it is active, the following byte transfer begins on the next effective edge of **DSCLK**.

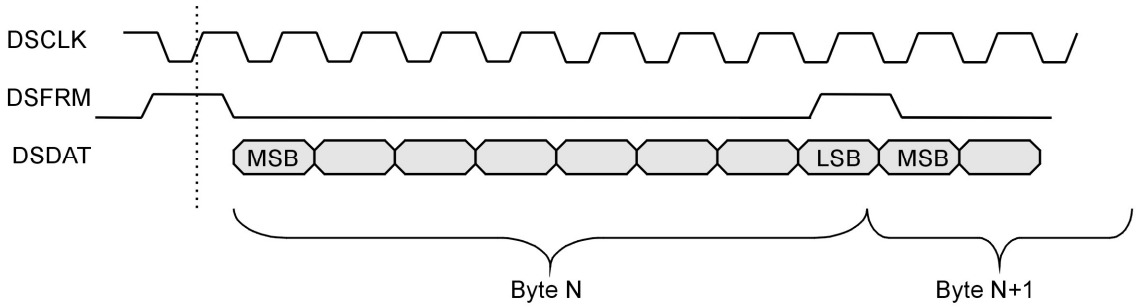


Figure 24: Single Byte Transfer Mode

Image-line Transfer Mode

In this mode, **DSFRM** is activated one clock before the continuous transfer of a complete image line. Transfer size should be configured on the receiving side according to the image line size, taking into consideration the **SAV** and **EAV** markers, if used.

Frame Transfer Mode

In this mode, the **DSFRM** signal is activated once in a frame, one clock cycle before the first byte of the image is transferred out.

The **DSFRM** signal duration is also configurable, to be of one clock cycle duration, or to be active until the last byte of data in the transfer is transmitted. The second mode can be used to generate an interrupt inside the receiving device, once the complete data has been transferred.

DSCLK Output

The **DSCLK** output can be configured to be continuous or gated. The gated option should be used when **DSFRM** is in the Frame-transfer mode.

5.4 Serial Video Interface

The TC5747 Serial Video interface unit is identical to the PVI unit described above, with two exceptions:

- Supports only serial interface
- Support also **SSI** input of data. The data input is controlled through the I^2C. The addition of input direction provides a high speed input serial interface for decompression of JPEG images.

5.5 I^2C Serial Interface

5.5.1 Overview

The I^2C interface is a two-wire bi-directional serial bus. The TC5747 can operate as a slave device only.

Both wires (**SCL** and **SDA**) are connected to a positive supply via a pull-up resistor, and when the bus is free both lines are high. The output stage of the device must have an open-drain or open collector type IO cell so that a wired-AND function between all devices that are connected on the bus can be performed.

Each device is recognized by a unique 7-bit address. The address allocated to TC5747-B0 is **0x47.** When performing write operations, add 0 to the LSB to get **0x8E**. For a Read operation add **1** to the LSB to get **0x8F**.

To summarize:

Address	I^2C Write	I^2C Read
0x47	0x8E	0x8F

Note: Some operating systems automatically add the 1 or 0 bit to the 7 bit address. The address for the TC5747-A0 is **0x47**.

A control of the byte order in I^2C transactions is provided through setting a register.

5.5.2 Mode of Operation

The bus master, typically the host **DSP**, initiates an access to the TC5747 device. The bus master activates a START condition, and passes the address of the requested device along with the type of access (read or write bit – the MSB or the start byte). The requested device replies with an acknowledge (ACK). The host can then perform as many transactions as it wishes, until the host activates a STOP condition. The bus is considered free after the STOP condition.

The data on the **SDA** pin must be stable during the high period of the clock (**SCL**) as shown in the figure below. Only the host may change the data while **SCL** is high. A high-to-low transition marks a START condition, and a low-to-high a STOP condition.

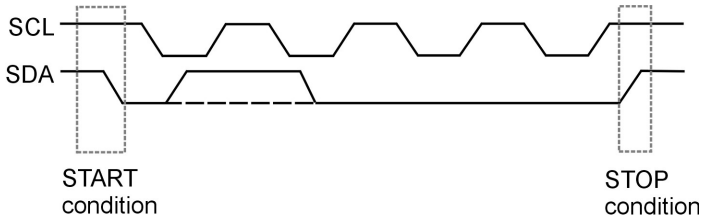


Figure 25: I²C Interface START and STOP Conditions

The master device activates a **START** condition, and sends the first byte of data that contains the 7-bit address, and a direction bit (**R/W#**, 1 for read, 0 for write). The addressed device answers by pulling down the SDA line as acknowledge procedure.

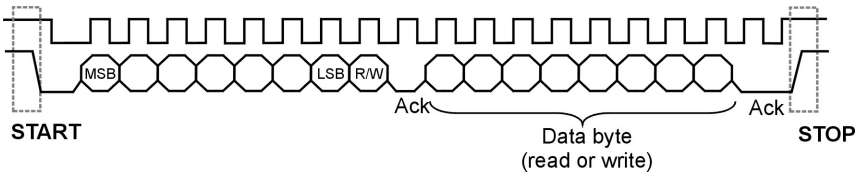


Figure 26: I²C Protocol

The TC5747 expects the first two bytes after the address byte to be the register address of the first register that is to be read or written by the host. Programming is done in host commands level which is translated into a series of register level commands.

When writing registers to the TC5747, the following bytes are data bytes. The data for each READ or WRITE access is two bytes long. The TC5747 performs auto increment until the STOP condition is identified. Auto increment is not performed when the initial address is in the address space that is allocated to the On-Chip-Memories. This address space is reserved for tables, where multiple bytes are written to a single address.

When reading registers from the TC5747, the register address (2 bytes) should be followed by a repeated START condition, device address, and **R/W#** bit equal to 1, to change mode from write (address) to read (data).

The sequence of loading or reading registers is described in the figure below.

- The colored boxes represent host-to-slave data transfer.
- The clear boxes represent slave-to-host data transfer.

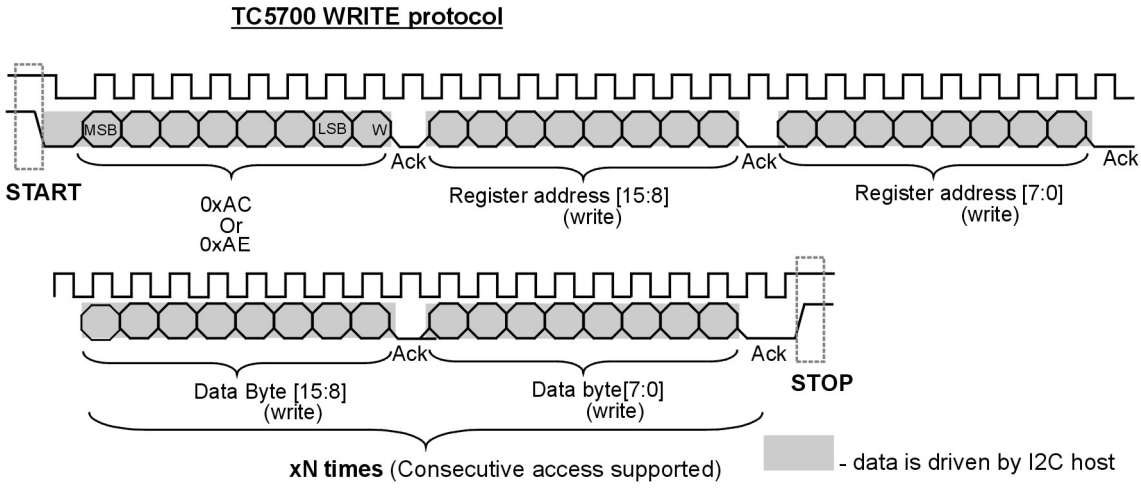


Figure 27: I^{2}C Host-Write Access

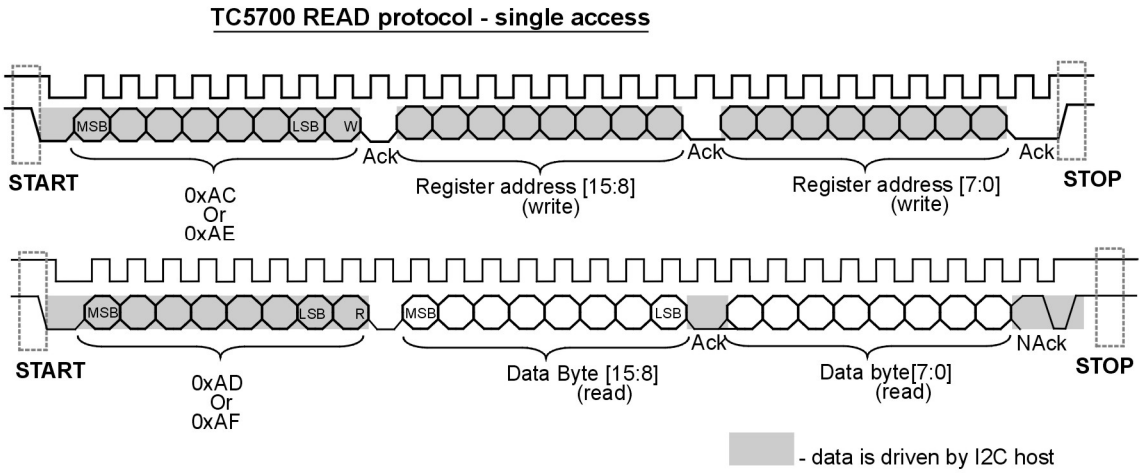


Figure 28: I^{2}C Host-Read Access

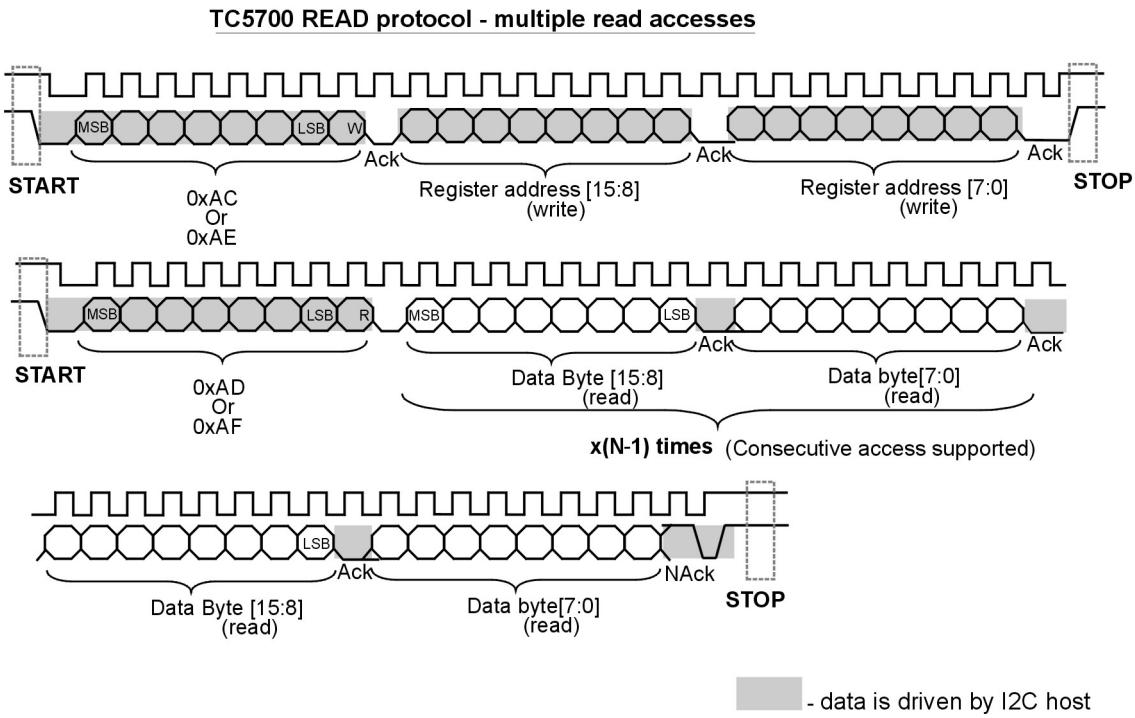


Figure 29: I^{2}C Host-Read Multiple (N) Accesses

The host should activate the STOP condition if a direction change is needed.

6. High Level API Programming

All TC5747 series products come with a flexible software API (Applications Program Interface) for integration of the product and interfacing it to a wide range of hosts. The API is based on a set of defined host commands.

The TC5747 is controlled by an embedded microcontroller. The microcontroller runs the firmware that is supplied by TransChip. The microcontroller receives the host commands, and executes them to perform various camera control functions.

Refer to the *TC5747 Programmer's Reference* guide for a list of available host commands, a detailed description on how to load the TC5747 firmware and check its status and how to read and write specific registers.

6.1 Firmware Loading

The microcontroller firmware (program) may be loaded through the host interface. (When using I2C or UART for control, firmware is loaded either using the I^2C interface or the UART interface). Once the program is loaded, the microcontroller sets the registers and controls the entire chip according to the firmware preset defaults and according to host commands which the microcontroller receives through the control interfaces.

7. AC/DC Specifications

The TC5747 chip excels in low power consumption

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max
V_{DD}	DC supply Voltage		4.0V
T_A	Storage Temperature	-30	70°C

Table 10: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Symbol	Parameter	Min	Max
V_{DD}	DC supply Voltage – 2.8V nominal	2.52	3.08V
T_A	Operating Temperature	-10	60°C

Table 11: Recommended Operating Conditions

7.3 DC Electrical Characteristics

Symbol	Characteristic	Condition	Specifications		
			Min	Typ	Max
VIH[1]	Input Hi-Volt	**VDD**=2.8V;Temp=25ºC	2.0V		
VIH[2]	Input Hi-Volt	**VDD**=2.8V;Temp=25ºC			
VIL[1]	Input Low-Volt	**VDD**=2.8V;Temp=25ºC			0.8V
VIL[2]	Input Low-Volt	**VDD**=2.8V;Temp=25ºC			
VOH	Input Hi-Volt	**VDD**=2.8V;Temp=25ºC	2.4V		
VOL	Input Low-Volt	**VDD**=2.8V;Temp=25ºC			0.4V
IOL		**VOL**=0.5*VDD;Temp=25ºC		13.3mA	
IOH		**VOH**=0.5*VDD;Temp=25ºC		19.4mA	
IDDmax	Supply current in working conditions	**VDD**=2.8V;Temp=25ºC **VGA** mode, 15 fps		15mA TBD	
Il/Ioz	Input leakage/ Output tristate leakage			+/- 1uA	+/- 10uA

Table 12: DC Electrical Characteristics

1 - All pins except **clk_in**
2 - **clk_in**

7.4 Parallel Video Output Clock Qualified Mode AC Characteristics

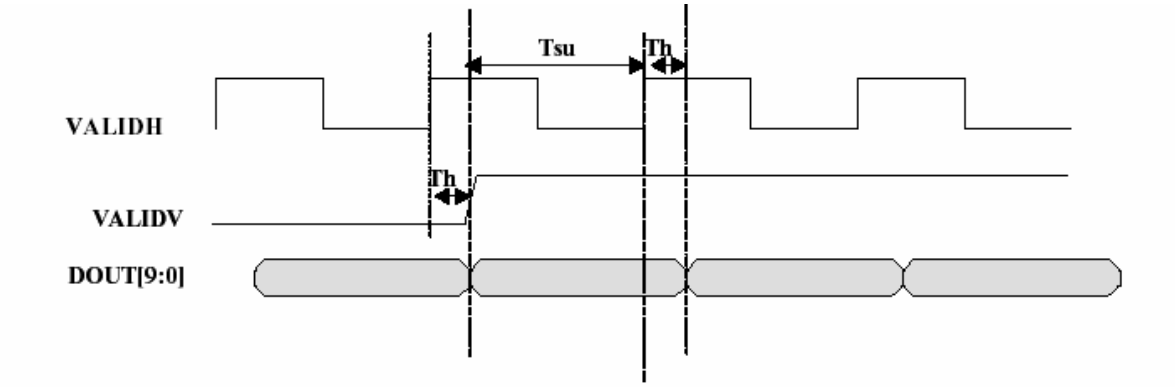


Figure 30: Parallel Video Output Clock Qualified Mode

Parameter	Description	Specifications		Units
		Min	Max	
Tsu	Data setup before effective edge of **VALIDH**	150	-	ns
Th		25	-	ns

Table 13: Parallel Video Output Clock Qualified Mode AC Characteristics

* Results depend on device frequency and mode. The results in this table are for 32MHz, **PVI CLK = clk_in.**

7.5 Parallel Video Output Camera Interface Mode AC Characteristics

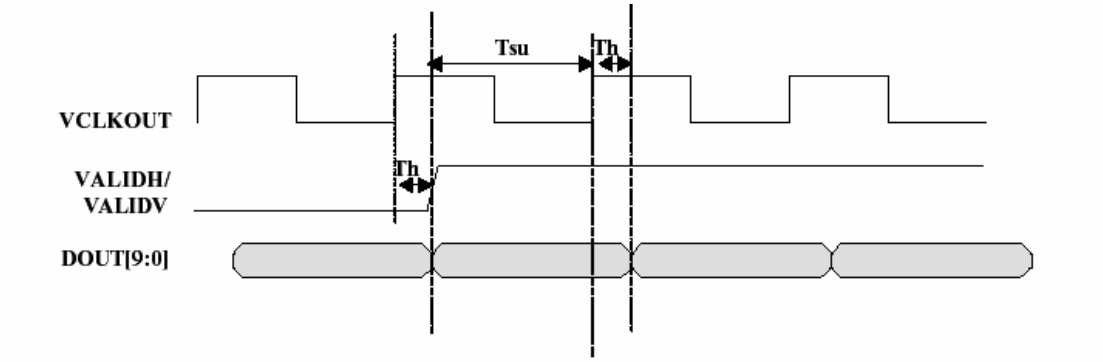


Figure 31: Parallel Video Output Camera Interface Mode

Parameter	Description	Specifications		Units
		Min	Max	
Tsu	Data setup before effective edge of **VCLKOUT**	150	-	ns
Th		25	-	ns

Table 14: Parallel Video Output Camera Interface Mode AC Characteristics

* Results depend on device frequency and mode. The results in this table are for 32MHz, **PVI CLK = clk_in.**

7.6 Parallel Host interface AC Characteristics

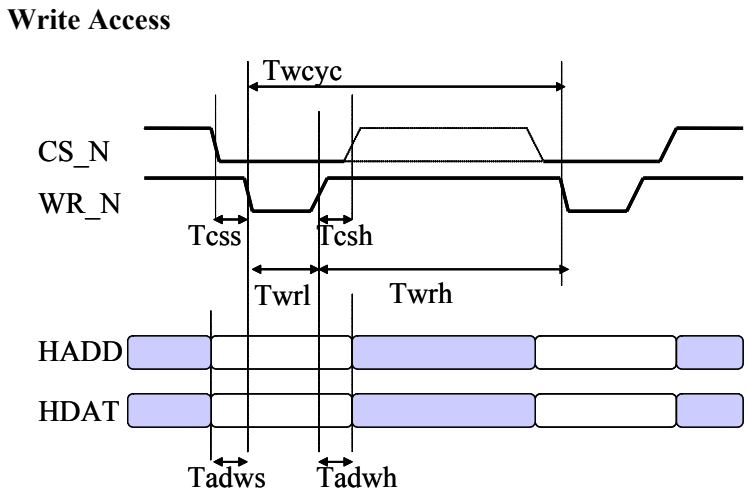


Figure 32: I80-type Write Access

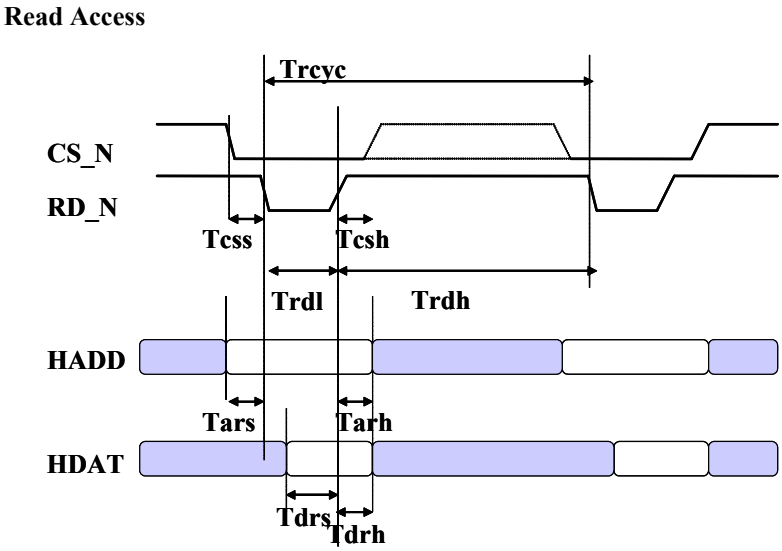


Figure 33: I80-type Read Access

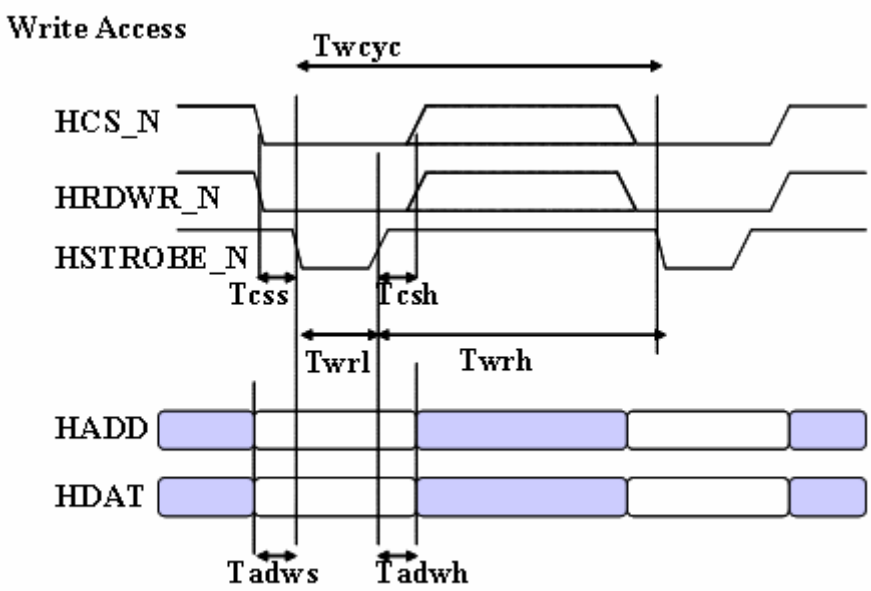


Figure 34: M86-style Write Access

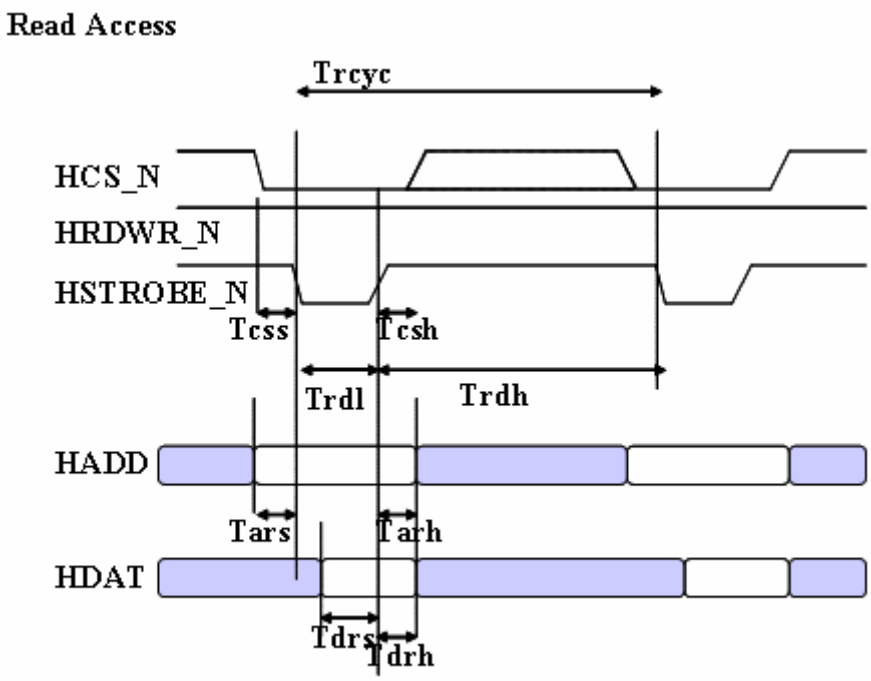


Figure 35: M86-style Read Access

The timing parameters of the Host access are given in the table below

Timing Parameter	Symbol	Min	Max	Units	Notes
Chip-select setup/hold to WR_N / RD_N	**Tcss** **Tcsh**	5		nsec	
Host-Write Cycle duration	**Twcyc**	5***Tcyc**		nsec	**Tcyc** is internal clock cycle duration
Write signal active low	**Twrl**	3***Tcyc**		nsec	
Write signal high between consecutive cycles	**Twrh**	2***Tcyc**		nsec	
Setup of address, data to fall of write signal	**Tadws**	5		nsec	
Hold of address, data to rise of write signal	**Tadwh**	0		nsec	
Minimum delay between READ and WRITE	**Twr_min**	2***Tcyc**		nsec	
Host-Read Cycle duration	**Trcyc**	9***Tcyc**		nsec	Normal Read Mode
		5***Tcyc**		nsec	Pre Read Mode
Read signal active low	**Trdl**	7***Tcyc**		nsec	Normal Read Mode
		7***Tcyc**		nsec	Pre Read Mode
Read signal high between consecutive cycles	**Trdh**	2***Tcyc**		nsec	
Setup of address to fall of write signal	**Tars**	5		nsec	
Hold of address to rise of write signal	**Tarh**	0		nsec	
Setup of output data to rising edge of READ signal / Strobe	**Tdrs**	2***Tcyc** – IO delay			
Hold of output data to rising edge of READ signal / Strobe	**Tdrh**	0			
Tri-stating of output data to rising edge of READ signal / Strobe	**Tdtri**		10	nsec	

Table 15: Timing Parameters

7.7 Parallel Video Output Interface AC Characteristics

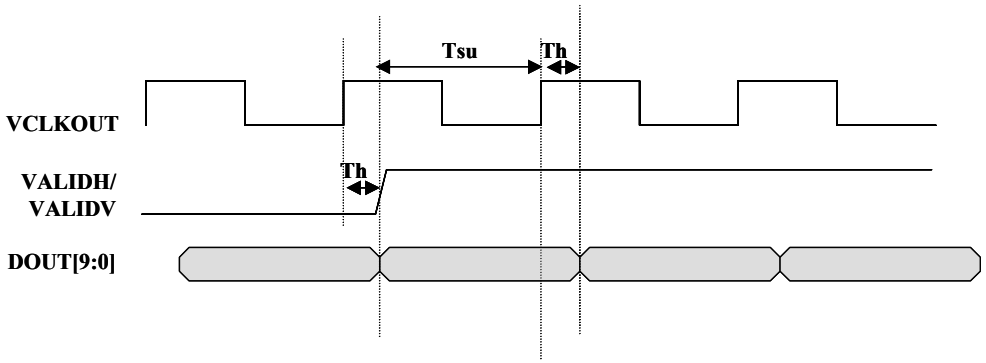


Figure 36: Parallel Video Output Interface Signals

Parameter	Description	Min	Max	Units
Tsu	Data setup before effective edge of **VCLKOUT**	150	-	nsec
Th		25	-	nsec

Table 16: Parallel Video Output Interface AC Characteristics

7.8 Serial Video Output Interface AC Characteristics

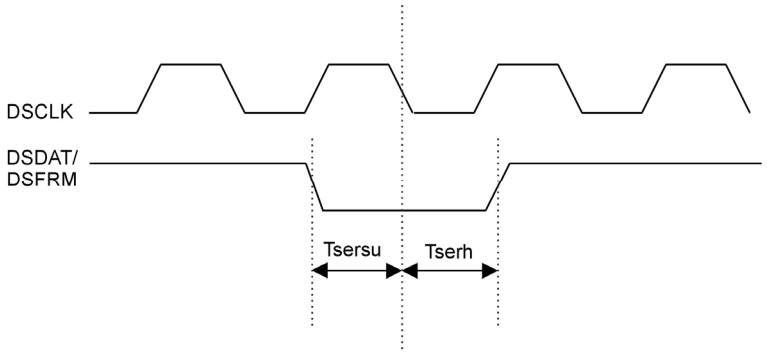


Figure 37: Serial Video Output Interface Signals

Parameter	Description	Min	Max	Units
Tsersu	Data setup (**DSDAT** and **DSFRM**) before negative edge of **DSCLK.**	5	-	nsec
Tserh	Data hold (**DSDAT** and **DSFRM**) before negative edge of **DSCLK.**	5	-	nsec

7.9 Serial Video Output Clock Qualified mode AC Characteristics

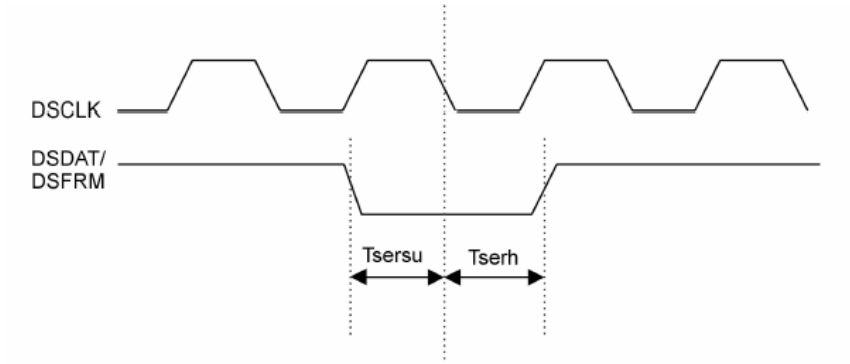


Figure 38: Serial Video Output Clock Qualified mode AC

Parameter	Description	Specifications		Units
		Min	Max	
Tsersu	Data setup (**DSDAT** and **DSFRM**) before negative edge of **DSCLK**	5	-	ns
Tserh	Data hold (**DSDAT** and **DSFRM**) before negative edge of **DSCLK.**	5	-	ns

Table 17: Serial Video Output Clock Qualified mode AC Characteristics

* Results depend on device frequency and mode. The results in this table are for 32MHz, **SVI CLK = clk_in.**

7.10 Serial Video Output SSI mode AC Characteristics

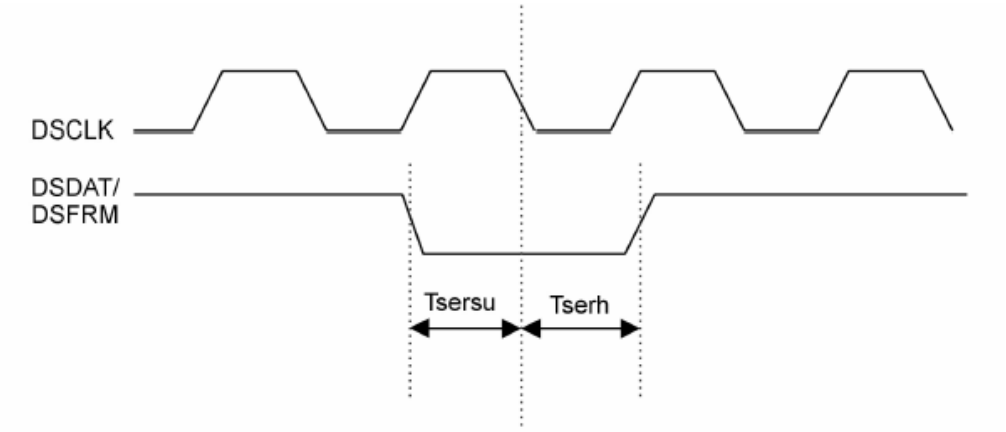


Figure 39: Serial Video Output SSI mode

Param	Description	Specifications		Units
		Min	Max	
Tsersu	Data setup (**DSDAT** and **DSFRM**) before negative edge of **DSCLK**	5	-	ns
Tserh	Data hold (**DSDAT** and **DSFRM**) before negative edge of **DSCLK**	5	-	ns

Table 18: Serial Video Output SSI mode AC Characteristics

* Results depend on device frequency and mode. The results in this table are for 32MHz, **SVI CLK = clk_in.**

7.11 I²C-Compatible Interface AC Characteristics

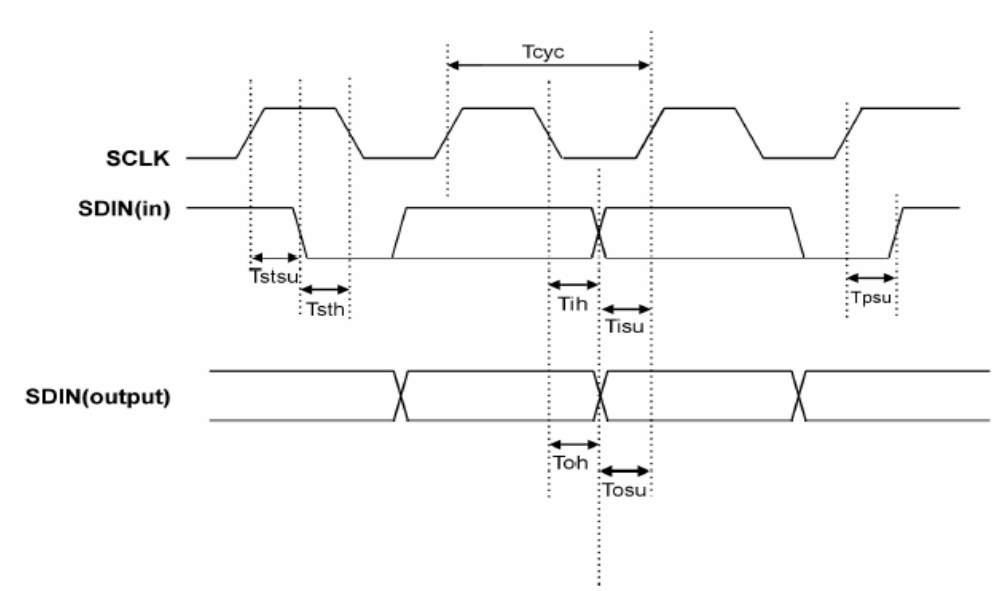


Figure 40: I²C-Compatible Interface

Parameter	Description	Specifications		Units
		Min	Max	
Fmax	Maximum **SCLK** frequency		400	KHz
Tcyc	**SCLK** cycle duration	2500		ns
Tstsu	Start condition **SCLK** setup time	125		ns
Tsth	Start condition **SCLK** hold time	250		ns
Tih	**SDIN** input hold time	125		ns
Tisu	**SDIN** input setup time	250		ns
Tpsu	Stop condition **SCLK** setup time	125		ns
Toh	**SDIN** output hold time	125		ns
Tosu	**SDIN** output setup time	250		ns

Table 19: I^2C-Compatible Interface AC Characteristics

Note: Data entered is calculated for 400KHz **SCLK** frequency.

8. Mechanical and Electrical Drawings

8.1 TC5747 39-pin Package

Following is a mechanical drawing of the TC5747 39-pin module with board-to-board connector.

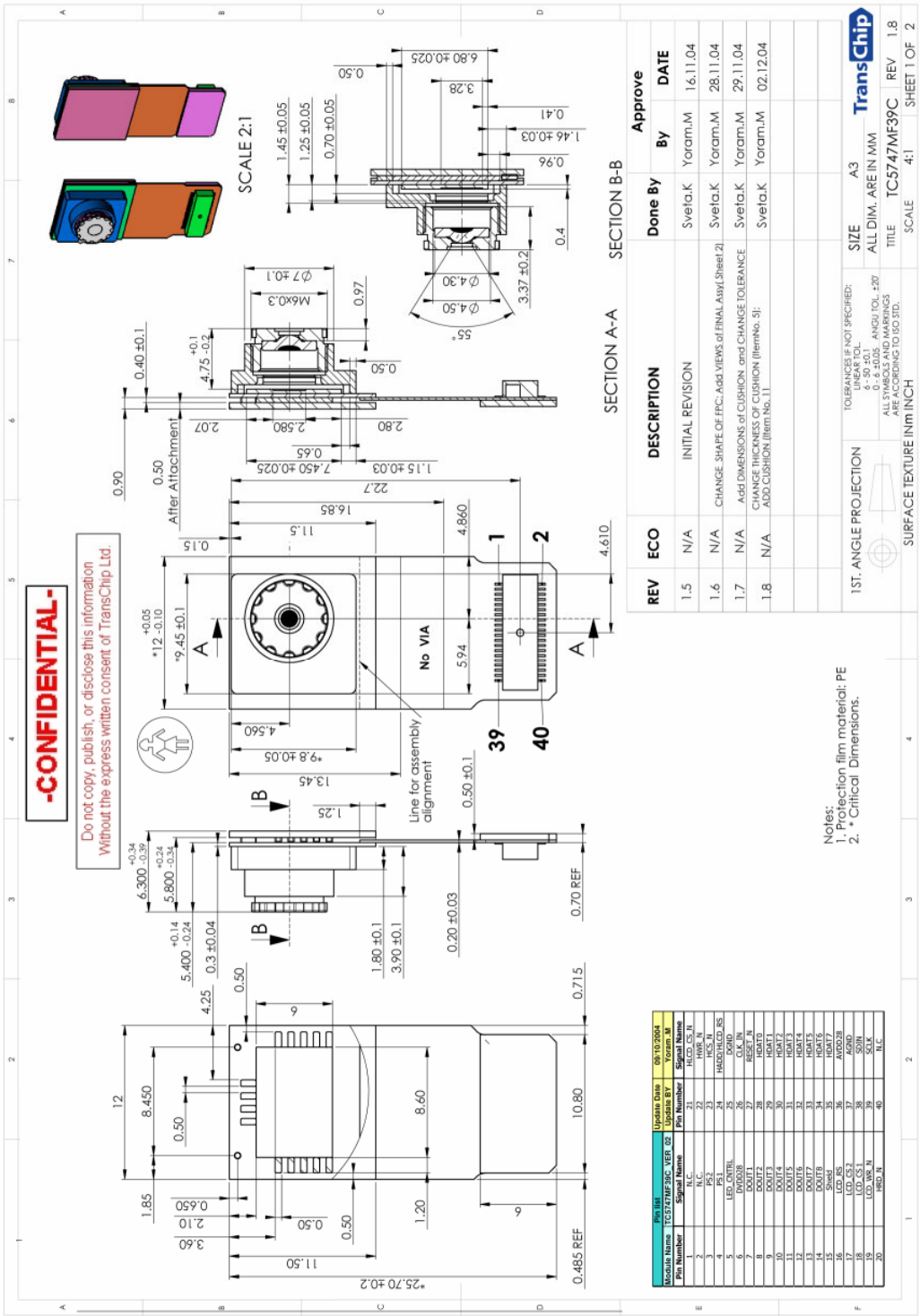


Figure 41:TC5747 39-pin Module Mechanical Drawing

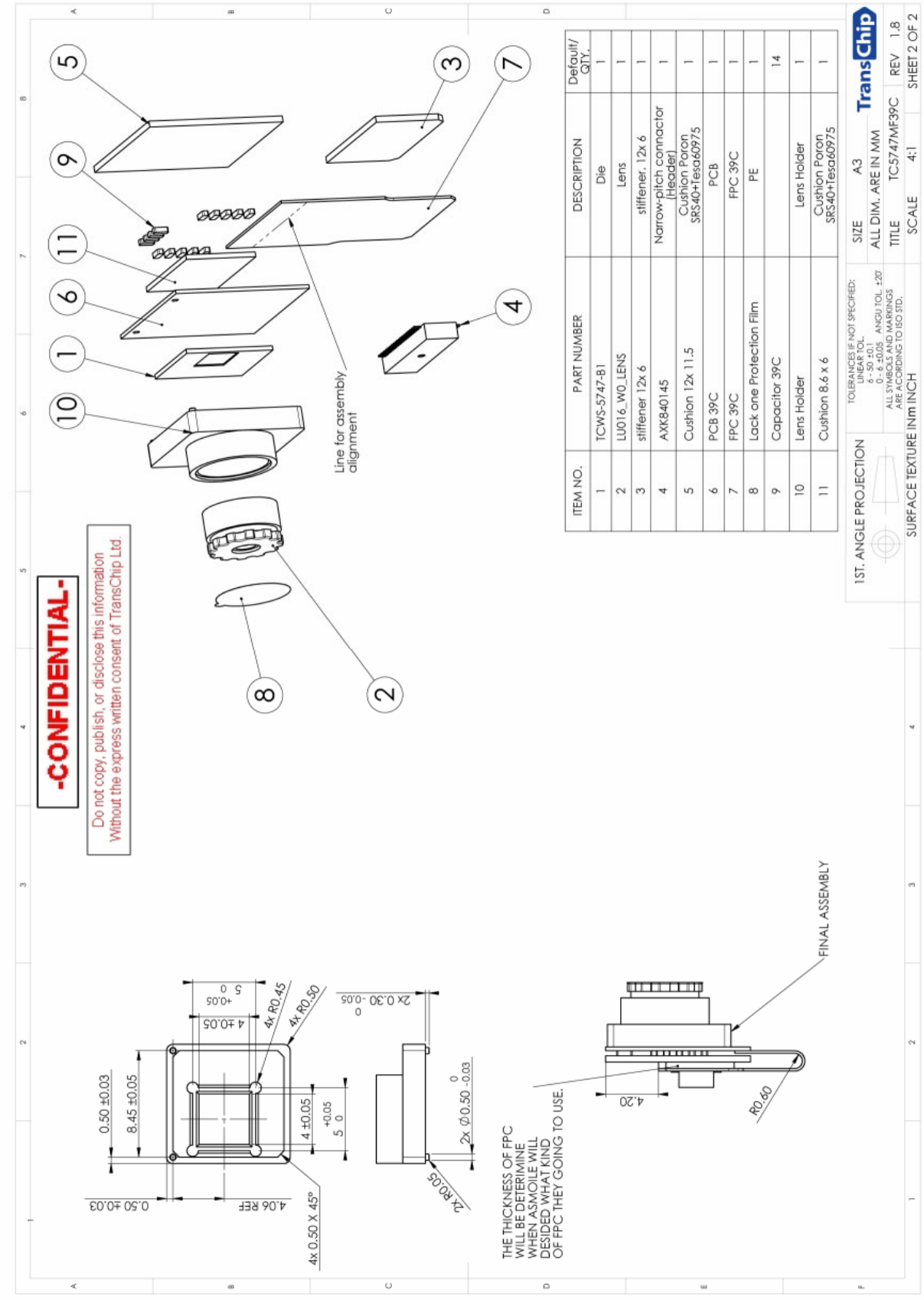


Figure 42:TC5747 39-pin Module Mechanical Drawing Continued

8.2 TC5747 24 Pin Package

Following is a mechanical drawing of the TC5747 24 pin module with board-to-board connector.

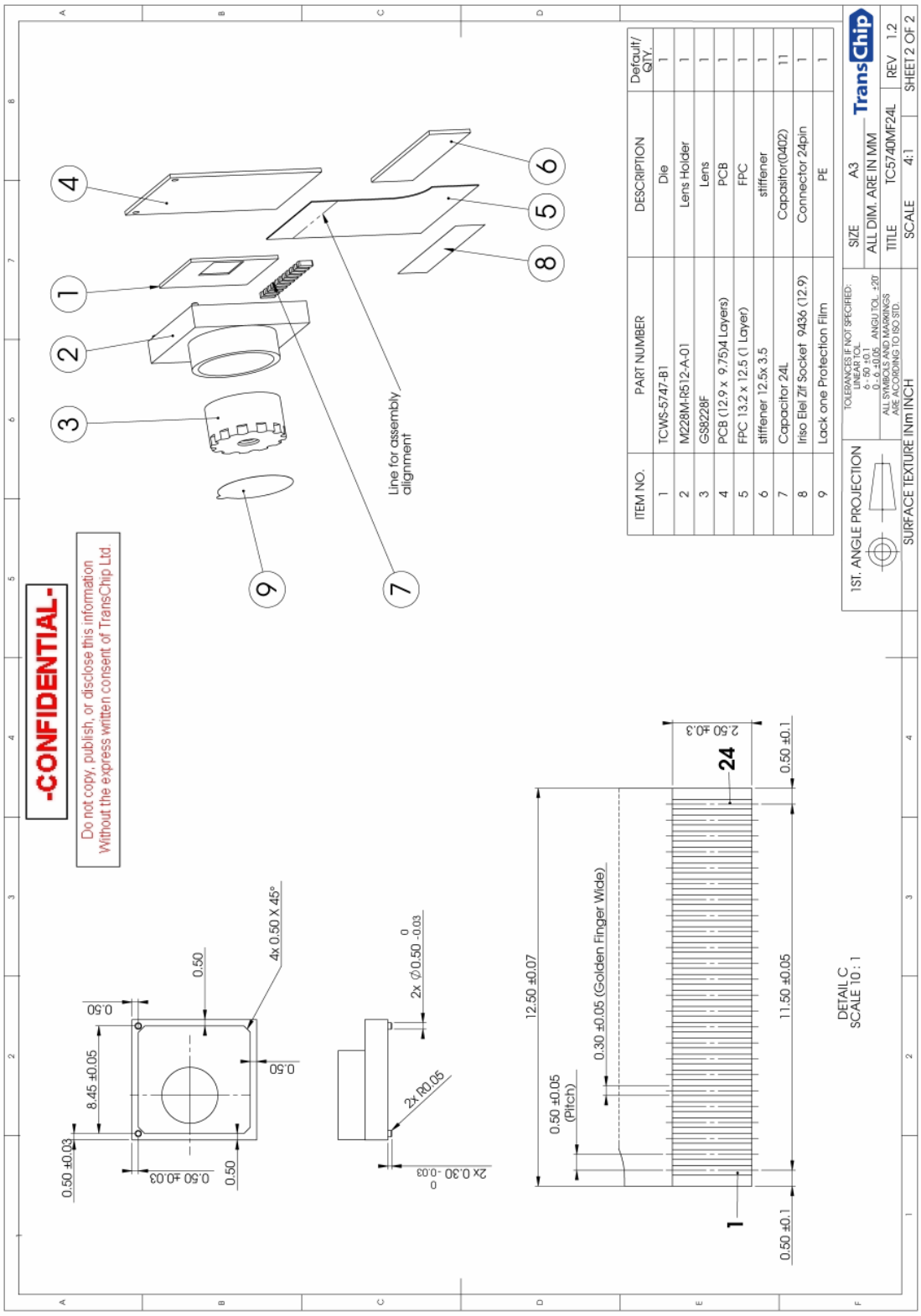


Figure 43: TC5747 24-pin Module Mechanical Drawing

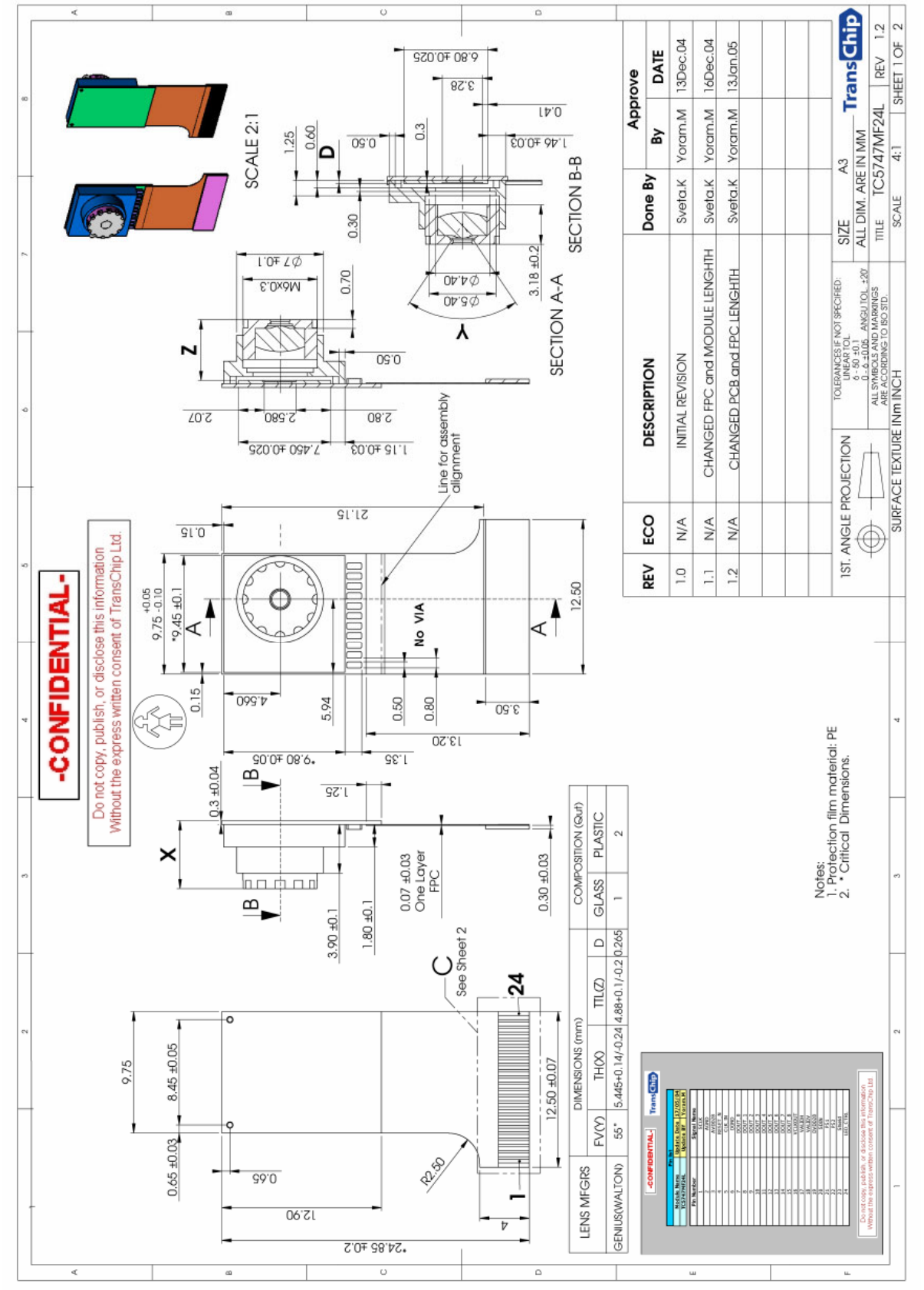


Figure 44: TC5747 24-pin Module Mechanical Drawing Continued

8.3 TC5747 51-pin Package

The mechanical drawing of 51-pin version with Flex cable connector is TBD.

8.4 Lens Specification

Characteristic	1/4 " Lens module
Material	Heat resistant plastic
Structure	Three element (one glass and two plastic)
Effective Focal Length	3.72 mm
Focal Range	40cm - infinity
F Number	2.4
Angle of View (FOV)	55° Diagonal 45° Horizontal 35° Vertical
Focus	Factory fixed focused
IR Filter	Included
Resolution (MTF) for RGB	0.47 @ 45 cy/mm on-axis 0.40 @ 45 cy/mm Vertical 0.30 @ 45 cy/mm Horizontal 0.27 @ 45 cy/mm Diagonal
Relative Illumination	100% On-Axis 75% Vertical 65% Horizontal 55% Diagonal
TV Distortion	<1%
Module Height	5.5 mm +0.1 mm/ -0.2mm

Table 20: Lens Specifications