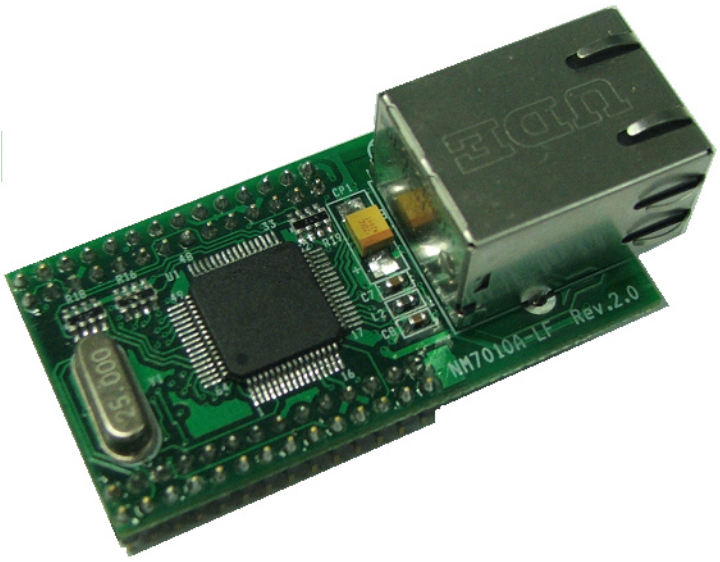
# NM7010A-LF

**(Ver. 2.6)**

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# Document History Information

| Revision | Data | Description |
|---|---|---|
| V2.5 | July 3, 2006 | Revision Docs & NM7010A-LF Module<br>- Datasheet, Part List, Schematics<br>- NM7010A-LF 1.1 → NM7010A-LF 2.0 (Replace PHY & Mag-Jack Parts) |
| V2.6 | July 24, 2007 | Revision Docs & NM7010A-LF Module<br>- Datasheet, PartList, Schematics<br>- NM7010A-LF Rev.2.0 replace PHY and related parts |

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## Table of Contents

# 1. Introduction

NM7010A-LF is the network module that includes W3100A-LF (TCP/IP hardwired chip), Ethernet PHY **(IP101A**), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W3100A-LF and PHY chip. The NM7010A-LF is an ideal option for users who want to develop their Internet enabling systems rapidly.

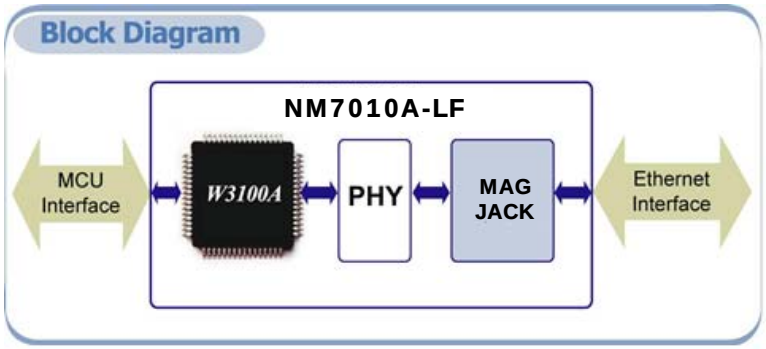
NM7010A-LF consists of W3100A-LF, Ethernet PHY and MAG-JACK.

- TCP/IP, MAC protocol layer: W3100A-LF
- Physical layer: Ethernet PHY(IP101A-LF LQFP48)
- Connector: MAG-JACK

## 1.1. Features

- Supports 10/100 Base TX half/full duplex operation
- Supports auto-negotiation, **Auto MDI/MDIX**
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports Intel/Motorola MCU bus Interface and $I^2C$ Interface
- Supports Direct/Indirect mode bus access
- Supports clocked mode, non-clocked mode, external clocked mode
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 14 header pin

## 1.2. Block Diagram



# 2. Pin Assignments & descriptions

I : Input O : Output

I/O : Bi-directional Input and output P : Power

## 2.1. Power & Ground

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| VCC | P | JP1 : 1 , JP2 : 24 | **Power** : 3.3 V power supply |
| GND | P | JP1 : 8, JP1 : 13, JP1 : 24,<br>JP2 : 1, JP2 : 4, JP2 : 7,<br>JP2 : 13, JP2 : 14, JP2 : 23 | **Ground** |

## 2.2. MCU Interfaces

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| A14~A8 | I | JP1 : 7, JP1 : 10<br>JP1 : 9, JP1 : 12<br>JP1 : 11, JP1 : 14<br>JP1 : 15 | **Address / Device Address :**In Bus access mode is used as Address[14-8] pin<br>In $I^2C$ interface mode is used as device address[6-0] pin |
| A7~A0 | I | JP1 : 16 ~ JP1 : 23 | **Address :**<br>In Bus access mode is used as Address[7-0] pin<br>In $I^2C$ interface mode, these pins are not used, so leave them NC or ground them. |
| D7~D0 | I/O | JP2 : 21, JP2 : 22, JP2 : 19,<br>JP2 : 20, JP2 : 17, JP2 : 18<br>JP2 : 15, JP2 : 16 | **Data** : 8 bit-wide data bus |
| /CS | I | JP1 : 5 | **Module Select** : Active low.<br>/CS of W3100A-LF |
| /RD | I | JP1 : 4 | **Read Enable** : Active low.<br>/RD of W3100A-LF |
| /WR | I | JP1 : 3 | **Write Enable** : Active low<br>/WR of W3100A-LF |

| | | | |
|---|---|---|---|
| /INT | O | JP1 : 2 | **Interrupt** : Active low<br>After reception or transmission it indicates that the W3100A-LF requires MCU attention.<br>By writing values to the Interrupt Status Register of W3100A-LF the interrupt will be cleared.<br>All interrupts can be masked by writing values to the IMR of W3100A-LF(Interrupt Mask Register).<br>For more details refer to the W3100A-LF Datasheet |
| I_SCL | I | JP2 : 25 | **SCL** :<br>Used as clock by $I^2C$ interface mode.<br>Internally pull-down |
| I_SDA | I/O | JP2 : 26 | **SDA** :<br>Used as data by $I^2C$ interface mode.<br>Internally pull-down |

## 2.3. Network status & LEDs

You can observe the network status using MAC-JACK LEDs. LED interface can be extended to the LED of the main board.

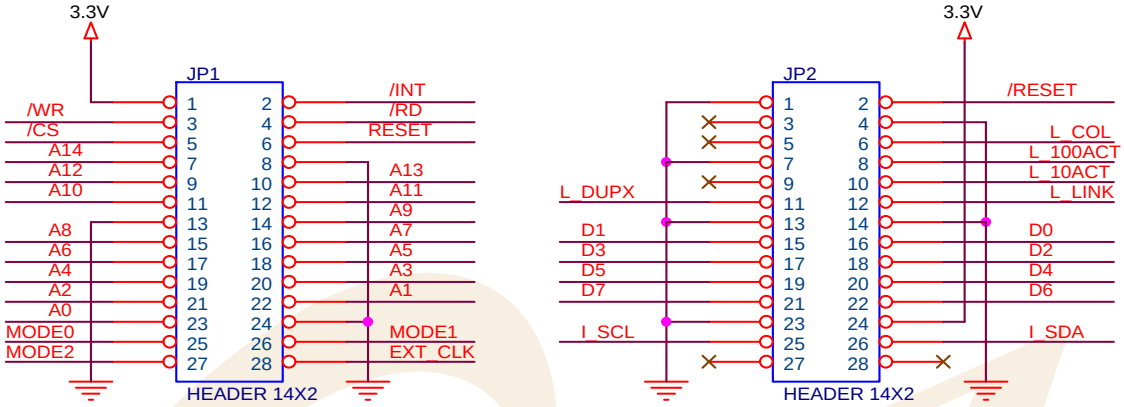
| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| L_COL | O | JP2 : 6 | **Collision LED** : Active low when collisions occur. |
| L_100ACT | O | JP2 : 8 | **Link 100/ACT LED** : Active low when linked by 100 Base TX, and blinking when transmitting or receiving data. |
| L_10ACT | O | JP2 : 10 | **Link 10/ACT LED** : Active low when linked by 10 Base T, and blinking when transmitting or receiving data. |
| L_DUPX | O | JP2 : 11 | **Full Duplex LED** : Active low when in full duplex operation. Active high when in half duplex operation. |
| L_LINK | O | JP2 : 12 | **Link LED** : Active low when linked |

## 2.4. Miscellaneous Signals

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>RESET</td><td>I</td><td>JP1 : 6</td><td>Reset : Active high<br>Initializes or Reinitializes the W3100A-LF. Asserting this pin will force a reset process to occur, which will result in all internal registers reinitializing to their default and all strapping options are reinitialized.<br>For complete reset function, this pin must be asserted low for at least 10us. Refer to W3100A-LF datasheet for further detail regarding reset.</td></tr>
<tr><td>/RESET</td><td>I</td><td>JP2 : 2</td><td>Reset : Active low<br>Reset RTL8201BL chip. For complete reset function this pin must be asserted low for at least 10ms.</td></tr>
<tr><td>MODE1~0</td><td>I</td><td>JP1 : 26 ,<br>JP1 : 25</td><td>Mode Select : These pins select MCU interface and operating mode. Since each pin is pull-down internally, clocked mode (the default mode) is selected when these pins are not connected.
<table>
<tr><th>M1 M0</th><th>Mode</th></tr>
<tr><td>0 0</td><td>Clocked</td></tr>
<tr><td>0 1</td><td>External clocked</td></tr>
<tr><td>1 0</td><td>Non-clocked</td></tr>
<tr><td>1 1</td><td>$I^2C$ interface</td></tr>
</table>
Refer to W3100A-LF datasheet for further detail regarding mode select</td></tr>
<tr><td>EXT_CLK</td><td>I</td><td>JP1 : 28</td><td>External clock : supplementary clock used for external clocked mode.<br>In external clocked mode, W3100A-LF uses this clock to interface with MCU.<br>Refer to W3100A-LF datasheet for further detail regarding external clock.</td></tr>
<tr><td>NC</td><td>-</td><td>JP1 : 27, JP2 : 3<br>JP2 : 5, JP2 : 9<br>JP2 : 27, JP2 : 28</td><td>Not Connect</td></tr>
</table>

## 2.5. Pin Location & Schematic

Refer to “Chapter 4. Dimension”.




# 3. Timing Diagrams

NM7010A-LF provides following interfaces of W3100A-LF

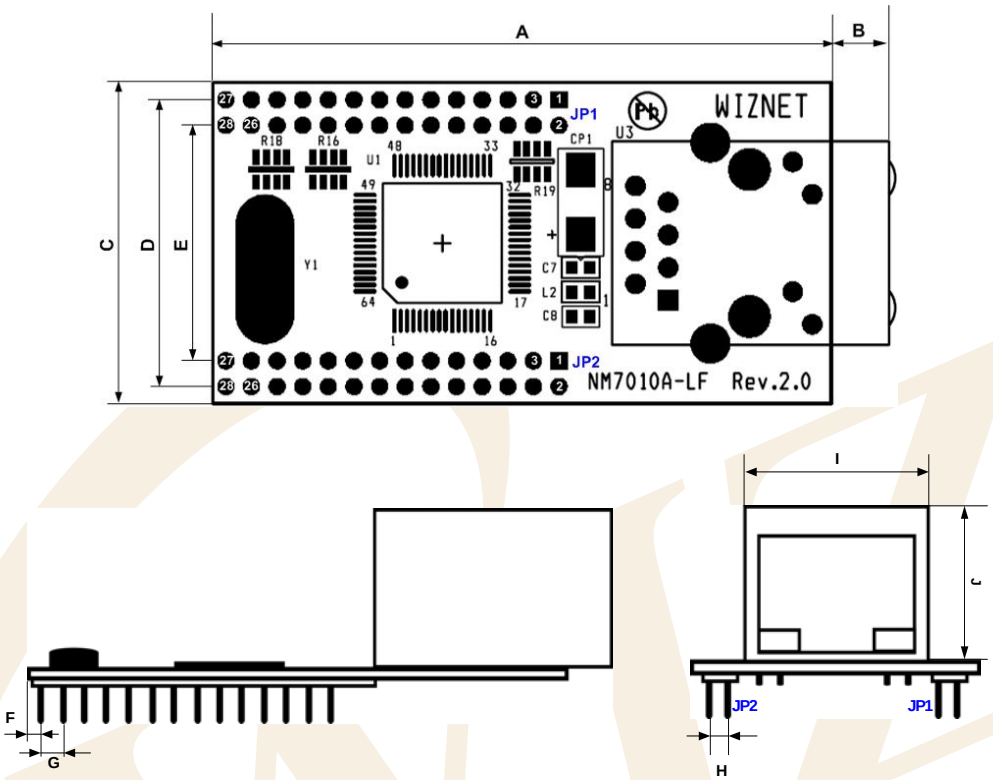
-. Direct/Indirect mode bus access

-. $I^2C$ Interface

-. Clocked mode, Non-Clocked mode, External clocked mode

Refer to W3100A-LF datasheet for timing of NM7010A-LF

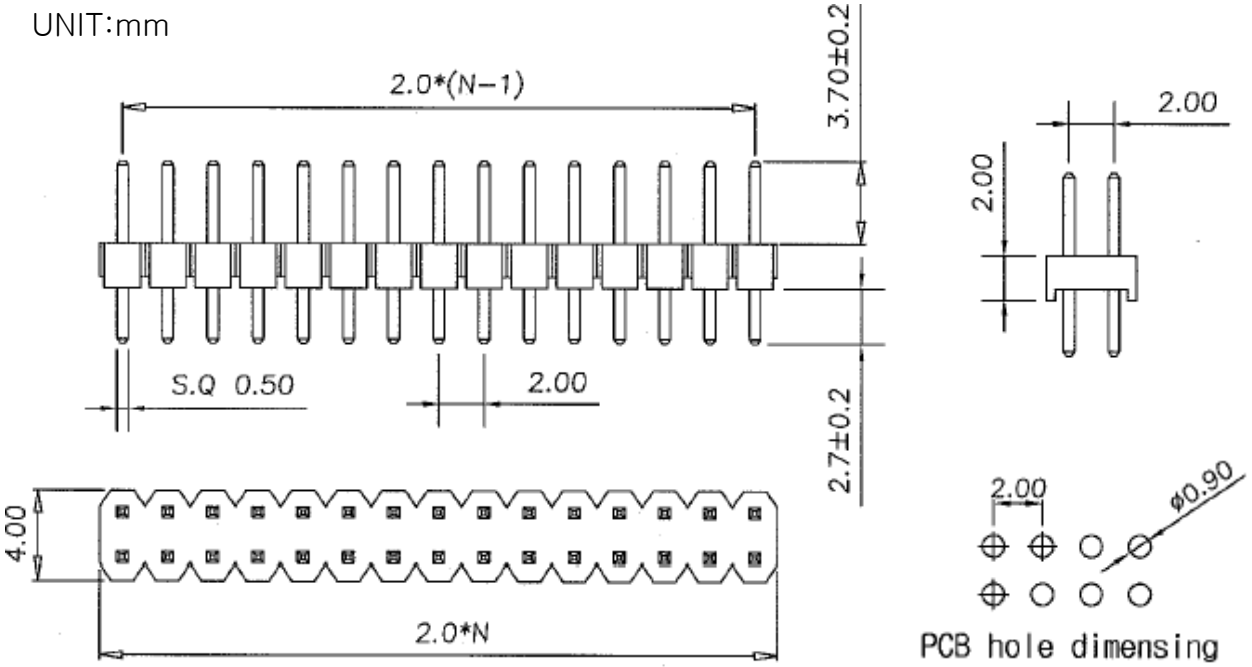
# 4. Dimensions



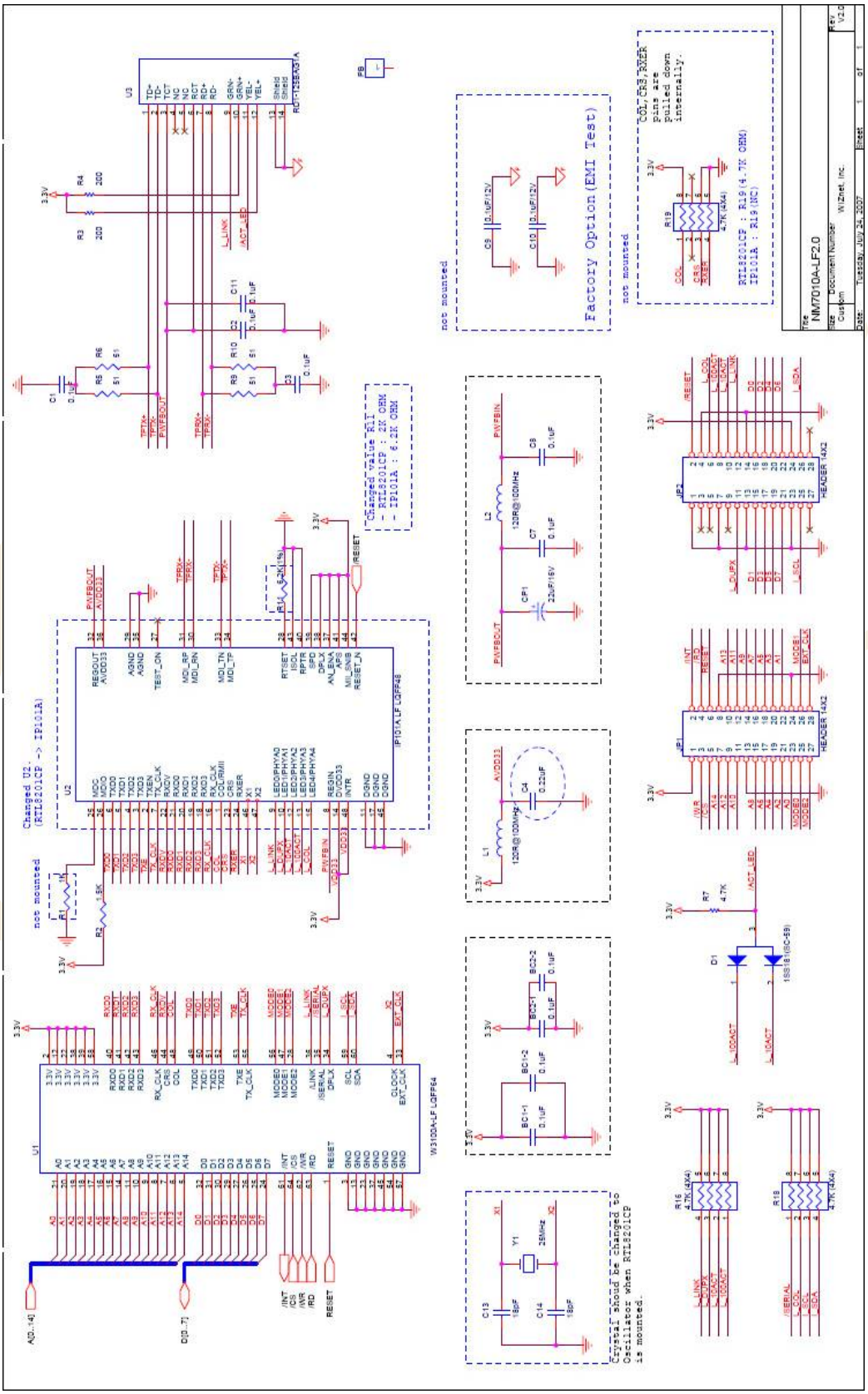

| Symbols | Dimensions (mm) |
|---|---|
| A | 48.0 |
| B | 4.0 |
| C | 25.0 |
| D | 22.4 |
| E | 18.4 |
| F | 1.0 |
| G | 2.0 |
| H | 2.0 |
| I | 16.0 |
| J | 13.4 |

# 5. Connector Specification

UNIT:mm



# 6. Schematic



[ Schematic History ( NM7010A-LF REV.2.0) ]

| | Description | Parts |
|---|---|---|
| Before | W3100A + RTL8201CP | R19 : 4.7K OHM ARRAY<br>R1 : 1K OHM<br>R11 : 2K OHM 1%<br>C4 : 0.1uF<br>U2 : RTL8201CP |
| After | W3100A + IP101A-LF. | R19 : Not mounted<br>R1 : Not mounted<br>R11 : 6.2K OHM 1%<br>C4 : 0.22uF<br>U2 : IP101A-LF |

※ If you have the hardware having previous parts, refer to the NM7010A datasheet V2.5 for the usage. For more stable operation, we recommend using the part revised hardware.

# 7. PartLists

| Item | Q.ty | Reference | Part | Tech. Characteristics | Package |
|---|---|---|---|---|---|
| 1 | 10 | C1,C2,C3,C7,C8, C11,BC1-1,BC1-2, BC2-1,BC2-2 | 0.1uF | 50V-20% Ceramic | CASE 0603 |
| 2 | 1 | C4 | 0.22uF | 50V-20% Ceramic | CASE 0603 |
| 3 | 1 | CP1 | 22uF | 16Vmin 10% | EIA/IECQ 3528 |
| 4 | 2 | C13,C14 | 18pF | 50V-20% Ceramic | CASE 0603 |
| 5 | 0 | C9,C10 | 0.1uF | **NOT MOUNTED** | |
| 6 | 1 | D1 | 1SS181 Switching Diode | | SC-59 |
| 7 | 2 | JP1,JP2 | 2X14 28PIN 2mm DIP STRAIGHT Header | 2 X 14 2mm pitch | |
| 8 | 2 | L1,L2 | 120R Chip Ferrite Bead | 120R@100MHz 300mA | CASE 0603 |
| 9 | 0 | R1 | 1K | **NOT MOUNTED** | |
| 10 | 1 | R2 | 1.5K | 1/10W-5% SMD | CASE 0603 |
| 11 | 2 | R3,R4 | 200 | 1/10W-5% SMD | CASE 0603 |
| 12 | 4 | R5,R6,R9,R10 | 51 1% | 1/10W-1% SMD | CASE 0603 |
| 13 | 1 | R7 | 4.7K | 1/10W-5% SMD | CASE 0603 |
| 14 | 1 | R11 | 6.2K 1% | 1/10W-1% SMD | CASE 0603 |
| 15 | 2 | R16,R18 | 4.7K Chip Array(0603 X 4) | 50V-5% SMD Chip-Array | CASE 1206 |
| 16 | 0 | R19 | 4.7K Chip Array(0603 X 4) | **NOT MOUNTED** | |
| 17 | 1 | U1 | W3100A-LF | | LQFP64 |
| 18 | 1 | U2 | IP101A-LF | | LQFP48 |
| 19 | 1 | U3 | RD1-125BAG1A | Transformer + RJ45 | |
| 20 | 1 | Y1 | 25MHz Crystal | Holder Type, CL=18pF | ATS-25U |
| 21 | 1 | | NM7010A-LF REV2.0 FR4 1.6T 4LAYER | PRINTED CIRCUIT BOARD | |