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Coherency in the Time Processor Unit (TPU)

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General Information

Sometimes, two parameters in the time processor unit (TPU) parameter RAM must be updated together. In other words, if one parameter is updated, the other also must be immediately updated. This is called coherency.

A data transfer is coherent if all of the data is transferred before any of it is updated or used. Thus, all of the data must be read or written at the same time. Some of the current TPU functions have two parameters that need to be read or written coherently.

An example is the PWM function. Its parameters, PWMHI (the pulse high time) and PWMPER (the pulse period), must be written coherently or else the TPU may use one parameter before the other is updated, thus generating an incorrect waveform.

Another example is the ITC function. Its parameters MAX_COUNT (the maximum number of transitions to be counted) and TRANS_COUNT (the current count) must be accessed coherently; otherwise, the TPU may update TRANS_COUNT between the two accesses.

The only way to coherently access two parameters in the parameter RAM is to do a long-word read or write. Doing two back-to-back word writes will not guarantee coherent access. The control registers cannot

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be guaranteed coherent access. For them, doing a long-word read or write is no different than doing two back-to-back word writes.

Although all of the parameter RAM and control registers are word accessible, the channel interrupt status register (CISR) is the only register that is byte accessible. If a byte is written to any other parameter RAM location or control register, the TPU will correctly write to the byte selected, but will write all 1s to the other half of the parameter RAM location.

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