

# INDEX



## -A-

ADDR D-23  
bus signals 5-29  
definition 2-4  
signal 5-33  
starting address D-18  
Address  
bus (ADDR) 5-29  
map 3-14  
-mark wakeup 6-33  
space  
encoding 5-31  
maps 3-14—3-18  
strobe ( $\overline{AS}$ ) 5-29  
Arbitration 6-3  
AS 5-29, 5-35, 5-38, 5-45  
Asserted (definition) 2-4  
ATEMP 4-21  
AVEC 5-22, 5-32, 5-61, 5-66  
enable bit 5-68, D-21

## -B-

Background  
debug mode 4-19, 5-39  
commands 4-22  
connector pinout 4-26  
enabling 4-20  
entering 4-21  
registers  
fault address register (FAR) 4-23  
instruction program counter (PCC) 4-23  
return program counter (RPC) 4-23  
returning from 4-24  
serial  
data word 4-26  
I/O block diagram 4-25  
interface 4-24  
peripheral interface protocol (SPI) 4-25  
sources 4-20  
Basic operand size 5-33  
Baud  
clock 6-28  
rate generator 6-2  
BC D-42  
BCD 4-4  
Berg connector (male) 4-26  
 $\overline{BERR}$  5-35, 5-39, 5-44, 5-45, 5-61  
assertion results 5-43  
 $\overline{BG}$  5-46, 5-66  
 $\overline{BGACK}$  5-46, 5-66

BGND instruction 4-21  
BH D-42  
Binary  
-coded decimal (BCD) 4-4  
BITS D-33  
encoding field 6-20  
Bits per transfer  
enable (BITSE) D-38  
field (BITS) D-33  
BITSE 6-22, D-38  
Bit-time 6-27  
 $\overline{BKPT}$  4-20, 5-39, 5-49, 5-58  
external signal 4-21  
BKPT (TPU asserted) D-42  
BL D-42  
BLC D-41  
Block size (BLKSZ) 5-66, D-18  
encoding 5-67, D-18  
BM D-42  
BME 5-23, D-13  
BMT 5-22, D-13  
BP D-42  
 $\overline{BR}$  5-45, 5-46, 5-66  
Branch latch control (BLC) D-41  
Break frame 6-28  
Breakpoint  
acknowledge cycle 5-39  
asserted flag (BKPT) D-42  
enable bits D-42  
flag (PCBK) D-43  
hardware breakpoints 5-39  
instruction 4-19  
mode selection 5-53  
operation 5-41  
software breakpoints 5-39  
Brushless motor commutation (COMM) 7-12  
BSA 4-20  
BT D-42  
Built-in emulation memory C-1  
Bus  
arbitration  
single device 5-47  
cycle  
regular 5-35  
termination sequences 5-42  
error  
exception processing 5-44  
signal ( $\overline{BERR}$ ) 5-22, 5-31, 5-44  
timing of 5-44  
grant ( $\overline{BG}$ ) 5-46  
grant acknowledge ( $\overline{BGACK}$ ) 5-46



monitor 5-22  
  external enable (BME) D-13  
  timeout period 5-23  
  timing (BMT) 5-22, D-13  
request (BR) 5-46  
state analyzer (BSA) 4-20  
BYTE (upper/lower byte option) 5-67, D-19

-C-

C (carry) flag 4-6, D-4

Case outlines

  831A-01 (132-pin package) B-4  
  863C-01 (144-pin package) B-5  
  918-02 (144-pin package) B-6

CCL D-42

CCR 4-6

CFSR D-44

CH D-44, D-45, D-46

CHANNEL D-44

Channel

  conditions latch (CCL) D-42  
  control registers 7-15  
  function select registers 7-15  
  interrupt  
    base vector (CIBV) D-43  
    enable  
      /disable field (CH) D-44  
      and status registers 7-15  
    request level (CIRL) D-43  
    status (CH) D-46

  orthogonality 7-4

  priority registers 7-17

  register breakpoint flag (CHBK) D-43

CHBK D-43

Chip-select

  base address  
    register boot ROM (CSBARBT) D-17  
    registers (CSBAR) 5-65, 5-66, D-17  
      reset values 5-71

  operation 5-68

  option

    register boot ROM (CSORBT) D-18  
    registers (CSOR) 5-65, 5-67, D-18  
      reset values 5-71

pin

  assignment registers (CSPAR) 5-65, D-15  
  field encoding 5-66, D-17  
  pin  
    assignments D-17

  reset operation 5-70

  signals for interrupt acknowledge 5-69

CIBV D-43

CIER 7-16, D-44

CIRL D-43

CISR 7-13, 7-16, D-46

Clear (definition) 2-4

CLKOUT 5-34, 5-49

CLKRST (clock reset) 5-48

CLKS D-42

Clock

control multipliers

  16.78 MHz 5-8  
  20.97 MHz 5-10  
  25.17 MHz 5-12

mode

  pin (MODCLK) 5-53  
  selection 5-53

output (CLKOUT) 5-34

phase (CPHA) D-33

polarity (CPOL) D-33

synthesizer

  control register (SYNCR) D-8  
  operation 5-5

Coherency 7-4

COMM 7-12

Command RAM 6-9

Common in-circuit emulator 4-20

Completed queue pointer (CPTQP) D-37

Condition code register (CCR) 4-6, 7-5

CONT D-38

Contention 5-61

Continue (CONT) D-38

Continuous transfer mode 6-7

Conventions 2-4

CPHA 6-19, D-33

CPOL 6-19, D-33

CPR D-46

CPTQP 6-10, D-37

CPU space

  address encoding 5-39

  cycles 5-38

  encoding for interrupt acknowledge 5-69

CPU32 5-48

  address registers/address organization in 4-5

  addressing modes 4-9

  block diagram 4-2

  data registers 4-4

    data organization 4-5

  development support 4-18

  exception processing 4-16

  features 3-1

  generated message encoding 4-26

  instructions 4-10

    LPSTOP 4-15

    MOVEC 4-7

    MOVES 4-7

    RESET 5-49

    special control instructions 4-15

  table lookup and interpolate (TBL) 4-15

  unimplemented MC68020 instructions 4-10

loop mode 4-15

memory organization 4-7

processing states 4-9

reference manual 4-1

register

  model 4-3, D-2

  registers 4-2

    alternate function code registers (SFC/DFC) 4-7

    condition code register (CCR) 4-6, D-3

    control registers 4-6



mnemonics 2-2  
program counter (PC) 4-1  
stack pointer (SP) 4-1  
status register (SR) 4-6, D-3  
vector base register (VBR) 4-7  
virtual memory 4-9  
**CR** D-38  
**CREG** D-22  
**CSBAR** D-17  
**CSBARBT** D-17  
**CSBOOT** 5-58, 5-64, 5-66  
  reset values 5-72  
**CSOR** D-18  
**CSORBT** D-18  
**CSPAR** D-15

**-D-**

**DATA** 5-29  
**Data**  
  and size acknowledge (**DSACK**) 5-22, 5-31  
  bus  
    mode selection 5-50  
    signals (**DATA**) 5-29  
  frame 6-28  
  multiplexer 5-33  
  strobe (**DS**) 5-30  
  types 4-4  
**DATA** (definition) 2-4  
**DBcc** 4-16  
**DCNR** D-47  
**DDRE** 5-72, D-10  
**DDRF** 5-72, D-11  
**DDRQS** 6-4, 6-18, 6-22, D-31  
**Delay**  
  after transfer (DT) 6-20, D-38  
  before SCK (**DSCKL**) D-34  
**Designated CPU space** 5-30  
**Development**  
  support and test registers (TPU) 7-17  
  tools and support C-1  
**DFC** 4-7  
**DIO** 7-6  
**Discrete input/output** (DIO) 7-6  
**Distributed register** (DREG) D-22  
**DIV8** clock 7-15  
**Double**  
  -buffered 6-29, 6-31  
  bus fault 4-21, 5-44  
  -row header 4-26  
**DREG** D-22  
**Driver types** 3-9  
**DS** 5-30, 5-35, 5-45  
**DSACK** 5-22, 5-35, 5-39, 5-61, 5-66, 5-68  
  assertion results 5-43  
  external/internal generation 5-38  
  option fields 5-38  
  signal effects 5-32  
  source specification in asynchronous mode 5-68,  
    D-19  
**DSCK** D-38

**DSCKL** D-34  
**DSCLK** 4-25  
**DSCR** D-41  
**DSSR** D-42  
**DT** D-38  
**DTL** D-35  
**Dynamic bus sizing** 5-32

**-E-**

**EBI** 5-61  
**ECLK** 5-20  
**EDIV** 5-20, D-8  
**EMU** 7-5, 7-15, D-40  
**Emulation**  
  control (EMU) 7-15, D-40  
  support 7-5  
**Encoded**  
  one of three channel priority levels (CH) D-46  
  time function for each channel (CHANNEL) D-44  
  type of host service (CH) D-45  
**Ending queue pointer** (ENDQP) D-36  
**ENDQP** 6-10, D-36  
**Error**  
  conditions 6-31  
  detection circuitry 6-2  
**Event timing** 7-3  
**Exception**  
  instruction (RTE) 5-44  
  processing 4-16, 5-48  
  sequence 4-18  
  types of exceptions 4-17  
  vectors 4-16  
    exception vector assignments 4-17  
    vector 5-48, 7-6  
**EXOFF** D-7  
**EXT** D-9  
**EXTAL** 5-4  
**External**  
  bus  
    arbitration 5-46  
    clock  
      division (EDIV) D-8  
      division bit (EDIV) 5-20  
      operation during LPSTOP 5-20  
      signal (ECLK) 5-20  
      interface (EBI) 5-27  
      control signals 5-29  
    clock off (EXOFF) D-7  
    reset (EXT) D-9  
**Externally**  
  input clock frequency D-14  
**EXTRST** (external reset) 5-56

**-F-**

**Factory test** 5-73  
**FAR** 4-23  
**Fast**  
  quadrature decode (FQD) 7-12  
  termination



cycles 5-34, 5-38  
FC 5-30  
FE 6-31, D-30  
FQD 7-12  
FQM 7-13  
Frame 6-28  
  size 6-32  
Framing error (FE) flag 6-31, D-30  
**FREEZE**  
  assertion response (FRZ)  
    QSM 6-3, D-25  
    SIM 5-3  
    TPU 7-5  
  bus monitor (FRZBM) 5-3, D-7  
  software enable (FRZSW) 5-3, D-7  
 $f_{ref}$  5-4  
**Frequency**  
  control  
    counter (Y) D-8  
    prescaler (X) D-8  
    VCO (W) D-8  
  measurement (FQM) 7-13  
**FRZ** D-25, D-42  
**FRZBM** 5-3, D-7  
**FRZSW** 5-3, D-7  
 $f_{sys}$  5-4, D-8  
F-term encoding 5-38  
**Function**  
  code (FC) signals 5-30, 5-38  
  library for TPU 7-5  
 $f_{VCO}$  5-6

## -H-

Hall effect decode (HALLD) 7-13  
**HALLD** 7-13  
**HALT** D-36  
**HALT** 5-23, 5-31, 5-35, 5-45  
  assertion results 5-43  
**Halt**  
  acknowledge flag (HALTA) D-37  
  monitor  
    enable (HME) 5-23, D-13  
    reset (HLT) D-9  
  operation 5-45  
    negating/reasserting 5-45  
  QSPI (HALT) D-36  
**HALTA** D-37  
**HALTA/MODF** interrupt enable (HMIE) bit D-36  
Handshaking 5-34  
Hang on T4 (HOT4) D-41  
Hardware breakpoints 5-39  
**HCMOS** 1-1  
High-density complementary metal-oxide semiconductor (HCMOS) 1-1  
**HLT** D-9  
**HME** 5-23, D-13  
**HMIE** D-36  
**Host**  
  sequence registers 7-17  
  service registers 7-17

HOT4 D-41  
HSQR D-45  
HSSR D-45  
Hysteresis 5-60

## -I-

**IARB**  
  QSM D-25  
  SIM 5-2, 5-3, 5-60, D-7  
  TPU 7-5, D-41  
**ICD16/ICD32** C-1  
 $I_{DD}$  5-54  
**IDLE** 6-32, D-29  
**Idle**  
  frame 6-28  
  -line  
    detect type (ILT) D-28  
    detected (IDLE) 6-32, D-29  
    detection process 6-32  
    interrupt enable (ILIE) 6-32, D-28  
    type (ILT) bit 6-32  
**ILIE** 6-32, D-28  
**ILQSPI** D-25  
**ILSCI** D-25  
**ILT** 6-32, D-28  
In-circuit debugger (ICD16/ICD32) C-1  
**Input**  
  capture/input transition counter (ITC) 7-6  
  clock ( $f_{ref}$ ) 5-4  
**Interchannel communication** 7-4  
**Intermodule bus** (IMB) 3-2  
**Internal**  
  bus  
    error (BERR) 5-22, 5-23  
    monitor 5-22  
    register map 3-14  
**Interrupt**  
  acknowledge  
    and arbitration 5-60  
    bus cycles 5-62  
    arbitration 5-2, 6-3  
    **IARB field**  
      QSM D-25  
      SIM 5-2, 5-3, 5-60, D-7  
      TPU 7-5, D-41  
    exception processing 5-59  
    level (IL)  
      for QSPI (ILQSPI) D-25  
      for SCI (ILSCI) D-25  
    priority  
      and recognition 5-59  
      level field (IPL) 5-68, D-20  
      mask (IP) field 4-6, 5-59, 6-3, 7-5, D-4  
    processing summary 5-61  
    vector  
      number 6-3  
      field (INTV) D-26  
**Interruptions**  
  QSM 6-3  
  SIM 5-58



TPU 7-5  
Inter-transfer delay 6-6  
INTV D-26  
IP 6-3, 7-5  
IPL D-20  
IRQ 5-59, 5-61, 7-5  
ITC 7-6

-L-

Length of delay after transfer (DTL) D-35  
Level-sensitivity 5-59  
LOC D-9  
Logic  
  analyzer pod connectors C-2  
  levels (definition) 2-4  
Loop  
  mode 4-15  
  (LOOPS) D-27  
  instruction sequence 4-15  
LOOPQ D-36  
LOOPS D-27  
Loss of clock reset (LOC) D-9  
Low power stop (LPSTOP)  
  broadcast cycle 5-42  
  CPU space cycle 5-42  
  CPU32 4-15  
  interrupt mask level 5-42  
  SIM 5-27  
  TPU 7-15  
  TPURAM 8-3  
Low-power  
  stop mode enable (STOP)  
    QSM 6-2, D-24  
    TPU D-40  
    TPURAM D-22  
LPSTOP 1-1, 4-15, 5-20, 5-27, 5-42  
LR D-46  
LSB 2-4, 4-4  
LSW 2-4

-M-

M 6-28, D-28  
M68000 family  
  compatibility 4-14  
  development support 4-19  
M68MEVB1632 C-1  
  modular evaluation board (MEVB) C-1  
M68MMDS1632 C-1  
Master  
  /slave mode select (MSTR) D-32  
  shift registers (TSTMSR) D-21  
Maximum system clock 1-1  
MC68010 4-14  
MC68020 4-10, 4-14  
MC68332  
  132-pin package 3-4, B-2  
  144-pin package 3-5, B-3  
  address map 3-14  
  block diagram 3-3

driver types 3-9  
memory maps  
  overall 3-15  
  separate supervisor and user space 3-16  
  supervisor space 3-17  
  user space 3-18

pin  
  characteristics 3-6  
  functions 3-10

MCU personality board (MPB) C-1

Mechanical information B-7

Memory

  CPU32 organization 4-7  
  virtual 4-9

Memory maps

  internal register map 3-14  
  overall 3-15  
  separate supervisor and user space 3-16  
  supervisor space 3-17  
  user space 3-18

Misaligned operand 5-33

MISO 6-18, 6-22

MM D-7

MMDS C-1

Mnemonics

  range (definition) 2-4  
  specific (definition) 2-4

MODCLK 5-4, 5-5, 5-57

MODE 5-67, D-18

Mode

  fault flag (MODF) 6-11, D-37  
  select (M) D-28

MODF 6-11, D-37

Modular platform board C-1

Module

  address map D-1  
  mapping (MM) bit 5-2, D-7  
  pin functions 5-53

Modulus counter 6-28

MOSI 6-18, 6-22

Motorola

*Microcontroller Development Tools Directory*  
    (MCUDEVTLDIR/D Rev. 3) C-1  
  modular development system (MMDS) C-1

MPB C-1

MSB 2-4, 4-4

MSTR D-32

  MSTRST (master reset) 5-49, 5-56, 5-58

MSW 2-4

  Multichannel pulse width modulation (MCPWM) 7-11

  Multimaster operation 6-11

-N-

N (negative) flag 4-6, D-4

Negated (definition) 2-4

New

  input capture/transition counter (NITC) 7-11  
  queue pointer value (NEWQP) D-36

NEWQP 6-10, 6-23, D-36

NF 6-31, D-30



NITC 7-11

Noise

  error (NF) flag 6-31

  error flag (NF) D-30

Nomenclature 2-1

Non-maskable interrupt 5-59

NRZ 6-2

**-O-**

OC 7-7

On-chip breakpoint hardware 4-27

OP (1 through 3) 5-33

Opcode tracking 4-27

Operand

  alignment 5-33

  byte order 5-33

  destination 4-4

  misaligned 5-33

  source 4-4

  transfer cases 5-34

Operators 2-1

OR D-30

Ordering information B-7

Output

  compare (OC) 7-7

Overrun error (OR) D-30

Overview information 3-1

**-P-**

Parallel I/O ports 5-72

Parentheses (definition) 2-4

Parity

  checking 6-29

  enable (PE) D-28

  error (PF) bit D-30

  error (PF) flag 6-31

  type (PT) 6-29, D-28

PCBK D-43

PCC 4-23

PCS D-39

  to SCK delay (DSCK) D-38

PCSO/SS 6-22

PE D-28

PEPAR 5-72, D-10

Period

  /pulse width accumulator (PPWA) 7-9

  measurement

    additional transition detect (PMA) 7-7

    missing transition detect (PMM) 7-8

Periodic

  interrupt

    control register (PICR) 5-26, D-13

    modulus counter 5-26

    priority 5-27

    request level (PIRQL) 5-26, D-13

    timer 5-25

      components 5-25

      modulus (PITM field 5-26

      PIT period calculation 5-26, D-14

register (PITR) D-14

timing modulus (PITM) D-14

vector (PIV) 5-26, D-13

timer prescaler control (PTP) 5-26, D-14

Peripheral

  breakpoints 4-21

  chip-selects (PCS) D-39

Peripheral chip-selects (PCS) 6-23

PF 6-31, D-30

PFPAR 5-72, D-12

Phase-locked loop (PLL) 1-1, 5-4

PICR 5-26, 5-61, D-13

Pin

  electrical state 5-54

  function 5-54

  reset states 5-55

PIRQL 5-26, D-13

PITM 5-26, D-14

PITR 5-26, D-14

PIV 5-26, D-13

PLL 1-1, 5-4

PMA 7-7

PMM 7-8

Pointer 6-7

Port

  parallel I/O in SIM 5-72

  replacement unit (PRU) C-2

  size 5-66

Port C data register (PORTC) 5-68, D-15

Port E

  data direction register (DDRE) 5-72, D-10

  data register (PORTE) 5-72, D-10

  pin assignment register (PEPAR) 5-72, D-10

Port F

  data direction register (DDRF) 5-72, D-11

  data register (PORTF) 5-72, D-11

  pin assignment register (PFPAR) 5-72, D-12

PORTC D-15

PORTE 5-72, D-10

PORTF 5-72, D-11

PORTQS 6-4, D-30

Position-synchronized pulse generator (PSP) 7-8

POW D-9

Power

  consumption reduction 5-20

  -up reset (POW) D-9

PPWA 7-9

PQSPAR 6-4, 6-18, 6-22, D-31

Prescaler

  clock

    (PSCK) D-41

  control

    for TCR1 7-13

    for TCR2 7-14

Program counter (PC) 4-1, 4-6

Programmable

  channel service priority 7-4

  time accumulator (PTA) 7-11

  transfer length 6-6

PRU C-2



PSCK 7-13, D-41  
PSP 7-8  
PT 6-29, D-28  
PTA 7-11  
PTP D-14  
Pulse width modulation  
    TPU waveform (PWM) 7-7  
PWM 7-7

-Q-

QDEC 7-10  
QILR 6-2, D-25  
QIVR 6-2, D-25  
QOM 7-11  
QSM  
    address map 6-2, D-23, D-24  
    block diagram 6-1  
    features 3-1  
    general 6-1  
    interrupts 6-3  
    pin function 6-5, D-32  
    QSPI 6-5  
        operating modes 6-10  
        operation 6-9  
        pins 6-9  
        RAM 6-8  
        registers 6-7  
    reference manual 6-1  
    registers  
        command RAM (CR) D-38  
        global registers 6-2  
            interrupt  
                level register (QILR) 6-2, D-25  
                vector register (QIVR) 6-2, D-25  
            test register (QTEST) 6-2  
        module configuration register (QSMCR) D-24  
        pin control registers 6-4  
            port QS  
                data direction register (DDRQS) 6-4, D-31  
                data register (PORTQS) 6-4, D-30  
                pin assignment register (PQSPAR) D-31  
    QSPI  
        control register 0 (SPCR0) D-32  
        control register 1 (SPCR1) D-34  
        control register 2 (SPCR2) D-35  
        control register 3 (SPCR3) D-36  
        status register (SPSR) D-36  
    receive data RAM (RR) D-37  
    SCI  
        control register 0 (SCCR0) D-27  
        control register 1 (SCCR1) D-27  
        data register (SCDR) D-30  
        status register (SCSR) D-29  
    test register (QTEST) D-25  
    transmit data RAM (TR) D-38  
    types 6-2  
SCI 6-23  
    operation 6-27

pins 6-27  
registers 6-24  
QSMCR D-24  
QSPI 6-1, 6-2, 6-5  
    block diagram 6-6  
    command RAM 6-9  
    enable (SPE) D-34  
    finished flag (SPIF) D-37  
    initialization operation 6-12  
    loop mode (LOOPQ) D-36  
    master operation flow 6-13  
    operating modes 6-10  
        master mode 6-10, 6-18  
        wraparound mode 6-21  
        slave mode 6-10, 6-22  
        wraparound mode 6-23  
    operation 6-9  
    peripheral chip-selects 6-23  
    pins 6-9  
    RAM 6-8  
        receive RAM 6-8  
        transmit RAM 6-9  
    registers 6-7  
        control registers 6-7  
        status register 6-8  
QTEST 6-2, D-25  
Quadrature decode (QDEC) 7-10  
Quad-word data 4-4  
Queue pointers  
    completed queue pointer (CPTQP) 6-10  
    end queue pointer (ENDQP) 6-10  
    new queue pointer (NEWQP) 6-10  
Queued  
    output match (QOM) 7-11  
Queued serial  
    module (QSM). *See* QSM 6-1  
    peripheral interface (QSPI) *See* QSPI. 6-1, 6-5

-R-

R/W 5-30, 5-35  
    field 5-68, D-19  
RAF D-29  
RAM  
    array  
        disable (RAMDS) D-23  
    RAMDS 8-1, D-23  
    RASP D-22  
    RDR 6-27  
    RDRF 6-31, D-29  
    RE 6-31, D-28  
Read  
    /write signal (R/W) 5-30  
    cycle 5-36  
        flowchart 5-36  
    system register command (RSREG) 4-22  
Receive  
    data  
        (RXD) pin — QSM 6-27  
        register full (RDRF) D-29  
    RAM 6-8



time sample clock (RT) 6-29, 6-31  
Receiver  
  active (RAF) D-29  
  data register (RDRF) flag 6-31  
  enable (RE) 6-31, D-28  
  interrupt enable (RIE) D-28  
  wakeup (RWU) 6-32, D-28  
Register bit and field mnemonics 2-2  
RESET 4-20, 5-48, 5-50, 5-54, 5-56  
Reset  
  control logic in SIM 5-48  
  exception processing 5-48  
  mode selection  
    use in determining SIM configuration 5-49  
  module pin function out of reset 5-53  
  operation in SIM 5-48  
  power-on 5-56  
  processing summary 5-58  
  source summary in SIM 5-49  
  states of pins assigned to other MCU modules 5-55  
  status register (RSR) 5-22, 5-58, D-9  
  timing 5-56  
Retry operation 5-45  
RIE D-28  
RMC 5-46  
RPC 4-23  
RR D-37  
RS-232C terminal C-2  
RSR 5-22, D-9  
RSREG 4-22  
RT 6-31  
RTE 5-44  
RWU 6-32, D-28  
RXD (QSM) 6-27

-S-

S D-4  
SBK 6-30, D-29  
SCBR D-27  
SCCR 6-24  
SCCR0 D-27  
SCCR1 D-27  
SCDR 6-27, D-30  
SCI 6-1, 6-2, 6-18, 6-23  
  baud  
    clock 6-28  
    rate (SCBR) D-27  
    equation D-27  
  idle-line detection 6-32  
  internal loop 6-33  
  operation 6-27  
  parity checking 6-29  
  pins (QSM) 6-27  
  receiver  
    block diagram  
    QSM 6-26  
    operation 6-31  
    wakeup 6-32  
  registers 6-24  
    control registers — QSM (SCCR) 6-24

data register  
  QSM (SCDR) 6-27  
status register  
  QSM (SCSR) 6-27  
transmitter  
  block diagram  
  QSM 6-25  
  operation 6-29  
SCK 6-18, 6-22  
  actual delay before SCK (equation) 6-19  
  baud rate (equation) 6-19  
SCSR 6-27, D-29  
Send break (SBK) 6-30, D-29  
Serial  
  clock baud rate (SPBR) D-34  
  communication interface (SCI) 6-1, 6-23  
  formats 6-28  
  interface 4-24  
  mode (M) bit 6-28  
  shifter 6-27, 6-29  
Service  
  request breakpoint flag (SRBK) D-43  
Set (definition) 2-4  
SFC 4-7  
SGLR D-47  
SHEN 5-47, D-7  
Show cycle  
  enable (SHEN) 5-3, 5-47, D-7  
  operation 5-47  
SIM 5-1  
  address map D-5  
  block diagram 5-2  
  bus operation 5-34  
  chip-selects 5-62  
  external bus interface (EBI) 5-27  
  features 3-1  
  functional blocks 5-1  
  halt monitor 5-23  
  interrupt arbitration 5-3  
  interrupts 5-58  
  low-power stop operation 5-27  
  module configuration register (SIMCR) D-6  
  parallel I/O ports 5-72  
  periodic interrupt timer 5-25  
    block diagram (with software watchdog) 5-25  
  register access 5-3  
registers  
  chip-select  
    base address  
      register boot ROM (CSBARBT) D-17  
      registers (CSBAR) 5-65, 5-66, D-17  
  option  
    register boot ROM (CSORBT) D-18  
    registers (CSOR) 5-65, 5-67, D-18  
    pin assignment registers (CSPAR) 5-65, D-15  
  clock synthesizer control register (SYNCR) D-8  
  distributed register (DREG) D-22  
  master shift register A/B (TSTMSRA/B) D-21  
  module configuration register (SIMCR) 5-2



periodic interrupt  
    control register (PICR) D-13  
    timer register (PITR) 5-26, D-14  
port C data register (PORTC) 5-68, D-15  
port E  
    data direction register (DDRE) 5-72, D-10  
    data register (PORTE) 5-72, D-10  
    pin assignment register (PEPAR) 5-72,  
        D-10  
port F  
    data direction register (DDRF) 5-72, D-11  
    data register (PORTF) 5-72, D-11  
    pin assignment register (PFPAR) 5-72,  
        D-12  
reset status register (RSR) D-9  
software service register (SWSR) D-15  
system  
    integration  
        test register - ECLK (SIMTRE) D-9  
        test register (SIMTR) D-8  
    protection control register (SYPCR) D-12  
test  
    module  
        repetition count (TSTRC) D-21  
        shift count register (TSTSC) D-21  
    submodule control register (CREG) D-22  
reset 5-48  
    state of pins 5-54  
software watchdog 5-23  
    block diagram (with PIT) 5-23  
spurious interrupt monitor 5-23  
system  
    clock 5-4  
        block diagram 5-4  
        synthesizer operation 5-5  
    configuration 5-2  
    protection 5-21  
*SIM Reference Manual* 5-62  
SIMCR 5-2, 8-1, D-6  
SIMTR D-8  
SIMTRE D-9  
SIZ 5-30, 5-33, 5-48  
Size signals (SIZ) 5-30  
    encoding 5-30  
Slave select signal ( $\overline{SS}$ ). *See*  $\overline{SS}$  6-22  
SLOCK 5-6, D-8  
Slow reference frequency 5-4, 5-26, D-14  
SM 7-9  
Software  
    breakpoints 5-39  
    service register (SWSR) D-15  
watchdog 5-23  
    block diagram 5-25  
    clock rate 5-24  
    enable (SWE) D-12  
    enable (SWE) bit 5-23  
    prescale (SWP) D-12  
    prescale (SWP) bit 5-24  
    ratio of SWP and SWT bits 5-24  
    reset (SW) D-9  
timeout period calculation 5-24  
timing field (SWT) 5-24, D-13  
SPACE (address space select) 5-68, D-20  
SPBR D-34  
SPCR0 D-32  
SPCR1 D-34  
SPCR2 D-35  
SPCR3 D-36  
SPE 6-7, D-34  
SPI 4-25  
    finished interrupt enable (SPIFIE) D-35  
SPIF D-37  
SPIFIE D-35  
SPSR D-36  
SPWM 7-7  
SR 4-6  
SRBK D-43  
 $\overline{SS}$  6-22, 6-23  
SSP 4-10  
Stack pointer (SP) 4-1  
Standard  
    nonreturn to zero (NRZ) 6-2  
Standby RAM module w/ TPU emulation (TPURAM). *See* TPURAM 8-1  
Start bit (beginning of data frame) 6-27  
State machine 6-31  
Stepper motor (SM) 7-9  
STEXT 5-20, D-9  
STF D-41  
STOP 6-2, D-22, D-24, D-40  
Stop  
    clocks to TCRs (CLKS) D-42  
    enable (STOP) bit  
        QSM 6-2  
        TPU 7-15  
    flag (STF) D-41  
    mode  
        external clock (STEXT) 5-20, D-9  
        SIM clock (STSIM) 5-20, D-9  
        SCI end of data frame bit 6-27  
STRB (address strobe/data strobe) bit 5-38, 5-68, D-19  
STSIM 5-20, D-9  
Supervisor  
    /unrestricted data space (SUPV)  
        CPU32 D-4  
        QSM D-25  
        SIM 5-3, D-7  
        TPU D-41  
        stack pointer (SSP) 4-10  
    SUPV 5-3, D-25  
    SW D-9  
    SWE 5-23, D-12  
    SWP 5-24, D-12  
    SWSR D-15  
    SWT 5-24, D-13  
    Symbols 2-1  
    Synchronized pulse width modulation (SPWM) 7-7  
    SYNCR D-8  
    Synthesizer lock flag (SLOCK) D-8  
    SYPCR D-12



SYS D-9  
SYSRST (system reset) 5-49  
System  
  clock 1-1, 5-4  
  block diagram 5-4  
  output (CLKOUT) 5-34  
  sources 5-4  
frequencies  
  16.78 MHz 5-14  
  20.97 MHz 5-16  
  25.17 MHz 5-18  
integration  
  module. *See* SIM D-5  
  module. *See* SIM 5-1  
  test register - ECLK (SIMTRE) D-9  
memory maps. *See* Memory maps 3-14  
protection control register (SYPCR) D-12  
reset (SYS) D-9

-T-

T D-3  
T2CG 7-14, D-41  
Table stepper motor (TSM) 7-10  
TBL 4-15  
TC 6-30, D-29  
TCIE 6-31, D-28  
TCR D-41  
TCR1P 7-13, D-40  
TCR2 clock/gate control (T2CG) D-41  
TCR2P D-40  
TDR 6-27  
TDRE 6-30, D-29  
TE D-28  
Temporary register A (ATEMP) 4-21  
Test  
  module  
    repetition count (TSTRC) D-21  
    shift count register (TSTSC) D-21  
  submodule  
    control register (CREG) D-22  
    reset (TST) D-9  
Three-state control (TSC) 5-57  
TICR 7-13, D-43  
TIE 6-31, D-28  
Time  
  processor unit. *See* TPU 7-1  
Timer  
  count register  
    1 prescaler control (TCR1P) D-40  
    2 prescaler control (TCR2P) D-40  
TPU  
  A mask functions 7-6  
  discrete input/output (DIO) 7-6  
  input capture/input transition counter (ITC) 7-6  
  output compare (OC) 7-7  
  period  
    /pw accumulator (PPWA) 7-9  
  measurement  
    add transition detect (PMA) 7-7  
    missing transition detect (PMM) 7-8

position-synch pulse generator (PSP) 7-8  
pulse width modulation (PWM) 7-7  
quadrature decode (QDEC) 7-10  
stepper motor (SM) 7-9  
synch pw modulation (SPWM) 7-7  
address map D-39  
block diagram 7-1  
components 7-2  
features 3-2  
FREEZE flag (TPUF) D-43  
function library 7-5  
G mask functions 7-10  
  brushless motor commutation (COMM) 7-12  
  fast quadrature decode (FQD) 7-12  
  frequency measurement (FQM) 7-13  
  hall effect decode (HALLD) 7-13  
  multichannel pulse width modulation (PCPWM)  
    7-11  
  new input capture/transition counter (NITC) 7-11  
  programmable time accumulator (PTA) 7-11  
  queued output match (QOM) 7-11  
  table stepper motor (TSM) 7-10  
  universal asynchronous receiver/transmitter  
    (UART) 7-12  
host interface 7-3  
interrupts 7-5  
microengine 7-3  
operation 7-3  
  coherency 7-4  
  emulation support 7-5  
  event timing 7-3  
  interchannel communication 7-4  
  programmable channel service priority 7-4  
overview 7-1  
parameter RAM 7-3, D-47  
  address map D-47  
registers  
  channel  
    function select registers (CSR) D-44  
  interrupt  
    enable register (CIER) 7-5, D-44  
    status register (CISR) 7-5, D-46  
    priority registers (CPR) D-46  
  decoded channel number register (DCNR) D-47  
development  
  support control register (DSCR) D-41  
  support status register (DSSR) D-42  
host  
  sequence registers (HSQR) D-45  
  service request registers (HSSR) D-45  
link register (LR) D-46  
module configuration register (TPUMCR) D-40  
service grant latch register (SGLR) D-47  
test configuration register (TCR) D-41  
TPU interrupt configuration register (TICR) D-43  
scheduler 7-3  
time  
  bases 7-2  
  timer channels 7-2  
  timing (electricals) A-43

**TPU Reference Manual** 7-3, 7-17  
**TPUF** D-43  
**TPUMCR** 7-13, D-40  
**TPURAM**  
 address map D-22  
 array  
     address mapping 8-1  
     base address (ADDR) D-23  
     space (RASP) D-22  
 features 3-2  
 general 8-1  
 operation  
     normal 8-2  
     standby 8-2  
 privilege level 8-2  
 register block 8-1  
 registers  
     base address and status register (TRAMBAR) D-23  
     module configuration register (TRAMMCR) D-22  
     test register (TRAMTST) D-23  
 reset 8-3  
 TPU microcode emulation 8-3  
**TR** D-38  
**Trace**  
 enable field (T) D-3  
 on instruction execution 4-19  
**TRAMBAR** 8-1, D-23  
**TRAMMCR** 8-1, D-22  
**TRAMTST** 8-1, D-23  
 Transfer length options 6-19  
 Transition-sensitivity 5-59  
**Transmit**  
 complete  
     (TC) flag  
     QSM 6-30  
 bit (TC) D-29  
 interrupt enable (TCIE) D-28  
     QSM 6-31  
 data  
     (TXD) pin — QSM 6-27  
     register empty (TDRE) flag D-29  
     QSM 6-30  
 enable (TE)  
     QSM 6-29  
 interrupt enable (TIE) D-28  
     QSM 6-31  
 RAM 6-9  
 Transmitter enable (TE) D-28  
**TSC** 5-57  
**TSM** 7-10  
**TST** D-9  
**TSTMSR** D-21  
**TSTRC** D-21  
**TSTSC** D-21  
**TXD** (QSM) 6-27

**-U-**

UART 7-12  
 Unimplemented instruction emulation 4-19

Universal asynchronous receiver/transmitter (UART) 7-12  
**User stack pointer (USP)** 4-10  
*Using the TPU Function Library and TPU Emulation Mode* 7-5  
**USP** 4-10

**-V-**

V (overflow) flag 4-6, D-4  
**VBR** 4-7, 4-16  
 VCO frequency ( $f_{VCO}$ ) 5-6  
**V<sub>DD</sub>** 5-56, 8-1  
     ramp time 5-57  
**V<sub>DDSYN</sub>** 5-5, 5-56  
 Vector base register (VBR) 3-14, 4-7, 4-16, 5-59  
 Virtual memory 4-9  
**Voltage**  
     controlled oscillator (VCO) 5-6  
     frequency ramp time 5-57  
**V<sub>PP</sub>** C-2  
**V<sub>SS</sub>** 8-2  
**V<sub>STBY</sub>** 8-1, 8-2

**-W-**

W bit D-8  
**WAKE** 6-33, D-28  
**Wakeup**  
     address mark (WAKE) 6-33, D-28  
     functions 6-2  
**Wired-OR**  
 mode  
     for QSPI pins (WOMQ) D-33  
     for SCI pins (WOMS) D-28  
     QSM 6-29  
**WOMQ** D-33  
**WOMS** 6-29, D-28  
**Wrap**  
     enable (WREN) D-35  
     to (WRTO) D-35  
**Wraparound mode** 6-7  
     master 6-21  
     slave 6-23  
**WREN** D-35  
**Write cycle** 5-37  
     flowchart 5-37  
**WRTO** D-35

**-X-**

**X**  
     (extract) flag 4-6, D-4  
     bit in SYNCR D-8  
**XFC** 5-6  
**XTRST** (external reset) 5-48

**-Y-**

Y field D-8



**-Z-**

Z (zero) flag 4-6, D-4

