



Figure Number	LIST OF FIGURES	Page Number
3-1	MC68332 Block Diagram .....	3-3
3-2	MC68332 Pin Assignments for 132-Pin Package .....	3-4
3-3	MC68332 Pin Assignments for 144-Pin Package .....	3-5
3-4	MC68332 Address Map .....	3-14
3-5	Overall Memory Map .....	3-15
3-6	Separate Supervisor and User Space Map .....	3-16
3-7	Supervisor Space (Separate Program/Data Space) Map .....	3-17
3-8	User Space (Separate Program/Data Space) Map .....	3-18
4-1	CPU32 Block Diagram .....	4-2
4-2	User Programming Model .....	4-3
4-3	Supervisor Programming Model Supplement .....	4-4
4-4	Data Organization in Data Registers .....	4-5
4-5	Address Organization in Address Registers .....	4-6
4-6	Memory Operand Addressing .....	4-8
4-7	Loop Mode Instruction Sequence .....	4-15
4-8	Common In-Circuit Emulator Diagram .....	4-20
4-9	Bus State Analyzer Configuration .....	4-20
4-10	Debug Serial I/O Block Diagram .....	4-25
4-11	BDM Serial Data Word .....	4-26
4-12	BDM Connector Pinout .....	4-26
5-1	System Integration Module Block Diagram .....	5-2
5-2	System Clock Block Diagram .....	5-4
5-3	System Clock Oscillator Circuit .....	5-5
5-4	System Clock Filter Networks .....	5-6
5-5	LPSTOP Flowchart .....	5-21
5-6	System Protection Block .....	5-22
5-7	Periodic Interrupt Timer and Software Watchdog Timer .....	5-25
5-8	MCU Basic System .....	5-28
5-9	Operand Byte Order .....	5-33
5-10	Word Read Cycle Flowchart .....	5-36
5-11	Write Cycle Flowchart .....	5-37
5-12	CPU Space Address Encoding .....	5-39
5-13	Breakpoint Operation Flowchart .....	5-41
5-14	LPSTOP Interrupt Mask Level .....	5-42
5-15	Bus Arbitration Flowchart for Single Request .....	5-47
5-16	Preferred Circuit for Data Bus Mode Select Conditioning .....	5-51
5-17	Alternate Circuit for Data Bus Mode Select Conditioning .....	5-52
5-18	Power-On Reset .....	5-57
5-19	Basic MCU System .....	5-63
5-20	Chip-Select Circuit Block Diagram .....	5-64
5-21	CPU Space Encoding for Interrupt Acknowledge .....	5-69

<b>Figure Number</b>		<b>Page Number</b>
6-1	QSM Block Diagram .....	6-1
6-2	QSPI Block Diagram .....	6-6
6-3	QSPI RAM .....	6-8
6-4	Flowchart of QSPI Initialization Operation .....	6-12
6-5	Flowchart of QSPI Master Operation (Part 1) .....	6-13
6-6	Flowchart of QSPI Master Operation (Part 2) .....	6-14
6-7	Flowchart of QSPI Master Operation (Part 3) .....	6-15
6-8	Flowchart of QSPI Slave Operation (Part 1) .....	6-16
6-9	Flowchart of QSPI Slave Operation (Part 2) .....	6-17
6-10	SCI Transmitter Block Diagram .....	6-25
6-11	SCI Receiver Block Diagram .....	6-26
7-1	TPU Block Diagram .....	7-1
7-2	TCR1 Prescaler Control .....	7-14
7-3	TCR2 Prescaler Control .....	7-14
A-1	CLKOUT Output Timing Diagram .....	A-21
A-2	External Clock Input Timing Diagram .....	A-21
A-3	ECLK Output Timing Diagram .....	A-21
A-4	Read Cycle Timing Diagram .....	A-22
A-5	Write Cycle Timing Diagram .....	A-23
A-6	Fast Termination Read Cycle Timing Diagram .....	A-24
A-7	Fast Termination Write Cycle Timing Diagram .....	A-25
A-8	Bus Arbitration Timing Diagram — Active Bus Case .....	A-26
A-9	Bus Arbitration Timing Diagram — Idle Bus Case .....	A-27
A-10	Show Cycle Timing Diagram .....	A-28
A-11	Chip-Select Timing Diagram .....	A-29
A-12	Reset and Mode Select Timing Diagram .....	A-29
A-13	BDM Serial Communication Timing Diagram .....	A-32
A-14	BDM Freeze Assertion Timing Diagram .....	A-32
A-15	ECLK Timing Diagram .....	A-37
A-16	QSPI Timing — Master, CPHA = 0 .....	A-41
A-17	QSPI Timing — Master, CPHA = 1 .....	A-41
A-18	QSPI Timing — Slave, CPHA = 0 .....	A-42
A-19	QSPI Timing — Slave, CPHA = 1 .....	A-42
A-20	TPU Timing Diagram .....	A-43
B-1	MC68332 Pin Assignments for 132-Pin Package .....	B-2
B-2	MC68332 Pin Assignments for 144-Pin Package .....	B-3
B-3	132-Pin Package Dimensions — Case 831A-01 .....	B-4
B-4	144-Pin Package Dimensions — Case 863C-01 .....	B-5
B-5	144-Pin Package Dimensions Thin Quad Flat Pack — Case 918-02 .....	B-6
D-1	User Programming Model .....	D-2
D-2	Supervisor Programming Model Supplement .....	D-3

