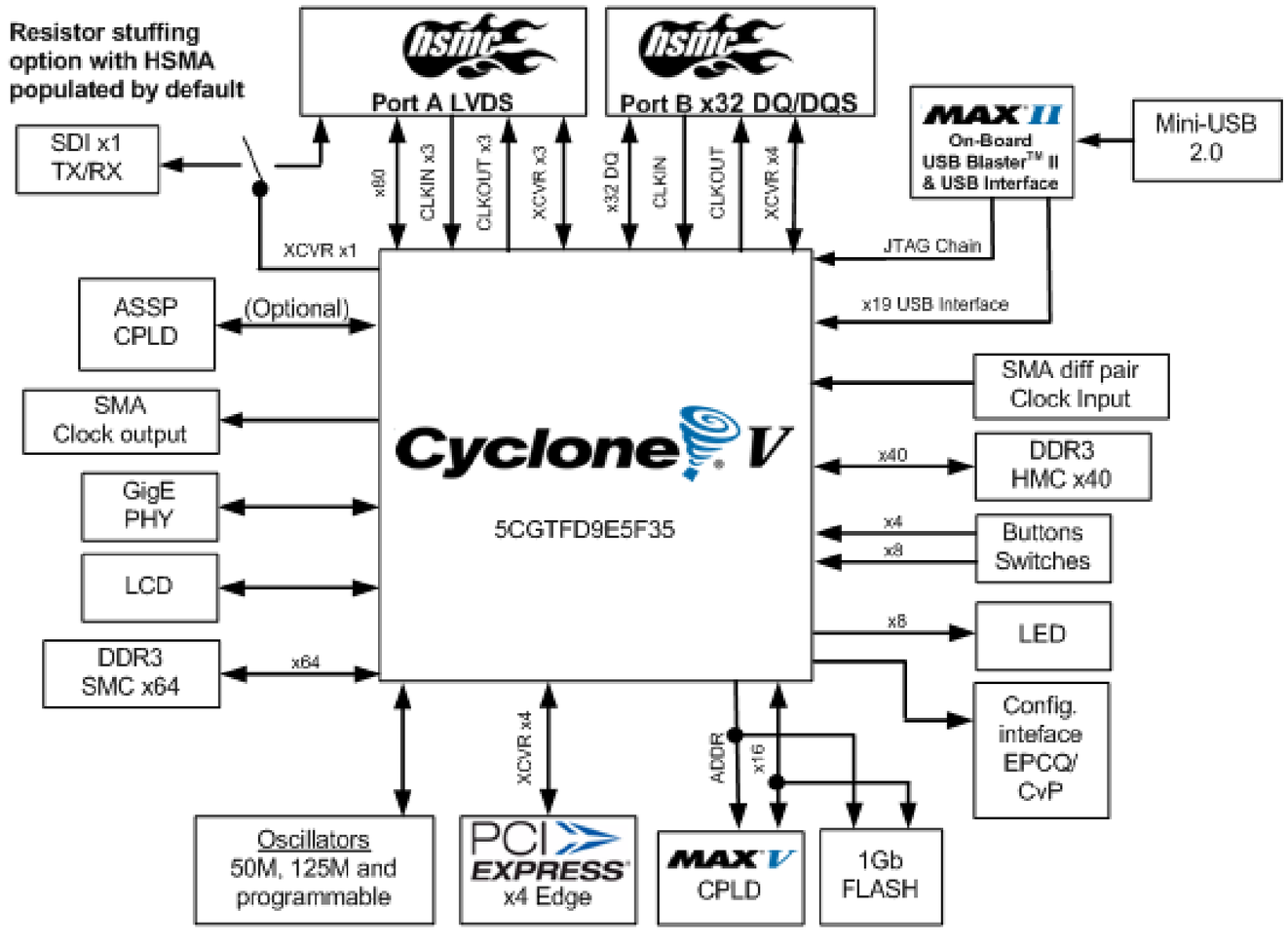
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321004-B1
Gerber Files	110-0321004-B1
PCB Design Files	120-0321004-B1
Assembly Drawing	130-0321004-B1
Fab Drawing	140-0321004-B1
Schematic Drawing	150-0321004-B1
PCB Film	160-0321004-B1
Bill of Materials	170-0321004-B1
Schematic Design Files	180-0321004-B1
Functional Specification	210-0321004-B1
PCB Layout Guidelines	220-0321004-B1
Assembly Rework	320-0321004-B1

2. 1129 Parts, 106 Library Parts, 1085 Nets, 5532 Pins

Cyclone V GT Development Kit Board



REV	DATE	PAGES	DESCRIPTION
A	1/04/2013	All	Released Rev A
B	3/15/2013	All	Released Rev B - Swap HSMA/B Dip switch position, Changed ASSP MAX II device to M100, Changed EPCQ, Rerouted JTAG signals and added filter to TCK, Changed LCD to include SPI option, Changed Flash connections and translator device, Moved C170 to top of board.

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone V GT FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0321004-B1 (6XX-44179R)	B

Date: Thursday, May 02, 2013 Sheet 1 of 30

Package Top View

BANK 8A

VCCIO = 2.5V

HSMC Port A - LVDS

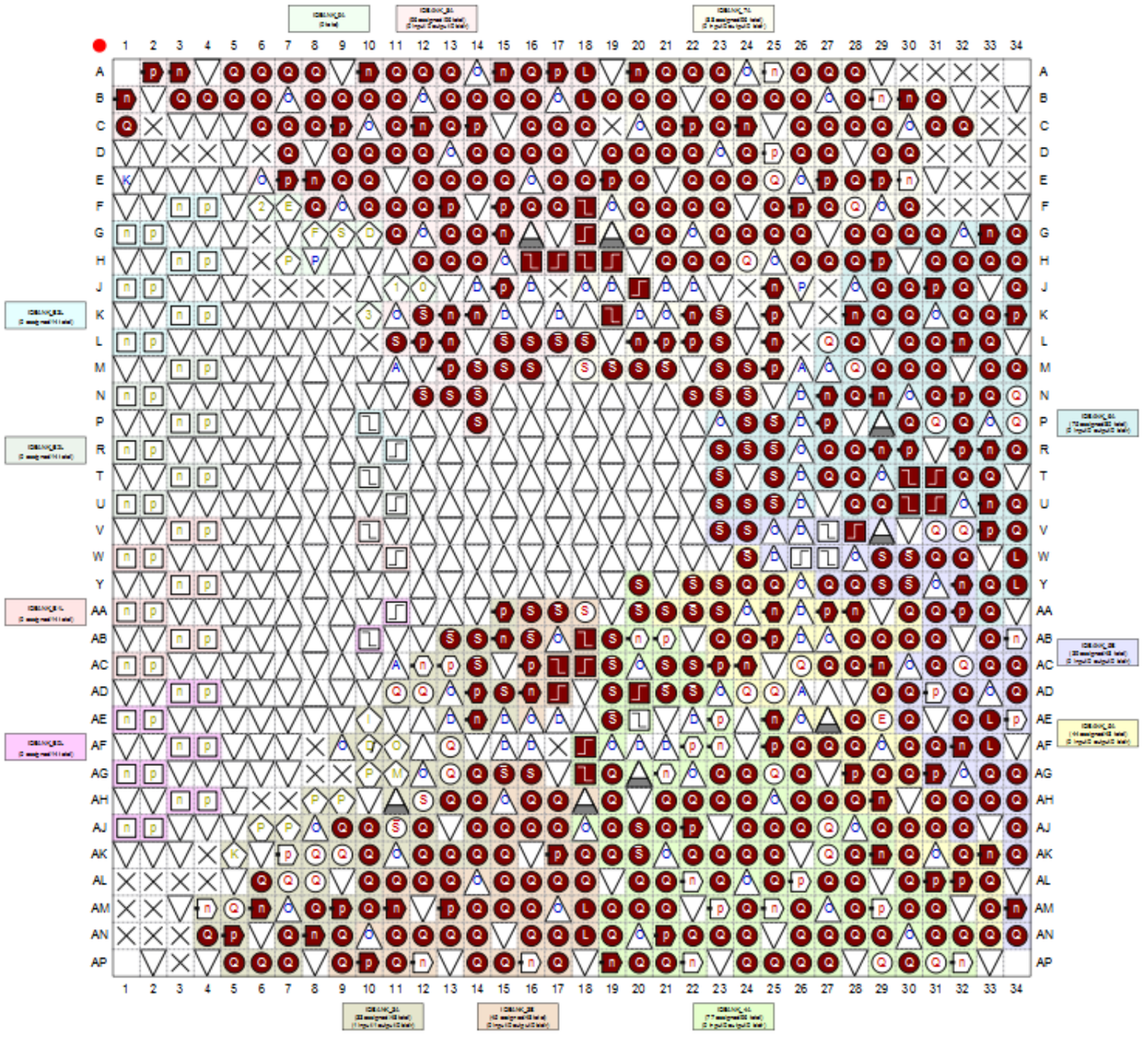
BANK 7A

VCCIO = Variable (Default = 2.5V)

HSMC Port B - x32 DQ/DQS

Top View - Wire Bond

Cyclone V - 5CGTFD9E5F35C7



XCVR BANKS QL2, QL3

HSMC Port A x2

HSMC Port B x4

Hardware Option

SDI x1

XCVR BANKS QL0, QL1

PCIe x4

HSMC Port A x2

BANK 5B / 6A

VCCIO = 1.5V

DDR3B X64

(SMC)

BANK 5A

VCCIO = 1.8V

Flash

BANK 3A

VCCIO = 2.5V

Ethernet, PCIe,
User I/O

BANK 3B

VCCIO = 1.5V

USB Blaster II
DDR3 x32
(HMC)

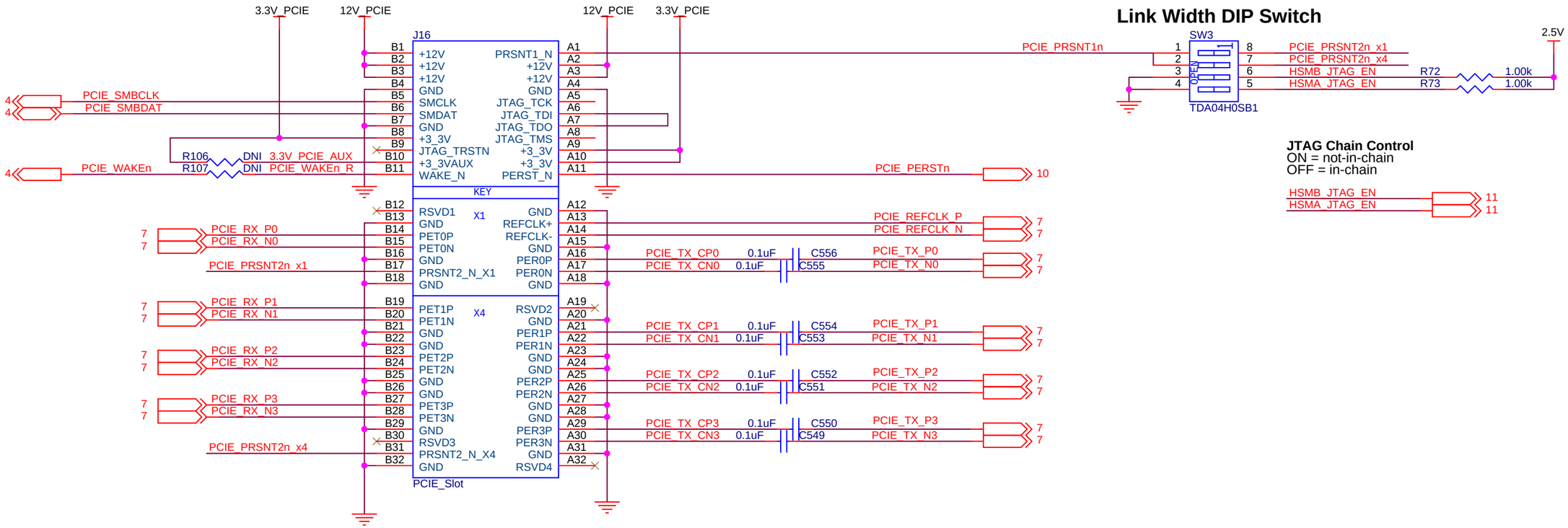
BANK 4A

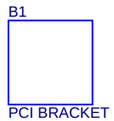
VCCIO = 1.5V

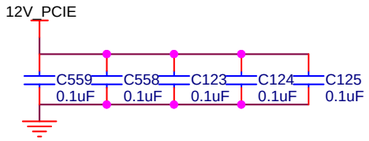
DDR3 x32
(HMC)

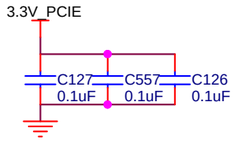
Title: Cyclone V GT FPGA Development Kit Board		
Size: B	Document Number: 150-0321004-B1 (6XX-44179R)	Rev: B
Date: Thursday, May 02, 2013	Sheet 2 of 30	

PCI Express Edge Connector









Title: **Cyclone V GT FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0321004-B1 (6XX-44179R)	B

Date: Thursday, May 02, 2013 Sheet 3 of 30

Cyclone V GT Banks 3 and 4

SDI INTERFACE

SDI_A_TX_EN	15,16
SDI_A_RX_BYPASS	15,16
SDI_A_RX_EN	15,16
SDI_A_TX_SD_HDn	16

U13A

Cyclone V GT Bank 3

Bank 3A *VCCIO = 2.5V*

DISP_I2C_SCL	AL6	DQ2B/DIFFIO_TX_B9p	DQ3B/DIFFIO_TX_B17p	AM8	ENET_MDC
DISP_I2C_SDA	AJ10	DQ2B/DIFFIO_RX_B10p	DQ3B/DIFFIO_RX_B18p	AG14	ENET_MDIO
ENET_INTn	AK10	DQ2B/DIFFIO_RX_B10n	DQ3B/DIFFIO_RX_B18n	AH14	ENET_RX_DV
SDI_A_RX_EN	AN4	DQ2B/DIFFIO_TX_B12n	DQ3B/DIFFIO_TX_B20n	AN9	ENET_RESETn
PCIE_WAKEn	AP6	DQ2B/DIFFIO_TX_B13p	DQ3B/DIFFIO_TX_B21p	AL10	ENET_RX_D1
PCIE_SMBCLK	AP5	DQ2B/DIFFIO_TX_B13n	DQ3B/DIFFIO_TX_B21n	AM10	ENET_RX_CLK
DISP_SPISS	AH13	DQ2B/DIFFIO_RX_B14p	DQ3B/DIFFIO_RX_B22p	AJ14	ENET_RX_D2
PCIE_SMBDAT	AJ12	DQ2B/DIFFIO_RX_B14n	DQ3B/DIFFIO_RX_B22n	AK14	ENET_RX_D0
	AN7	DQ2B/DIFFIO_TX_B16p	DQ3B/DIFFIO_TX_B24p	AK13	USER_PB0
ENET_GTX_CLK	AP7	DQ2B/DIFFIO_TX_B16n	DQ3B/DIFFIO_TX_B24n	AK12	ENET_RX_D3
ENET_TX_D0	AB14			AD15	ENET_TX_D1
ENET_TX_D3	AB13	DQS2B/DIFFIO_RX_B11p	DQS3B/DIFFIO_RX_B19p	AC14	ENET_TX_EN
		DQSn2B/DIFFIO_RX_B11n	DQSn3B/DIFFIO_RX_B19n		
	AD14			AM6	SDI_A_TX_EN
	AE14	DIFFIO_RX_B15p	DIFFIO_TX_B9n	AN5	SDI_A_TX_SD_HDn
USER_PB1	AA15	DIFFIO_RX_B15n	DIFFIO_TX_B12p	AN8	USER_PB2
ENET_TX_D2	AB15	DIFFIO_RX_B23p	DIFFIO_TX_B17n	AM9	SDI_A_RX_BYPASS
		DIFFIO_RX_B23n	DIFFIO_TX_B20p		

Bank 3B (HMC) *VCCIO = 1.5V*

DDR3A_BA0	AN16	HMC_B_BA_0/DQ6B/DIFFIO_TX_B41p	HMC_B_A_8/DQ5B/DIFFIO_RX_B38p	AH16	DDR3A_A8
DDR3A_BA1	AN17	HMC_B_BA_1/DQ6B/DIFFIO_RX_B42p	HMC_B_A_9/DQ5B/DIFFIO_RX_B38n	AJ16	DDR3A_A9
DDR3A_BA2	AP17	HMC_B_BA_2/DQ6B/DIFFIO_RX_B42n	HMC_B_A_10/DQ5B/DIFFIO_TX_B37p	AL16	DDR3A_A10
DDR3A_A0	AK18	HMC_B_A_0/DQ6B/DIFFIO_TX_B48p	HMC_B_A_11/DQ5B/DIFFIO_TX_B37n	AM16	DDR3A_A11
DDR3A_A1	AL18	HMC_B_A_1/DQ6B/DIFFIO_TX_B48n	HMC_B_A_12/DIFFIO_TX_B36p	AM13	DDR3A_A12
		HMC_B_A_2, 3 at Clock section	HMC_B_A_13/DQ5B/DIFFIO_TX_B36n	AN13	DDR3A_A13
DDR3A_A4	AH17		HMC_B_A_14/DQ5B/DIFFIO_TX_B34p	AM14	FLASH_WEn
DDR3A_A5	AJ17	HMC_B_A_4/DQ6B/DIFFIO_RX_B46p	HMC_B_A_15/DQ5B/DIFFIO_RX_B34n	AN14	USB_OEn
DDR3A_A6	AK17	HMC_B_A_5/DQ6B/DIFFIO_RX_B46n	HMC_B_CASn/DQ5B/DIFFIO_TX_B40p	AP15	DDR3A_CASn
DDR3A_A7	AL17	HMC_B_A_6/DIFFIO_TX_B44p	HMC_B_RASn/DQ5B/DIFFIO_TX_B40n	AP14	DDR3A_RASn
		HMC_B_A_7/DQ6B/DIFFIO_TX_B44n	HMC_B_WEn/DQ5B/DIFFIO_TX_B33p	AN12	DDR3A_WEn
DDR3A_CLK_P	AA18			AA16	DDR3A_CSn
DDR3A_CLK_N	AA17	HMC_B_CK/DQS6B/DIFFIO_RX_B43p	HMC_B_CSn_0/DQS5B/DIFFIO_RX_B35p	AB16	FLASH_RESETn
		HMC_B_CKn/DQSn6B/DIFFIO_RX_B43n	HMC_B_CSn_1/DQSn5B/DIFFIO_RX_B35n		
USB_DATA6	AL11	DQ4B/DIFFIO_TX_B25p	HMC_GND/DIFFIO_TX_B33n	AP12	
USB_DATA5	AL15	DQ4B/DIFFIO_RX_B26p	HMC_GND/DIFFIO_TX_B41n	AP16	
USB_DATA7	AM15	DQ4B/DIFFIO_RX_B26n			
USB_DATA4	AP9	DQ4B/DIFFIO_TX_B28n			
USB_DATA1	AN11	DQ4B/DIFFIO_TX_B29p			
USB_DATA3	AP11	DQ4B/DIFFIO_TX_B29n			
USB_DATA0	AJ15	DQ4B/DIFFIO_RX_B30p	DIFFIO_TX_B25n	AM11	USB_FULL
USB_DATA2	AK15	DQ4B/DIFFIO_RX_B30n	DIFFIO_TX_B28p	AP10	USB_EMPTY
USB_ADDR0	AL12	DQ4B/DIFFIO_TX_B32p	DIFFIO_RX_B31p	AC16	USB_SDA
USB_ADDR1	AL13	DQ4B/DIFFIO_TX_B32n	DIFFIO_RX_B31n	AD16	USB_SCL
FLASH_OEn	AG16				
USB_WRn	AG15	DQS4B/DIFFIO_RX_B27p			
		DQSn4B/DIFFIO_RX_B27n			

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Version = 0.2 Preliminary

U13B

Cyclone V GT Bank 4

Bank 4A *VCCIO = 1.5V*

DDR3A_DQ0	AN19	HMC_B_DQ_0/DQ7B/DIFFIO_RX_B50n	RZQ_0/DIFFIO_TX_B49n	AP19	RZQIN_1_5V
DDR3A_DQ1	AM19	HMC_B_DQ_1/DQ7B/DIFFIO_RX_B50p	HMC_B_DQ_32/DQ11B/DIFFIO_RX_B82n	AH23	DDR3A_DQ32
DDR3A_DQ2	AP20	HMC_B_DQ_2/DQ7B/DIFFIO_TX_B49p	HMC_B_DQ_33/DQ11B/DIFFIO_RX_B82p	AG23	DDR3A_DQ33
DDR3A_DQ3	AP21	HMC_B_DQ_3/DQ7B/DIFFIO_TX_B52n	HMC_B_DQ_34/DQ11B/DIFFIO_TX_B81p	AN32	DDR3A_DQ34
DDR3A_DQ4	AH19	HMC_B_DQ_4/DQ7B/DIFFIO_RX_B54n	HMC_B_DQ_35/DQ11B/DIFFIO_TX_B84n	AN29	DDR3A_DQ35
DDR3A_DQ5	AG19	HMC_B_DQ_5/DQ7B/DIFFIO_RX_B54p	HMC_B_DQ_36/DQ11B/DIFFIO_RX_B86n	AK25	DDR3A_DQ36
DDR3A_DQ6	AJ19	HMC_B_DQ_6/DQ7B/DIFFIO_TX_B53p	HMC_B_DQ_37/DQ11B/DIFFIO_RX_B86p	AJ25	DDR3A_DQ37
DDR3A_DQ7	AM21	HMC_B_DQ_7/DQ7B/DIFFIO_TX_B56n	HMC_B_DQ_38/DQ11B/DIFFIO_TX_B85p	AK28	DDR3A_DQ38
PCIE_LED_X1	AK19	HMC_B_ODT_1/DQ7B/DIFFIO_TX_B53n	HMC_B_DQ_39/DQ11B/DIFFIO_TX_B88n	AM30	DDR3A_DQ39
DDR3A_DM0	AL21	HMC_B_DM_0/DQ7B/DIFFIO_TX_B56p	HMC_B_DM_4/DQ11B/DIFFIO_TX_B88p	AL30	DDR3A_DM4
DDR3A_DQS_P0	AB19	HMC_B_DQS_0/DQS7B/DIFFIO_RX_B51p	HMC_B_DQS_4/DQS11B/DIFFIO_RX_B83p	AC21	DDR3A_DQS_P4
DDR3A_DQS_N0	AC19	HMC_B_DQSn_0/DQSn7B/DIFFIO_RX_B51n	HMC_B_DQSn_4/DQSn11B/DIFFIO_RX_B83n	AD21	DDR3A_DQS_N4
DDR3A_DQ8	AM20	HMC_B_DQ_8/DQ8B/DIFFIO_RX_B58n	HMC_B_ODT_0/DIFFIO_TX_B52p	AN21	DDR3A_ODT
DDR3A_DQ9	AL20	HMC_B_DQ_9/DQ8B/DIFFIO_RX_B58p	HMC_B_CKE_1/DIFFIO_TX_B60p	AM23	USER_LED0
DDR3A_DQ10	AN22	HMC_B_DQ_10/DQ8B/DIFFIO_TX_B57p	HMC_B_RESETn/DIFFIO_TX_B68p	AJ22	DDR3A_RESETn
DDR3A_DQ11	AN23	HMC_B_DQ_11/DQ8B/DIFFIO_TX_B60n			
DDR3A_DQ12	AP24	HMC_B_DQ_12/DQ8B/DIFFIO_RX_B62n		AE25	USER_LED1
DDR3A_DQ13	AP25	HMC_B_DQ_13/DQ8B/DIFFIO_RX_B62p	DIFFIO_RX_B95n	AF25	USER_LED4
DDR3A_DQ14	AN26	HMC_B_DQ_14/DQ8B/DIFFIO_TX_B61p	DIFFIO_RX_B95p	AK29	USER_LED2
DDR3A_DQ15	AN24	HMC_B_DQ_15/DQ8B/DIFFIO_TX_B64n	DIFFIO_TX_B89n	AL31	USER_LED3
DDR3A_CKE	AP26	HMC_B_CKE_0/DQ8B/DIFFIO_TX_B61n	DIFFIO_TX_B92p		
DDR3A_DM1	AM24	HMC_B_DM_1/DQ8B/DIFFIO_TX_B64p			
DDR3A_DQS_P1	AD19	HMC_B_DQS_1/DQS8B/DIFFIO_RX_B59p			
DDR3A_DQS_N1	AE19	HMC_B_DQSn_1/DQSn8B/DIFFIO_RX_B59n			
			DQ12B/DIFFIO_RX_B90n	AH24	ASSP_DATAOUT
DDR3A_DQ16	AP27		DQ12B/DIFFIO_RX_B90p	AG24	ASSP_RANDOM_IN
DDR3A_DQ17	AN27	HMC_B_DQ_16/DQ9B/DIFFIO_RX_B66n	DQ12B/DIFFIO_RX_B94n	AG26	ASSP_CLK
DDR3A_DQ18	AK22	HMC_B_DQ_17/DQ9B/DIFFIO_RX_B66p	DQ12B/DIFFIO_RX_B94p	AG25	ASSP_RUN_IN
DDR3A_DQ19	AJ21	HMC_B_DQ_18/DQ9B/DIFFIO_TX_B65p	DQ12B/DIFFIO_TX_B89p	AJ29	ASSP_SYS_RESET
DDR3A_DQ20	AH21	HMC_B_DQ_19/DQ9B/DIFFIO_TX_B68n	DQ12B/DIFFIO_TX_B92n	AM31	ASSP_SHIFT_EN
DDR3A_DQ21	AH22	HMC_B_DQ_20/DQ9B/DIFFIO_RX_B70n	DQ12B/DIFFIO_TX_B93n	AJ26	ASSP_TEST1
DDR3A_DQ22	AP30	HMC_B_DQ_21/DQ9B/DIFFIO_RX_B70p	DQ12B/DIFFIO_TX_B93p	AH26	ASSP_TEST2
DDR3A_DQ23	AN28	HMC_B_DQ_22/DQ9B/DIFFIO_TX_B69p	DQ12B/DIFFIO_TX_B96n	AJ27	USER_LED5
DDR3A_DM2	AM28	HMC_B_DQ_23/DQ9B/DIFFIO_TX_B72n	DQ12B/DIFFIO_TX_B96p	AH27	USER_LED7
DDR3A_DQS_P2	AJ20	HMC_B_DM_2/DQ9B/DIFFIO_TX_B72p		AC22	USER_LED6
DDR3A_DQS_N2	AK20	HMC_B_DQS_2/DQS9B/DIFFIO_RX_B67p	DQS12B/DIFFIO_RX_B91p	AD22	PCIE_LED_X4
		HMC_B_DQSn_2/DQSn9B/DIFFIO_RX_B67n	DQSn12B/DIFFIO_RX_B91n		
DDR3A_DQ24	AL23			AB21	
DDR3A_DQ25	AK23	HMC_B_DQ_24/DQ10B/DIFFIO_RX_B74n	HMC_GND/DIFFIO_RX_B71p	AB20	
DDR3A_DQ26	AL25	HMC_B_DQ_25/DQ10B/DIFFIO_RX_B74p	HMC_GND/DIFFIO_RX_B71n	AF22	
DDR3A_DQ27	AM26	HMC_B_DQ_26/DQ10B/DIFFIO_TX_B73p	HMC_GND/DIFFIO_RX_B79p	AG21	
DDR3A_DQ28	AK24	HMC_B_DQ_27/DQ10B/DIFFIO_TX_B76n	HMC_GND/DIFFIO_RX_B79n	AE23	
DDR3A_DQ29	AJ24	HMC_B_DQ_28/DQ10B/DIFFIO_RX_B78n	HMC_GND/DIFFIO_RX_B87p	AF23	
DDR3A_DQ30	AN31	HMC_B_DQ_29/DQ10B/DIFFIO_RX_B78p	HMC_GND/DIFFIO_RX_B87n	AP22	
DDR3A_DQ31	AL28	HMC_B_DQ_30/DQ10B/DIFFIO_TX_B77p	HMC_GND/DIFFIO_TX_B57n	AL22	
DDR3A_DM3	AL27	HMC_B_DQ_31/DQ10B/DIFFIO_TX_B80n	HMC_GND/DIFFIO_TX_B65n	AM25	
		HMC_B_DM_3/DQ10B/DIFFIO_TX_B80p	HMC_GND/DIFFIO_TX_B73n	AL26	
DDR3A_DQS_P3	Y20		HMC_GND/DIFFIO_TX_B76p	AP32	
DDR3A_DQS_N3	AA20	HMC_B_DQS_3/DQS10B/DIFFIO_RX_B75p	HMC_GND/DIFFIO_TX_B81n	AM29	
		HMC_B_DQSn_3/DQSn10B/DIFFIO_RX_B75n	HMC_GND/DIFFIO_TX_B84p	AP29	
			HMC_GND/DQ9B/DIFFIO_TX_B69n	AP31	
			HMC_GND/DQ10B/DIFFIO_TX_B77n	AK27	
			HMC_GND/DQ11B/DIFFIO_TX_B85n		

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Version = 0.2 Preliminary

AP19 RZQIN_1_5V — 100, 1% — R272

DDR3A x40 HMC INTERFACE

DDR3A_DQ[39:0]	12
DDR3A_A[13:0]	9,12
DDR3A_DQS_P[4:0]	12
DDR3A_DQS_N[4:0]	12
DDR3A_DM[4:0]	12
DDR3A_BA[2:0]	12
DDR3A_CSn	12
DDR3A_CASn	12
DDR3A_CKE	12
DDR3A_WEn	12
DDR3A_RASn	12
DDR3A_ODT	12
DDR3A_RESETn	12
DDR3A_CLK_P	12
DDR3A_CLK_N	12

USB INTERFACE

USB_DATA[7:0]	19
USB_ADDR[1:0]	19
USB_SDA	19
USB_SCL	19
USB_RESETn	9,19
USB_OEn	19
USB_RDn	9,19
USB_WRn	19
USB_FULL	19
USB_EMPTY	19

ETHERNET INTERFACE

ENET_TX_D[3:0]	17
ENET_RX_D[3:0]	17
ENET_GTX_CLK	17
ENET_TX_EN	17
ENET_RX_DV	17
ENET_RX_CLK	17
ENET_INTn	17
ENET_RESETn	17
ENET_MDIO	17
ENET_MDC	17

PCIE INTERFACE

PCIE_LED_X1	20
PCIE_LED_X4	20
PCIE_WAKEn	3
PCIE_SMBCLK	3
PCIE_SMBDAT	3

MVE ASSP Core Interface

ASSP_TEST1	21
ASSP_TEST2	21
ASSP_SHIFT_EN	21
ASSP_DATAOUT	21
ASSP_RANDOM_IN	21
ASSP_CLK	21
ASSP_RUN_IN	21
ASSP_SYS_RESET	21

FLASH INTERFACE

FLASH_RESETn	14,15
FLASH_WEn	14,15
FLASH_OEn	14,15

DISPLAY INTERFACE

DISP_I2C_SDA	20
DISP_I2C_SCL	20
DISP_SPISS	20

USER INTERFACE

USER_LED[7:0]	20
USER_PB[2:0]	20

Title	Cyclone V GT FPGA Development Kit Board	
Size B	Document Number 150-0321004-B1 (6XX-44179R)	Rev B
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Cyclone V GT Banks 5 and 6

U13C

Cyclone V GT Bank 5

VCCIO =1.8V

Bank 5A

		DQ1R/RZQ_1/DIFFIO_TX_R1p	AD24	FM_A26	
FM_A8	AF27	DQ2R/DIFFIO_TX_R10p	AK30	FM_A18	DQ3R/DIFFIO_TX_R18p
FM_A9	AF26	DQ2R/DIFFIO_TX_R10n	AJ30	FM_A19	DQ3R/DIFFIO_TX_R18n
FM_A10	AB28	DQ2R/DIFFIO_RX_R11p	AG30	FM_A20	DQ3R/DIFFIO_RX_R19p
FM_A12	AB29	DQ2R/DIFFIO_RX_R11n	AF30	FM_A22	DQ3R/DIFFIO_RX_R19n
FM_A11	AE28	DQ2R/DIFFIO_TX_R12p	AN33	FM_A21	DQ3R/DIFFIO_TX_R20p
FM_A13	AF28	DQ2R/DIFFIO_TX_R12n	AM33	FM_A23	DQ3R/DIFFIO_TX_R20n
FM_A14	AH28	DQ2R/DIFFIO_TX_R14n	AK32	FM_A24	DQ3R/DIFFIO_TX_R22n
FM_A15	AB30	DQ2R/DIFFIO_RX_R15p	AH31	FM_A25	DQ3R/DIFFIO_RX_R23p
FM_A17	AA30	DQ2R/DIFFIO_RX_R15n	AJ31	FM_D0	DQ3R/DIFFIO_RX_R23n
FM_A16	AG29	DQ2R/DIFFIO_TX_R16p	AL33	FM_D15	DQ3R/DIFFIO_TX_R24p
FM_D1	AA23		Y23	FM_D2	
FM_D3	Y22	DQS2R/DIFFIO_RX_R13p	W24	FM_D4	DQS3R/DIFFIO_RX_R21p
		DQSn2R/DIFFIO_RX_R13n			DQSn3R/DIFFIO_RX_R21n
FM_A3	AB24		AC29	FM_D5	
FM_A4	AB23	DQ1R/DIFFIO_RX_R4p	AB25	FM_D6	DIFFIO_TX_R7n
FM_A5	AC28	DQ1R/DIFFIO_RX_R4n	AA25	FM_D7	DIFFIO_RX_R9p
FM_A6	Y24	DQ1R/DIFFIO_TX_R7p	AG28	FM_D8	DIFFIO_RX_R9n
FM_A7	Y25	DQ1R/DIFFIO_RX_R8p	AH29	FM_D9	DIFFIO_TX_R14p
		DQ1R/DIFFIO_RX_R8n	AA27	FM_D10	DIFFIO_TX_R16n
			AA28	FM_D11	DIFFIO_RX_R17p
			AL32	FM_D12	DIFFIO_RX_R17n
			AK33	FM_A1	DIFFIO_TX_R22p
					DIFFIO_TX_R24n

Bank 5B

VCCIO = 1.5V

DDR3B_DM0	AE30	DQ4R/DIFFIO_TX_R26p	AG34	DDR3B_DQ18	DQ6R/DIFFIO_TX_R42p
DDR3B_DQ1	AD30	DQ4R/DIFFIO_TX_R26n	AH34	DDR3B_DQ22	DQ6R/DIFFIO_TX_R42n
DDR3B_DQ5	Y28	DQ4R/DIFFIO_RX_R27p	AC33	DDR3B_DQ17	DQ6R/DIFFIO_RX_R43p
DDR3B_DQ7	Y27	DQ4R/DIFFIO_RX_R27n	AC34	DDR3B_DM2	DQ6R/DIFFIO_RX_R43n
DDR3B_DQ4	AH32	DQ4R/DIFFIO_TX_R28p			DQ6R pins at Clock section
DDR3B_DQ2	AJ32	DQ4R/DIFFIO_TX_R28n	AD34	DDR3B_DQ16	
DDR3B_DQ0	AF31	DQ4R/DIFFIO_TX_R30n	W32	DDR3B_DQ23	DQ6R/DIFFIO_TX_R46n
DDR3B_DQ3	AC31	DQ4R/DIFFIO_RX_R31p	V32	DDR3B_DQ21	DQ6R/DIFFIO_RX_R47p
MAX_OEn	AC32	DQ4R/DIFFIO_RX_R31n	AB33	DDR3B_DQ19	DQ6R/DIFFIO_RX_R47n
DDR3B_DQ6	AN34	DQ4R/DIFFIO_TX_R32p			DQ6R/DIFFIO_TX_R48p
DDR3B_DQS_P0	Y29		V24	DDR3B_DQS_P2	
DDR3B_DQS_N0	Y30	DQS4R/DIFFIO_RX_R29p	V23	DDR3B_DQS_N2	DQS6R/DIFFIO_RX_R45p
		DQSn4R/DIFFIO_RX_R29n			DQSn6R/DIFFIO_RX_R45n
DDR3B_DQ12	AA31		AA32	DDR3B_ODT	
DDR3B_DQ10	AB31	DQ5R/DIFFIO_TX_R34p	Y32	DDR3B_RASn	DIFFIO_RX_R25p
DDR3B_DQ13	AK34	DQ5R/DIFFIO_TX_R34n	AG31	DDR3B_RESETn	DIFFIO_RX_R25n
DDR3B_DQ11	AJ34	DQ5R/DIFFIO_RX_R35p	AM34	DDR3B_WEn	DIFFIO_TX_R30p
DDR3B_DQ9	AH33	DQ5R/DIFFIO_RX_R35n	AD31	MAX_WEn	DIFFIO_TX_R32n
DDR3B_DQ15	AG33	DQ5R/DIFFIO_TX_R36p	AF32	DDR3B_CKE	DIFFIO_TX_R38p
DDR3B_DQ8	AD32	DQ5R/DIFFIO_TX_R36n	AE34	DDR3B_A8	DIFFIO_TX_R40n
DDR3B_DQ14	W31	DQ5R/DIFFIO_TX_R38n	AB34	FLASH_ADVn	DIFFIO_TX_R46p
	V31	DQ5R/DIFFIO_RX_R39p			DIFFIO_TX_R48n
DDR3B_DM1	AE32	DQ5R/DIFFIO_RX_R39n			
		DQ5R/DIFFIO_TX_R40p			
DDR3B_DQS_P1	W29				
DDR3B_DQS_N1	W30	DQS5R/DIFFIO_RX_R37p			
		DQSn5R/DIFFIO_RX_R37n			

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Version = 0.2 Preliminary

VCCIO = 1.5V

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Cyclone V GT Bank 6

Bank 6A

DDR3B_DQ29	Y33	DQ7R/DIFFIO_TX_R50p	M31	DDR3B_DQ54	DQ10R/DIFFIO_TX_R74p
DDR3B_DQ27	AA33	DQ7R/DIFFIO_TX_R50n	L31	DDR3B_DM6	DQ10R/DIFFIO_TX_R74n
DDR3B_DQ31	U28	DQ7R/DIFFIO_RX_R51p	L30	DDR3B_DQ49	DQ10R/DIFFIO_RX_R75p
DDR3B_DQ24	U29	DQ7R/DIFFIO_RX_R51n	K30	DDR3B_DQ51	DQ10R/DIFFIO_RX_R75n
DDR3B_DQ25	V34	DQ7R/DIFFIO_TX_R54n	J32	DDR3B_DQ52	DQ10R/DIFFIO_TX_R76p
DDR3B_DQ28	R34	DQ7R/DIFFIO_RX_R55p	H32	DDR3B_DQ53	DQ10R/DIFFIO_TX_R76n
DDR3B_DQ30	P34	DQ7R/DIFFIO_RX_R55n	H31	DDR3B_DQ55	DQ10R/DIFFIO_RX_R78n
DDR3B_DQ26	U34	DQ7R/DIFFIO_TX_R56p	N28	DDR3B_DQ48	DQ10R/DIFFIO_RX_R79p
		DQ7R pins at Clock section	M28	MAX_CSn	DQ10R/DIFFIO_RX_R79n
			P30	DDR3B_DQ50	DQ10R/DIFFIO_TX_R80p
DDR3B_DQS_P3	U24	DQS7R/DIFFIO_RX_R53p	R23	DDR3B_DQS_P6	DQS10R/DIFFIO_RX_R77p
DDR3B_DQS_N3	U25	DQSn7R/DIFFIO_RX_R53n	R24	DDR3B_DQS_N6	DQSn10R/DIFFIO_RX_R77n
DDR3B_DQ34	T33	DQ8R/DIFFIO_TX_R58p	G31	DDR3B_DQ58	DQ11R/DIFFIO_TX_R82p
DDR3B_DQ32	T32	DQ8R/DIFFIO_TX_R58n	G30	DDR3B_DQ56	DQ11R/DIFFIO_TX_R82n
DDR3B_DQ38	T27	DQ8R/DIFFIO_RX_R59p	M29	DDR3B_DQ61	DQ11R/DIFFIO_RX_R83p
DDR3B_DQ36	T28	DQ8R/DIFFIO_RX_R59n	M30	DDR3B_DQ59	DQ11R/DIFFIO_RX_R83n
DDR3B_DQ39	M34	DQ8R/DIFFIO_TX_R60p	J30	DDR3B_DQ60	DQ11R/DIFFIO_TX_R84p
DDR3B_DM4	M33	DQ8R/DIFFIO_TX_R60n	J29	DDR3B_DQ62	DQ11R/DIFFIO_TX_R84n
DDR3B_DQ37	J34	DQ8R/DIFFIO_TX_R62n	H28	DDR3B_DM7	DQ11R/DIFFIO_TX_R86n
DDR3B_DQ33	N33	DQ8R/DIFFIO_TX_R63p	L28	DDR3B_DQ63	DQ11R/DIFFIO_TX_R87p
SDI_CLK148_UP	N34	DQ8R/DIFFIO_RX_R63n	L27	DDR3B_A9	DQ11R/DIFFIO_RX_R87n
DDR3B_DQ35	L33	DQ8R/DIFFIO_TX_R64p	K29	DDR3B_DQ57	DQ11R/DIFFIO_TX_R88p
DDR3B_DQS_P4	U23	DQS8R/DIFFIO_RX_R61p	P24	DDR3B_DQS_P7	DQS11R/DIFFIO_RX_R85p
DDR3B_DQS_N4	T23	DQSn8R/DIFFIO_RX_R61n	P25	DDR3B_DQS_N7	DQSn11R/DIFFIO_RX_R85n
DDR3B_DQ40	K33		V33	DDR3B_A10	
DDR3B_DM5	K32	DQ9R/DIFFIO_TX_R66p	U33	DDR3B_A11	DIFFIO_TX_R54p
DDR3B_DQ47	R27	DQ9R/DIFFIO_TX_R66n	K34	DDR3B_A2	DIFFIO_TX_R56n
DDR3B_DQ43	R28	DQ9R/DIFFIO_RX_R67p	L32	DDR3B_A3	DIFFIO_TX_R62p
DDR3B_DQ46	H34	DQ9R/DIFFIO_RX_R67n	R32	DDR3B_A4	DIFFIO_TX_R64n
DDR3B_DQ44	H33	DQ9R/DIFFIO_TX_R68p	R33	DDR3B_A5	DIFFIO_RX_R65p
DDR3B_DQ41	N31	DQ9R/DIFFIO_TX_R68n	N32	DDR3B_A6	DIFFIO_RX_R65n
DDR3B_DQ45	P32	DQ9R/DIFFIO_TX_R70n	G33	DDR3B_A7	DIFFIO_TX_R70p
SDI_CLK148_DN	P31	DQ9R/DIFFIO_RX_R71p	R30	DDR3B_CLK_P	DIFFIO_TX_R72n
DDR3B_DQ42	G34	DQ9R/DIFFIO_RX_R71n	R29	DDR3B_CLK_N	DIFFIO_RX_R73p
		DQ9R/DIFFIO_TX_R72p	J31	DDR3B_BA0	DIFFIO_RX_R73n
DDR3B_DQS_P5	T25		N29	DDR3B_BA1	DIFFIO_TX_R78p
DDR3B_DQS_N5	R25	DQS9R/DIFFIO_RX_R69p	P27	DDR3B_BA2	DIFFIO_TX_R80n
		DQSn9R/DIFFIO_RX_R69n	N27	DDR3B_CASn	DIFFIO_RX_R81p
			H29	DDR3B_A0	DIFFIO_RX_R81n
			K28	DDR3B_A1	DIFFIO_TX_R86p
					DIFFIO_TX_R88n

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DDR3B x64 SMC INTERFACE

DDR3B_DQ[63:0] — 9,13
DDR3B_A[13:0] — 9,13
DDR3B_DQS_P[7:0] — 13
DDR3B_DQS_N[7:0] — 13
DDR3B_DM[7:0] — 9,13
DDR3B_BA[2:0] — 13
DDR3B_CSn — 9,13
DDR3B_CASn — 13
DDR3B_CKE — 13
DDR3B_WEn — 13
DDR3B_RASn — 13
DDR3B_RESETn — 13
DDR3B_ODT — 13
DDR3B_CLK_P — 13
DDR3B_CLK_N — 13

FLASH INTERFACE

FM_D[15:0] — 10,14,15
FM_A[26:1] — 10,14,15
FLASH_ADVn — 14,15

MAX V CONTROL

MAX_OEn — 15
MAX_CSn — 15
MAX_WEn — 15

SDI_CLK148_UP — 8
SDI_CLK148_DN — 8

Title: Cyclone V GT FPGA Development Kit Board

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Cyclone V GT Banks 7 and 8

VCCIO = Varies (Default = 2.5V)

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Cyclone V GT Bank 7

Bank 7A

HSMB_A13	B19	HMC_T_DQ_0/DQ6T/DIFFIO_RX_T47n			
HSMB_A14	B20	HMC_T_DQ_1/DQ6T/DIFFIO_RX_T47p			
HSMB_A15	A21	HMC_T_DQ_2/DQ6T/DIFFIO_TX_T48p			
HSMB_A8	D19	HMC_T_DQ_3/DQ6T/DIFFIO_TX_T46n			
HSMB_A9	B21	HMC_T_DQ_4/DQ6T/DIFFIO_RX_T43n			
HSMB_CASn	C21	HMC_T_DQ_5/DQ6T/DIFFIO_RX_T43p			
HSMB_RASn	A23	HMC_T_DQ_6/DQ6T/DIFFIO_TX_T44p			
HSMB_WEn	B24	HMC_T_DQ_7/DQ6T/DIFFIO_TX_T42n			
HSMB_CLK_IN0	A22	HMC_T_ODT_1/DQ6T/DIFFIO_TX_T44n			
HSMB_A11	B23	HMC_T_DM_0/DQ6T/DIFFIO_TX_T42p			
HSMB_C_P	M18	HMC_T_DQS_0/DQS6T/DIFFIO_RX_T45p			
HSMB_ADDR_CMD0	L18	HMC_T_DQSn_0/DQSn6T/DIFFIO_RX_T45n			
HSMB_BA2	D20	HMC_T_DQ_8/DQ5T/DIFFIO_RX_T39n			
HSMB_A10	E20	HMC_T_DQ_9/DQ5T/DIFFIO_RX_T39p			
HSMB_A3	A26	HMC_T_DQ_10/DQ5T/DIFFIO_TX_T40p			
HSMB_A4	D21	HMC_T_DQ_11/DQ5T/DIFFIO_TX_T38n			
HSMB_A5	C23	HMC_T_DQ_12/DQ5T/DIFFIO_RX_T35n			
HSMB_A7	D22	HMC_T_DQ_13/DQ5T/DIFFIO_RX_T35p			
HSMB_BA0	B26	HMC_T_DQ_14/DQ5T/DIFFIO_TX_T36p			
HSMB_BA1	A27	HMC_T_DQ_15/DQ5T/DIFFIO_TX_T34n			
HSMB_A1	B25	HMC_T_CKE_0/DQ5T/DIFFIO_TX_T36n			
HSMB_A2	A28	HMC_T_DM_1/DQ5T/DIFFIO_TX_T34p			
HSMB_PRSNTn	M20	HMC_T_DQS_1/DQS5T/DIFFIO_RX_T37p			
HSMB_BA3	M19	HMC_T_DQSn_1/DQSn5T/DIFFIO_RX_T37n			
HSMB_DQ1	G20				
HSMB_DQ2	F20	HMC_T_DQ_16/DQ4T/DIFFIO_RX_T31n			
HSMB_DQ3	D24	HMC_T_DQ_17/DQ4T/DIFFIO_RX_T31p			
HSMB_DQ4	C26	HMC_T_DQ_18/DQ4T/DIFFIO_TX_T32p			
HSMB_DQ5	G21	HMC_T_DQ_19/DQ4T/DIFFIO_TX_T30n			
HSMB_DQ6	F21	HMC_T_DQ_20/DQ4T/DIFFIO_RX_T27n			
HSMB_DQ7	D27	HMC_T_DQ_21/DQ4T/DIFFIO_RX_T27p			
HSMB_A0	E23	HMC_T_DQ_22/DQ4T/DIFFIO_TX_T28n			
HSMB_DQ0	E22	HMC_T_DQ_23/DQ4T/DIFFIO_TX_T26n			
HSMB_DQS_P0	N22	HMC_T_DM_2/DQ4T/DIFFIO_TX_T26p			
HSMB_DQS_N0	M21	HMC_T_DQS_2/DQS4T/DIFFIO_RX_T29p			
		HMC_T_DQSn_2/DQSn4T/DIFFIO_RX_T29n			
HSMB_DQ11	H21	HMC_T_DQ_24/DQ3T/DIFFIO_RX_T23n			
HSMB_DQ12	H22	HMC_T_DQ_25/DQ3T/DIFFIO_RX_T23p			
HSMB_DQ13	B28	HMC_T_DQ_26/DQ3T/DIFFIO_TX_T24p			
HSMB_DQ14	D26	HMC_T_DQ_27/DQ3T/DIFFIO_TX_T22n			
HSMB_DQ15	F22	HMC_T_DQ_28/DQ3T/DIFFIO_RX_T19n			
HSMB_DQ8	F23	HMC_T_DQ_29/DQ3T/DIFFIO_RX_T19p			
HSMB_DQ9	C29	HMC_T_DQ_30/DQ3T/DIFFIO_TX_T20p			
	E25	HMC_T_DQ_31/DQ3T/DIFFIO_TX_T18n			
HSMB_DQ10	E24	HMC_T_DM_3/DQ3T/DIFFIO_TX_T18p			
HSMB_DQS_P1	M23	HMC_T_DQS_3/DQS3T/DIFFIO_RX_T21p			
HSMB_DQS_N1	N23	HMC_T_DQSn_3/DQSn3T/DIFFIO_RX_T21n			

		RZQ_2/DIFFIO_TX_T48n	A20	RZQIN_HSMB_VAR	
		HMC_T_DQ_32/DQ2T/DIFFIO_RX_T15n	G23	HSMB_DQ17	
		HMC_T_DQ_33/DQ2T/DIFFIO_RX_T15p	H23	HSMB_DQ18	
		HMC_T_DQ_34/DQ2T/DIFFIO_TX_T16p	B31	HSMB_DQ19	
		HMC_T_DQ_35/DQ2T/DIFFIO_TX_T14n	E28	HSMB_DQ20	
		HMC_T_DQ_36/DQ2T/DIFFIO_RX_T11n	D29	HSMB_DQ21	
		HMC_T_DQ_37/DQ2T/DIFFIO_RX_T11p	D30	HSMB_DQ22	
		HMC_T_DQ_38/DQ2T/DIFFIO_TX_T12p	C32	HSMB_DQ23	
		HMC_T_DQ_39/DQ2T/DIFFIO_TX_T10n	F28		
		HMC_T_DM_4/DQ2T/DIFFIO_TX_T10p	F27	HSMB_DQ16	
		HMC_T_DQS_4/DQS2T/DIFFIO_RX_T13p	L23	HSMB_DQS_P2	
		HMC_T_DQSn_4/DQSn2T/DIFFIO_RX_T13n	K23	HSMB_DQS_N2	
			E19	HSMB_C_N	
		HMC_T_ODT_0/DIFFIO_TX_T46p	C22	HSMB_CKE	
		HMC_T_CKE_1/DIFFIO_TX_T38p	D25	HSMB_CLK_OUT0	
		HMC_T_RESETn/DIFFIO_TX_T30p			
			K25	HSMB_CLK_IN_P1	
		DIFFIO_RX_T1p	J25	HSMB_CLK_IN_N1	
		DIFFIO_RX_T1n	F26	HSMB_CLK_OUT_P2	
		DIFFIO_TX_T6p	E30		
		DIFFIO_TX_T8n			
		DQ1T/DIFFIO_TX_T2p	H27	HSMB_DM3	
		DQ1T/DIFFIO_TX_T2n	H26	HSMB_DQ24	
		DQ1T/DIFFIO_RX_T3p	G25	HSMB_DQ25	
		DQ1T/DIFFIO_RX_T3n	F25	HSMB_DQ27	
		DQ1T/DIFFIO_TX_T4p	G28	HSMB_DQ26	
		DQ1T/DIFFIO_TX_T4n	G29	HSMB_DQ28	
		DQ1T/DIFFIO_TX_T6n	G26	HSMB_CLK_OUT_N2	
		DQ1T/DIFFIO_RX_T7p	G24	HSMB_DQ30	
		DQ1T/DIFFIO_RX_T7n	H24	HSMB_DQ29	
		DQ1T/DIFFIO_TX_T8p	F30	HSMB_DQ31	
		DQS1T/DIFFIO_RX_T5p	M24	HSMB_DQS_P3	
		DQSn1T/DIFFIO_RX_T5n	N24	HSMB_DQS_N3	
		HMC_GND/DIFFIO_RX_T9p	M25	HSMB_CSn	
		HMC_GND/DIFFIO_RX_T9n	L25	HSMB_A12	
		HMC_GND/DIFFIO_TX_T14p	E29	HSMB_A6	
		HMC_GND/DIFFIO_TX_T16n	B30	HSMB_RX_LED	
		HMC_GND/DIFFIO_RX_T17p	L22	HSMB_CLK_OUT_P1	
		HMC_GND/DIFFIO_RX_T17n	K22	HSMB_CLK_OUT_N1	
		HMC_GND/DIFFIO_TX_T22p	E27	HSMB_SCL	
		HMC_GND/DIFFIO_TX_T24n	B29		
		HMC_GND/DIFFIO_RX_T25p	L21		
		HMC_GND/DIFFIO_RX_T25n	L20	HSMB_SDA	
		HMC_GND/DIFFIO_TX_T32n	C24	HSMB_TX_LED	
		HMC_GND/DIFFIO_TX_T40n	A25		
		HMC_GND/DQ2T/DIFFIO_TX_T12n	C31	HSMB_DM2	
		HMC_GND/DQ3T/DIFFIO_TX_T20n	C28	HSMB_DM1	
		HMC_GND/DQ4T/DIFFIO_TX_T28n	C27	HSMB_DM0	

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HSMA_TX_D_P6	A7	DQ9T/DIFFIO_TX_T66p		DQ11T/DIFFIO_TX_T82p	D11	HSMA_TX_D_P8
HSMA_TX_D_N6	A6	DQ9T/DIFFIO_TX_T66n		DQ11T/DIFFIO_TX_T82n	D10	HSMA_TX_D_N8
HSMA_RX_D_P5	B8	DQ9T/DIFFIO_RX_T67p		DQ11T/DIFFIO_TX_T83p	G13	HSMA_RX_D_P11
HSMA_RX_D_N5	A8	DQ9T/DIFFIO_RX_T67n		DQ11T/DIFFIO_TX_T83n	H13	HSMA_RX_D_N11
HSMA_TX_D_P11	C11	DQ9T/DIFFIO_TX_T68p		DQ11T/DIFFIO_TX_T84p	C8	HSMA_TX_D_P7
HSMA_TX_D_N11	B11	DQ9T/DIFFIO_TX_T68n		DQ11T/DIFFIO_TX_T84n	C7	HSMA_TX_D_N7
HSMA_TX_D_N1	B9	DQ9T/DIFFIO_TX_T70n		DQ11T/DIFFIO_TX_T86n	B3	HSMA_TX_LED
HSMA_RX_D_P8	E15	DQ9T/DIFFIO_RX_T71p		DQ11T/DIFFIO_RX_T87p	E12	HSMA_SCL
HSMA_RX_D_N8	D15	DQ9T/DIFFIO_RX_T71n		DQ11T/DIFFIO_RX_T87n	D12	HSMA_RX_LED
HSMA_TX_D_P5	C13	DQ9T/DIFFIO_TX_T72p		DQ11T/DIFFIO_TX_T88p	C1	HSMA_CLK_OUT_P1
HSMA_RX_D_P15	L16	DQS9T/DIFFIO_RX_T69p		DQS11T/DIFFIO_RX_T85p	N13	HSMA_RX_D_P3
HSMA_RX_D_N15	L15	DQSn9T/DIFFIO_RX_T69n		DQSn11T/DIFFIO_RX_T85n	N12	HSMA_RX_D_N3
HSMA_TX_D_P2	B5	DQ10T/DIFFIO_TX_T74p		DQ12T/DIFFIO_TX_T90p	F10	HSMA_CLK_OUT0
HSMA_TX_D_N2	A5	DQ10T/DIFFIO_TX_T74n		DQ12T/DIFFIO_TX_T90n	E10	USER_DIPSW2
HSMA_RX_D_P12	E14	DQ10T/DIFFIO_RX_T75p		DQ12T/DIFFIO_TX_T91p	F12	HSMA_D2
HSMA_RX_D_N12	D14	DQ10T/DIFFIO_RX_T75n		DQ12T/DIFFIO_TX_T91n	F11	HSMA_D1
HSMA_TX_D_P4	C6	DQ10T/DIFFIO_TX_T76p		DQ12T/DIFFIO_TX_T92p	E9	USER_DIPSW4
HSMA_TX_D_N4	B6	DQ10T/DIFFIO_TX_T76n		DQ12T/DIFFIO_TX_T92n	D9	USER_DIPSW3
HSMA_TX_D_N13	E13	DQ10T/DIFFIO_TX_T78n		DQ12T/DIFFIO_TX_T94n	D7	USER_DIPSW5
HSMA_RX_D_P7	H14	DQ10T/DIFFIO_RX_T79p		DQ12T/DIFFIO_TX_T95p	H12	USER_DIPSW0
HSMA_RX_D_N7	G14	DQ10T/DIFFIO_RX_T79n		DQ12T/DIFFIO_TX_T95n	G11	HSMA_CLK_IN0
HSMA_TX_D_P0	B4	DQ10T/DIFFIO_TX_T80p		DQ12T/DIFFIO_TX_T96p	F8	
HSMA_RX_D_P0	P14	DQS10T/DIFFIO_RX_T77p		DQS12T/DIFFIO_RX_T93p	L11	HSMA_PRSNTn
HSMA_RX_D_N0	N14	DQSn10T/DIFFIO_RX_T77n		DQSn12T/DIFFIO_RX_T93n	K12	HSMA_D3

HMC

HMC_T_BA_0/DQ7T/DIFFIO_TX_T56p		HMC_T_A_8/DQ8T/DIFFIO_RX_T59p	F17	HSMA_RX_D_P16	
HMC_T_BA_1/DQ7T/DIFFIO_RX_T55p		HMC_T_A_9/DQ8T/DIFFIO_RX_T59n	F16	HSMA_RX_D_N16	
HMC_T_BA_2/DQ7T/DIFFIO_RX_T55n		HMC_T_A_10/DQ8T/DIFFIO_TX_T60p	B13	HSMA_TX_D_P10	
HMC_T_A_0/DQ7T/DIFFIO_TX_T50p		HMC_T_A_11/DQ8T/DIFFIO_TX_T60n	A13	HSMA_TX_D_N10	
HMC_T_A_1/DQ7T/DIFFIO_TX_T50n		HMC_T_A_12/DQ8T/DIFFIO_TX_T62p	C14	HSMA_TX_D_P12	
HMC_T_A_2, 3 at Clock section		HMC_T_A_13/DQ8T/DIFFIO_TX_T62n	B14	HSMA_TX_D_N12	
HMC_T_A_4/DQ7T/DIFFIO_RX_T51p		HMC_T_A_14/DQ8T/DIFFIO_RX_T63p	D17	HSMA_RX_D_P14	
HMC_T_A_5/DQ7T/DIFFIO_RX_T51n		HMC_T_A_15/DQ8T/DIFFIO_RX_T63n	D16	HSMA_RX_D_N14	
HMC_T_A_6/DIFFIO_TX_T54p		HMC_T_CASn/DQ8T/DIFFIO_TX_T58p	A12	HSMA_TX_D_P3	
HMC_T_A_7/DQ7T/DIFFIO_TX_T54n		HMC_T_RASn/DQ8T/DIFFIO_TX_T58n	A11	HSMA_TX_D_N3	
		HMC_T_WEn/DQ8T/DIFFIO_TX_T64p	B10	HSMA_TX_D_P9	
HMC_T_CK/DQS7T/DIFFIO_RX_T53p		HMC_T_CSn_0/DQS8T/DIFFIO_RX_T61p	M15	HSMA_RX_D_P1	
HMC_T_CKn/DQSn7T/DIFFIO_RX_T53n		HMC_T_CSn_1/DQSn8T/DIFFIO_RX_T61n	M14	HSMA_RX_D_N1	
		HMC_GND/DIFFIO_TX_T56n	A15	HSMA_TX_D_N15	
		HMC_GND/DIFFIO_TX_T64n	A10	HSMA_TX_D_N9	
DIFFIO_RX_T65p					
DIFFIO_RX_T65n					
DIFFIO_TX_T70p					
DIFFIO_RX_T73p					
DIFFIO_RX_T73n		DIFFIO_TX_T72n	C12	HSMA_TX_D_N5	
DIFFIO_RX_T81p		DIFFIO_TX_T78p	F13	HSMA_TX_D_P13	
DIFFIO_RX_T81n		DIFFIO_TX_T80n	A3	HSMA_TX_D_N0	
DIFFIO_TX_T88n		DIFFIO_TX_T86p	A2	USER_DIPSW1	
DIFFIO_RX_T89p		DIFFIO_TX_T94p	E7	USER_DIPSW7	
DIFFIO_RX_T89n		DIFFIO_TX_T96n	E8	USER_DIPSW6	

HSMA_RX_D_P10	E18				
HSMA_RX_D_N10	E17				
HSMA_TX_D_P14	A17				
HSMA_TX_D_N14	A16				
HSMA_RX_D_P4	M16				
HSMA_RX_D_N4	L17				
HSMA_RX_D_P9	F15				
HSMA_RX_D_N9	G15				
HSMA_TX_D_P1	C9				
HSMA_RX_D_P6	J15				
HSMA_RX_D_N6	K14				
HSMA_RX_D_P2	M13				
HSMA_RX_D_N2	L13				
HSMA_CLK_OUT_N1	B1				
HSMA_D0	L12				
HSMA_SDA	K13				

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Version = 0.2 Preliminary

HSMC PORT A INTERFACE

HSMA_D[3:0]	18
HSMA_CLK_OUT_P[2:1]	9,18
HSMA_CLK_OUT_N[2:1]	9,18
HSMA_TX_D_P[16:0]	18
HSMA_TX_D_N[16:0]	18
HSMA_RX_D_P[16:0]	18
HSMA_RX_D_N[16:0]	18
HSMA_SDA	18
HSMA_SCL	18
HSMA_CLK_OUT0	18
HSMA_TX_LED	20
HSMA_RX_LED	20
HSMA_PRSNTn	6,15,18,20
HSMA_CLK_IN0	18
HSMA_PRSNTn	6,15,18,20

HSMC PORT B INTERFACE

HSMB_A[15:0]	18
HSMB_BA[3:0]	18
HSMB_DM[3:0]	18
HSMB_DQ[31:0]	18
HSMB_DQS_P[3:0]	18
HSMB_DQS_N[3:0]	18
HSMB_CLK_IN_P[2:1]	9,18
HSMB_CLK_IN_N[2:1]	9,18
HSMB_CLK_OUT_P[2:1]	18
HSMB_CLK_OUT_N[2:1]	18
HSMB_WEn	18
HSMB_CSn	18
HSMB_CKE	18
HSMB_CASn	18
HSMB_RASn	18
HSMB_CLK_IN0	18
HSMB_CLK_OUT0	18
HSMB_C_P	18
HSMB_C_N	18
HSMB_ADDR_CMD0	18
HSMB_SCL	18
HSMB_SDA	18
HSMB_RX_LED	20
HSMB_TX_LED	20
HSMB_PRSNTn	15,18,20

USER I/O INTERFACES

USER_DIPSW[7:0]	20

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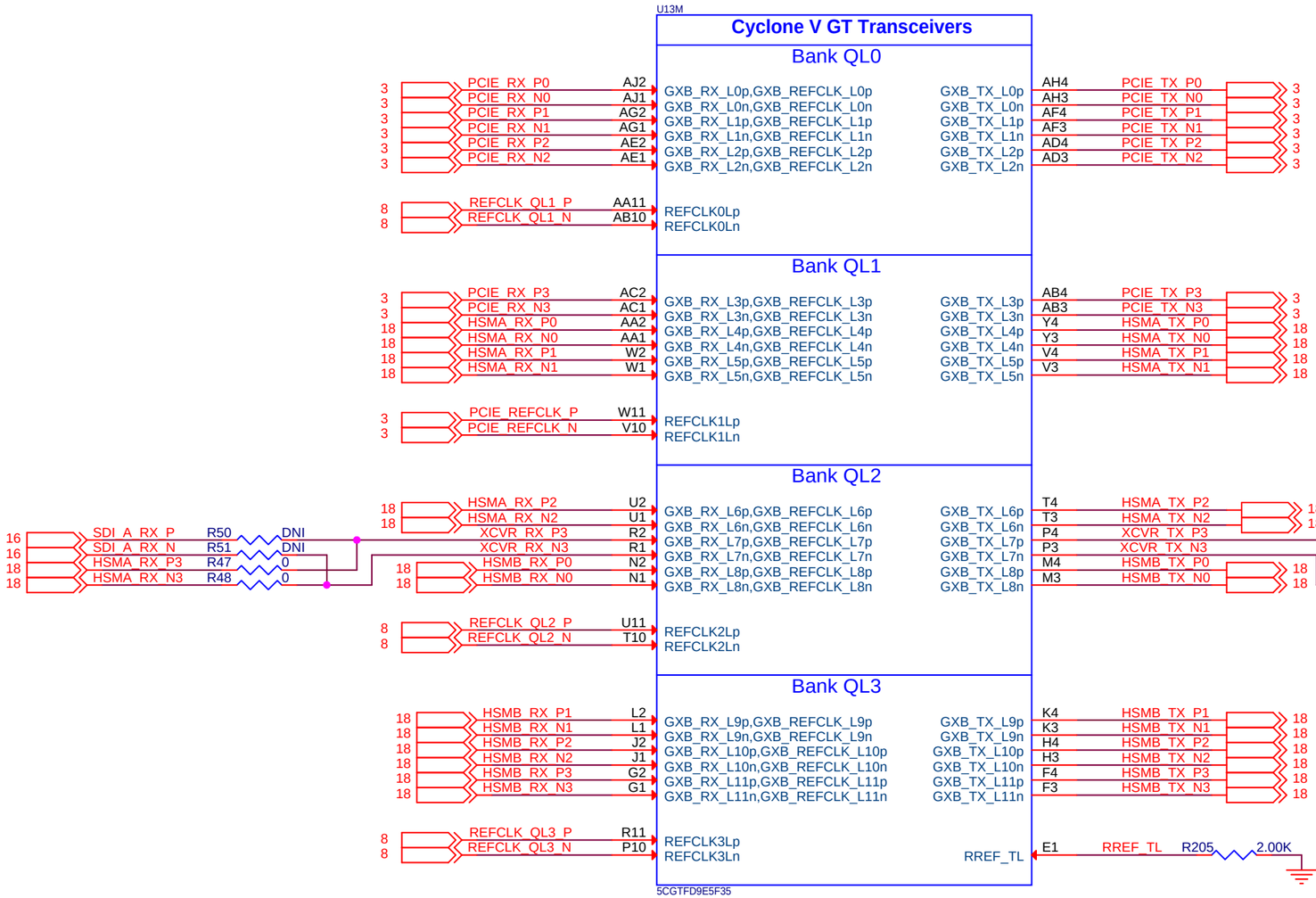
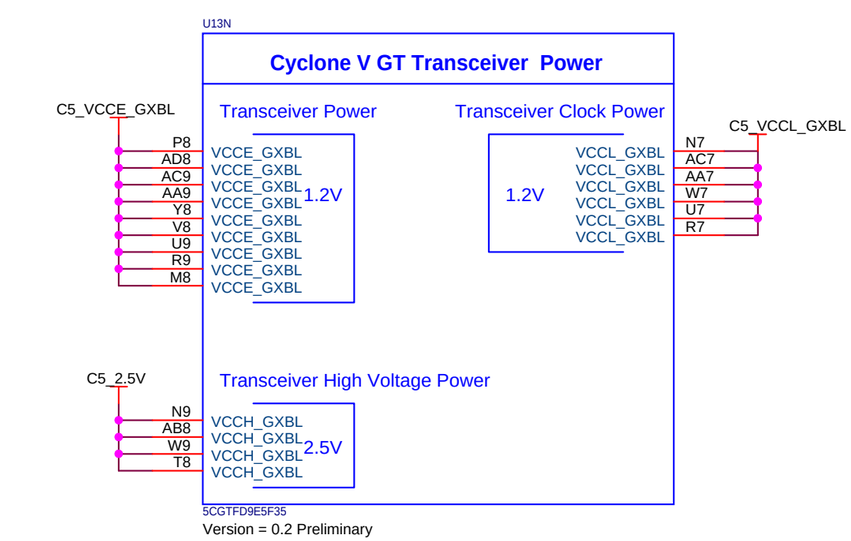
Cyclone V GT Transceivers and Power





Title	Cyclone V GT FPGA Development Kit Board	
Size B	Document Number 150-0321004-B1 (6XX-44179R)	Rev B
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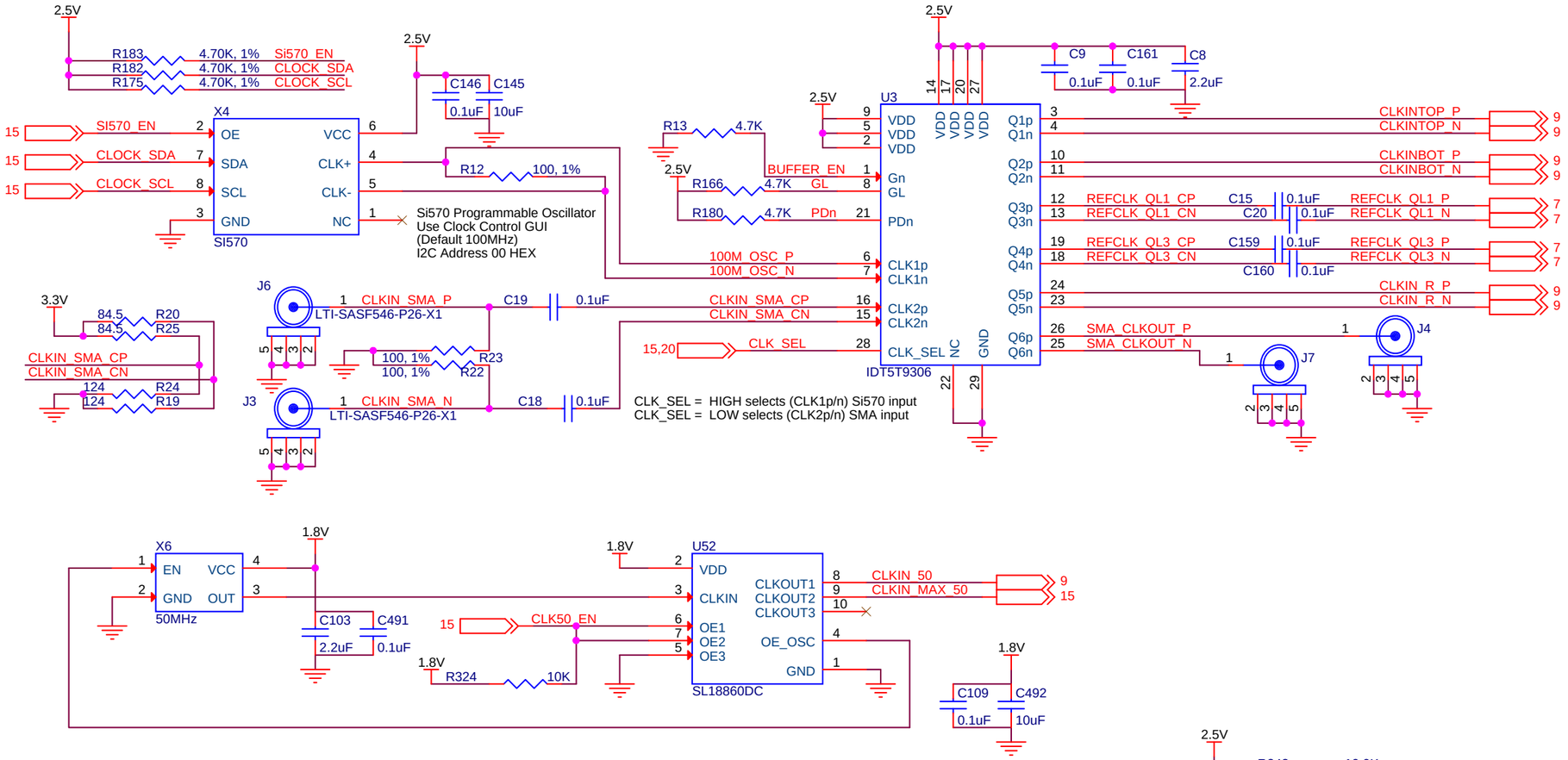
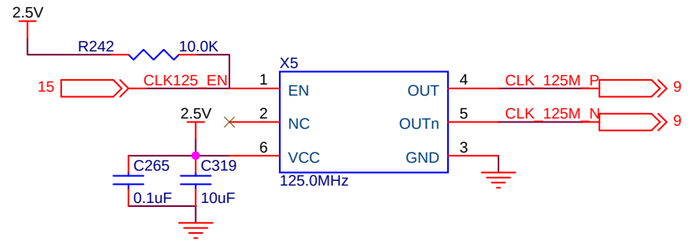
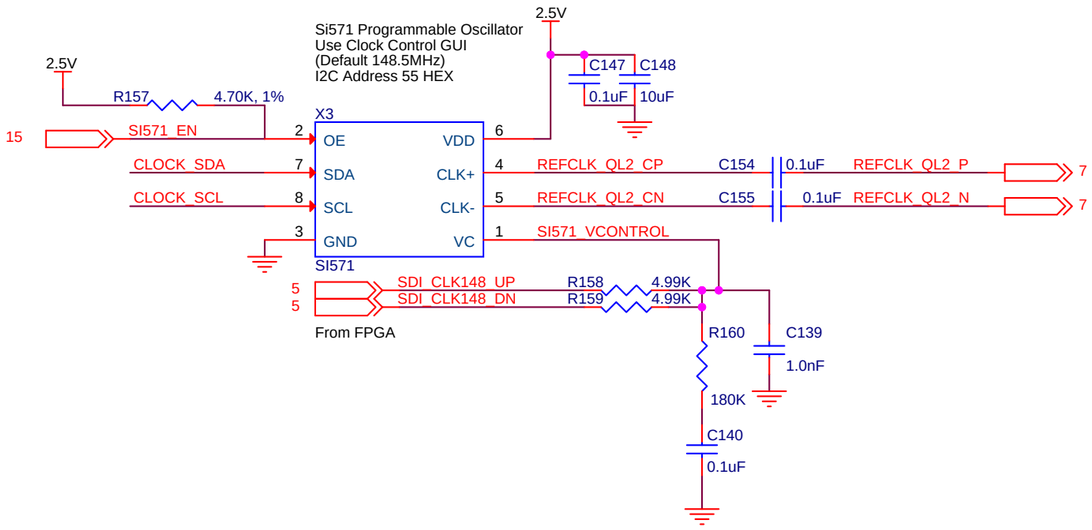
Clocks/Oscillators







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Cyclone V GT Clocks

CLKINBOT_P	R266	100, 1%	CLKINBOT_N
CLKIN_R_P	R251	100, 1%	CLKIN_R_N
CLKINTOP_P	R181	100, 1%	CLKINTOP_N
CLK_125M_P	R245	100, 1%	CLK_125M_N
HSMB_CLK_IN_P2	R223	100, 1%	HSMB_CLK_IN_N2
HSMA_CLK_IN_P1	R217	DNI	HSMA_CLK_IN_N1
HSMA_CLK_IN_P2	R218	DNI	HSMA_CLK_IN_N2

DOES NOT NEED TO BE A CLOCK OUT, CAN BE USED AS I/O.

SMA_CLKOUT — 1 — J14 (2, 3, 4, 5)

U13G

Cyclone V GT Clocks

Bank 3B *VCCIO = 1.5V*

	AD17	CLK0p/FPLL_BL_FBp/DIFFIO_RX_B39p	DQ6B/HMC_B_A_2/FPLL_BL_CLKOUT0/FPLL_BL_CLKOUTp/FPLL_BL_FB/DIFFIO_TX_B45p
USB_RESETn	AC17	CLK0n/FPLL_BL_FBn/DIFFIO_RX_B39n	DQ6B/HMC_B_A_3/FPLL_BL_CLKOUT1/FPLL_BL_CLKOUTn/DIFFIO_TX_B45n
USB_CLK	AC18	CLK1p/DIFFIO_RX_B47p	
USB_RDn	AB18	CLK1n/DIFFIO_RX_B47n	

AM18 DDR3A_A2
AN18 DDR3A_A3

Bank 4A *VCCIO = 1.5V*

CLKINBOT_P	AF18	CLK2p/DIFFIO_RX_B55p
CLKINBOT_N	AG18	CLK2n/DIFFIO_RX_B55n
FLASH_RDYBSYn	AD20	CLK3p/DIFFIO_RX_B63p
	AE20	CLK3n/DIFFIO_RX_B63n

Bank 5B *VCCIO = 1.5V*

CLKIN_50	V28	CLK6p/DIFFIO_RX_R41p	DQ6R/FPLL_BR_CLKOUT0/FPLL_BR_CLKOUTp/FPLL_BR_FB/DIFFIO_TX_R44p
DDR3B_CSn	V27	CLK6n/DIFFIO_RX_R41n	DQ6R/FPLL_BR_CLKOUT1/FPLL_BR_CLKOUTn/DIFFIO_TX_R44n
CLKIN_R_P	W26	CLK7p/FPLL_BR_FBp/DIFFIO_RX_R33p	
CLKIN_R_N	W27	CLK7n/FPLL_BR_FBn/DIFFIO_RX_R33n	

AF33 SMA_CLKOUT
AE33 DDR3B_DQ20

Bank 6A *VCCIO = 1.5V*

DDR3B_A12	T31	CLK4p/FPLL_TR_FBp/DIFFIO_RX_R57p	DQ7R/FPLL_TR_CLKOUT0/FPLL_TR_CLKOUTp/FPLL_TR_FB/DIFFIO_TX_R52p
DDR3B_A13	T30	CLK4n/FPLL_TR_FBn/DIFFIO_RX_R57n	DQ7R/FPLL_TR_CLKOUT1/FPLL_TR_CLKOUTn/DIFFIO_TX_R52n
CLK_125M_P	U31	CLK5p/DIFFIO_RX_R49p	
CLK_125M_N	U30	CLK5n/DIFFIO_RX_R49n	

Y34 MAX_CLK
W34 DDR3B_DM3

Bank 7A *VCCIO = VARIES*

CLKINTOP_P	H19	CLK10p/DIFFIO_RX_T41p
CLKINTOP_N	H18	CLK10n/DIFFIO_RX_T41n
HSMB_CLK_IN_P2	J20	CLK11p/DIFFIO_RX_T33p
HSMB_CLK_IN_N2	K19	CLK11n/DIFFIO_RX_T33n

Bank 8A *VCCIO = 2.5V*

HSMA_CLK_IN_P2	H17	CLK8p/FPLL_TL_FBp/DIFFIO_RX_T57p	DQ7T/HMC_T_A_2/FPLL_TL_CLKOUT0/FPLL_TL_CLKOUTp/FPLL_TL_FB/DIFFIO_TX_T52p
HSMA_CLK_IN_N2	H16	CLK8n/FPLL_TL_FBn/DIFFIO_RX_T57n	DQ7T/HMC_T_A_3/FPLL_TL_CLKOUT1/FPLL_TL_CLKOUTn/DIFFIO_TX_T52n
HSMA_CLK_IN_P1	G18	CLK9p/DIFFIO_RX_T49p	
HSMA_CLK_IN_N1	F18	CLK9n/DIFFIO_RX_T49n	

B18 HSMA_CLK_OUT_P2
A18 HSMA_CLK_OUT_N2

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Version = 0.2 Preliminary

CLOCKS

CLKIN_50 8
CLKINBOT_P 8
CLKINBOT_N 8
CLKIN_R_P 8
CLKIN_R_N 8
CLKINTOP_P 8
CLKINTOP_N 8
CLK_125M_P 8
CLK_125M_N 8

HSMC PORT A INTERFACE

HSMA_CLK_IN_P[2:1] 18
HSMA_CLK_IN_N[2:1] 18
HSMA_CLK_OUT_P[2:1] 6,18
HSMA_CLK_OUT_N[2:1] 6,18

HSMC PORT B INTERFACE

HSMB_CLK_IN_P[2:1] 6,18
HSMB_CLK_IN_N[2:1] 6,18

USB INTERFACE

USB_RESETn 19
USB_RDn 19
USB_CLK 15,19

DDR3A x40 HMC INTERFACE

DDR3A_A[13:0] 4,12

DDR3B X64 SMC INTERFACE

DDR3B_DQ[31:0] 5,13
DDR3B_A[13:0] 5,13
DDR3B_DM[7:0] 5,13
DDR3B_CSn 13

FLASH INTERFACE

FLASH_RDYBSYn 14,15

MAX_CLK 15

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Cyclone V GT Configuration

INSTALL THIS RESISTOR ONLY WHEN FPGA IS NOT POPULATED.

JTAG_FPGA_TDO — R258 DNI — JTAG_BLASTER_TDO

U13H

Cyclone V GT Configuration

Bank 3A

11,15,19	JTAG_TMS	AG11 — TMS
11,15,18,19	JTAG_TCK	AK5 — TCK
11,19	JTAG_BLASTER_TDO	AE10 — TDI
11,18	JTAG_FPGA_TDO	AF11 — TDO
		AF13 — CLKUSR/DQ1B/DIFFIO_RX_B5p
14,15	FPGA_DCLK	AF10 — DCLK
14,15	FPGA_CONFIG_D[15:0]	
	FPGA_CONFIG_D0	AH9 — AS_DATA0/ASDO
	FPGA_CONFIG_D1	AJ7 — AS_DATA1
	FPGA_CONFIG_D2	AH8 — AS_DATA2
	FPGA_CONFIG_D3	AJ6 — AS_DATA3
	FPGA_CONFIG_D4	AG10 — DATA4/nCSO
	FPGA_CONFIG_D5	AM4 — DATA5/DIFFIO_TX_B2n
	FPGA_CONFIG_D6	AD11 — DATA6/DQ1B/DIFFIO_RX_B1n
	FPGA_CONFIG_D7	AM5 — DATA7/DQ1B/DIFFIO_TX_B2p
	FPGA_CONFIG_D8	AD12 — DATA8/DQ1B/DIFFIO_RX_B1p
	FPGA_CONFIG_D9	AL7 — DATA9/DQ1B/DIFFIO_TX_B4n
	FPGA_CONFIG_D10	AJ11 — DATA10/DQSn1B/DIFFIO_RX_B3n
	FPGA_CONFIG_D11	AK7 — DATA11/DIFFIO_TX_B4p
	FPGA_CONFIG_D12	AH12 — DATA12/DQS1B/DIFFIO_RX_B3p
	FPGA_CONFIG_D13	AL8 — DATA13/DQ1B/DIFFIO_TX_B6n
	FPGA_CONFIG_D14	AG13 — DATA14/DQ1B/DIFFIO_RX_B5n
	FPGA_CONFIG_D15	AK8 — DATA15/DQ1B/DIFFIO_TX_B6p
		AJ9 — IO/DQ1B/DIFFIO_TX_B8p
	FLASH_CLK	AE29 — DEV_OE/DIFFIO_TX_R5p
15,20	CPU_RESETn	AD29 — DEV_CLRn/DQ1R/DIFFIO_TX_R5n
	FM_D14	AC23 — INIT_DONE/DIFFIO_RX_R2p
15	FPGA_nSTATUS	G9 — nSTATUS
15	FPGA_nCONFIG	G8 — nCONFIG
15	FPGA_CONF_DONE	G10 — CONF_DONE
	FPGA_CEn	F7 — nCE

Bank 5A

		PR_READY/DQ1B/DIFFIO_TX_B8n — AK9 — FPGA_PR_READY
		PR_ERROR/DIFFIO_RX_B7p — AC13 — FPGA_PR_ERROR
		PR_DONE/DIFFIO_RX_B7n — AC12 — FPGA_PR_DONE
		PR_REQUEST/DQ1R/DIFFIO_TX_R1n — AD25 — FPGA_PR_REQUEST
		CvP_CONFDONE/DQ1R/DIFFIO_TX_R3n — AC26 — FPGA_CvP_CONFDONE
		CRC_ERROR/DIFFIO_RX_R2n — AC24 — FM_D13
		nPERSTL0/DQS1R/DIFFIO_RX_R6p — AA21 — FLASH_CEn
		nPERSTL1/DQSn1R/DIFFIO_RX_R6n — AA22 — PCIE_PERSTn — 3
		nCEO/DQ1R/DIFFIO_TX_R3p — AC27 — FM_A2

Bank 9A

		MSEL0 — J12 — FPGA_MSEL0
		MSEL1 — J11 — FPGA_MSEL1
		MSEL2 — F6 — FPGA_MSEL2
		MSEL3 — K10 — FPGA_MSEL3
		MSEL4 — H7 — FPGA_MSEL4

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Version = 0.2 Preliminary

FPGA_DCLK — R97 DNI — C97 DNI; R98 DNI

2.5V — R355 10K; R332 10K; R331 10K

2.5V — R190 DNI; R189 1.00k

C5_VCCIO_2.5V — R269 10K; R256 10K; R254 10K; R255 10K

SW5 (DIP-8) TDA04H0SB1

1	8	FPGA_MSEL1	R119 1.00k
2	7	FPGA_MSEL2	R120 1.00k
3	6	FPGA_MSEL4	R121 1.00k
4	5	FORCE_FAN	R122 10K

2.5V — FPGA_MSEL0 — R186 DNI; R185 1.00k

2.5V — FPGA_MSEL3 — R188 DNI; R187 1.00k

FLASH INTERFACE

FM_D[15:0]	5,14,15
FM_A[26:1]	5,14,15
FLASH_CLK	14,15
FLASH_CEn	14,15
FPGA_CEn	15
FPGA_MSEL0	15
FPGA_MSEL1	15
FPGA_MSEL2	15
FPGA_MSEL3	15
FPGA_MSEL4	15
FORCE_FAN	15

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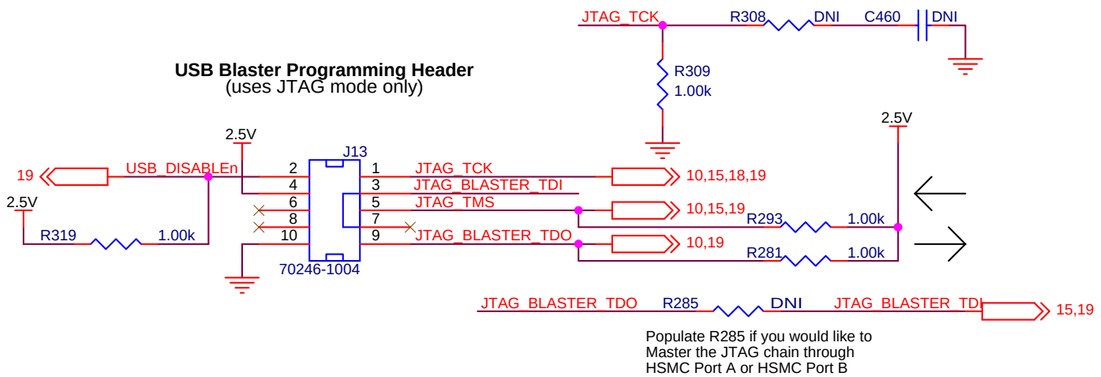
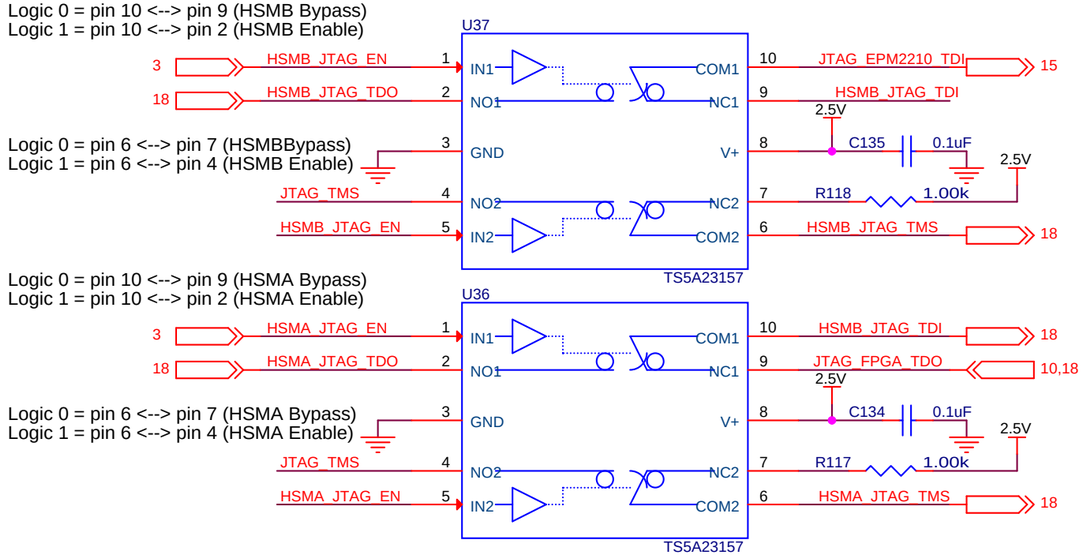
JTAG

USB Blaster Programming Header
(uses JTAG mode only)



Populate R285 if you would like to
Master the JTAG chain through
HSMC Port A or HSMC Port B

TS5A23157 Switch Functions
When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON



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DDR3A (x40 HMC)

Uses Hard Memory Controller

DDR3A_CLK_P 200 R317 DDR3A_CLK_N

DDR3A_CLK_P 200 R318 DDR3A_CLK_N

Place one termination resistor at the end of each branch.

VTT_DDR3A — CN5 (1 2 3 4 / 8 7 6 5) 0.1uF

VTT_DDR3A — CN4 (1 2 3 4 / 8 7 6 5) 0.1uF

VTT_DDR3A — CN6 (1 2 3 4 / 8 7 6 5) 0.1uF

DDR3A_RESETn R339 51 1.5V_DDR3

DDR3A_CKE R330 4.70K, 1%

VTT_DDR3A

DDR3A_A13	RN6A	1	16 51
DDR3A_BA2	RN6D	4	13 51
DDR3A_A8	RN6G	7	10 51
DDR3A_CSn	RN7B	2	15 51
DDR3A_A7	RN7E	5	12 51
DDR3A_A9	RN7H	8	9 51
DDR3A_A6	RN5C	3	14 51
DDR3A_BA1	RN5F	6	11 51

VTT_DDR3A

DDR3A_A2	RN6B	2	15 51
DDR3A_A11	RN6E	5	12 51
	RN6H	8	9 51
DDR3A_A3	RN7C	3	14 51
DDR3A_A5	RN7F	6	11 51
DDR3A_RASn	RN5A	1	16 51
DDR3A_A4	RN5D	4	13 51
	RN5G	7	10 51

VTT_DDR3A

DDR3A_WEn	RN6C	3	14 51
DDR3A_A1	RN6F	6	11 51
DDR3A_ODT	RN7A	1	16 51
DDR3A_BA0	RN7D	4	13 51
DDR3A_A0	RN7G	7	10 51
DDR3A_A12	RN5B	2	15 51
DDR3A_CASn	RN5E	5	12 51
DDR3A_A10	RN5H	8	9 51

4 DDR3A_DQS_P[4:0]

4 DDR3A_DQS_N[4:0]

4 DDR3A_DQ[39:0]

4,9 DDR3A_A[13:0]

4 DDR3A_BA[2:0]

4 DDR3A_DM[4:0]

U28 — DDR3 Device

DDR3A_A0	N3	A0	DQ0	E3	DDR3A_DQ32
DDR3A_A1	P7	A1	DQ1	F7	DDR3A_DQ33
DDR3A_A2	P3	A2	DQ2	F2	DDR3A_DQ34
DDR3A_A3	N2	A3	DQ3	F8	DDR3A_DQ35
DDR3A_A4	P8	A4	DQ4	H3	DDR3A_DQ36
DDR3A_A5	P2	A5	DQ5	H8	DDR3A_DQ37
DDR3A_A6	R8	A6	DQ6	G2	DDR3A_DQ38
DDR3A_A7	R2	A7	DQ7	H7	DDR3A_DQ39
DDR3A_A8	T8	A8	DQ8	D7	RN4B 2 15 51
DDR3A_A9	R3	A9	DQ9	C3	RN4C 3 14 51
DDR3A_A10	L7	A10/AP	DQ10	C8	RN4D 4 13 51
DDR3A_A11	R7	A11	DQ11	C2	RN4E 5 12 51
DDR3A_A12	N7	A12/BCn	DQ12	A7	RN4F 6 11 51
DDR3A_A13	T3	A13	DQ13	A2	RN4G 7 10 51
			DQ14	B8	RN4A 1 16 51
DDR3A_CKE	K9	CKE	DQ15	A3	RN4H 8 9 51
DDR3A_CLK_P	J7	CK_P	DQS_P0	F3	DDR3A_DQS_P4
DDR3A_CLK_N	K7	CK_N	DQS_N0	G3	DDR3A_DQS_N4
DDR3A_DM4	E7	DM0	DQS_P1	C7	240 R286
DDR3A_DM3	D3	DM1	DQS_N1	B7	240 R287
DDR3A_CSn	L2	CS			
DDR3A_WEn	L3	WE	NC1	J1	
DDR3A_RASn	J3	RAS	NC2	J9	
DDR3A_CASn	K3	CAS	NC3	L1	
			NC4	L9	
DDR3A_BA0	M2	BA0	NC5	M7	
DDR3A_BA1	N8	BA1	NC6	T7	
DDR3A_BA2	M3	BA2			
DDR3A_RESETn	T2	RESETn			
DDR3A_ODT	K1	ODT			
DDR3A_ZQ03	L8	ZQ			
VREF_DDR3A	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
			VSS	A9	
1.5V_DDR3	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

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U27 — DDR3 Device

DDR3A_A0	N3	A0	DQ0	E3	DDR3A_DQ16
DDR3A_A1	P7	A1	DQ1	F7	DDR3A_DQ17
DDR3A_A2	P3	A2	DQ2	F2	DDR3A_DQ18
DDR3A_A3	N2	A3	DQ3	F8	DDR3A_DQ19
DDR3A_A4	P8	A4	DQ4	H3	DDR3A_DQ20
DDR3A_A5	P2	A5	DQ5	H8	DDR3A_DQ21
DDR3A_A6	R8	A6	DQ6	G2	DDR3A_DQ22
DDR3A_A7	R2	A7	DQ7	H7	DDR3A_DQ23
DDR3A_A8	T8	A8	DQ8	D7	DDR3A_DQ24
DDR3A_A9	R3	A9	DQ9	C3	DDR3A_DQ25
DDR3A_A10	L7	A10/AP	DQ10	C8	DDR3A_DQ26
DDR3A_A11	R7	A11	DQ11	C2	DDR3A_DQ27
DDR3A_A12	N7	A12/BCn	DQ12	A7	DDR3A_DQ28
DDR3A_A13	T3	A13	DQ13	A2	DDR3A_DQ29
			DQ14	B8	DDR3A_DQ30
DDR3A_CKE	K9	CKE	DQ15	A3	DDR3A_DQ31
DDR3A_CLK_P	J7	CK_P	DQS_P0	F3	DDR3A_DQS_P2
DDR3A_CLK_N	K7	CK_N	DQS_N0	G3	DDR3A_DQS_N2
DDR3A_DM2	E7	DM0	DQS_P1	C7	DDR3A_DQS_P3
DDR3A_DM3	D3	DM1	DQS_N1	B7	DDR3A_DQS_N3
DDR3A_CSn	L2	CS			
DDR3A_WEn	L3	WE	NC1	J1	
DDR3A_RASn	J3	RAS	NC2	J9	
DDR3A_CASn	K3	CAS	NC3	L1	
			NC4	L9	
DDR3A_BA0	M2	BA0	NC5	M7	
DDR3A_BA1	N8	BA1	NC6	T7	
DDR3A_BA2	M3	BA2			
DDR3A_RESETn	T2	RESETn			
DDR3A_ODT	K1	ODT			
DDR3A_ZQ02	L8	ZQ			
VREF_DDR3A	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
			VSS	A9	
1.5V_DDR3	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

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U26 — DDR3 Device

DDR3A_A0	N3	A0	DQ0	E3	DDR3A_DQ0
DDR3A_A1	P7	A1	DQ1	F7	DDR3A_DQ1
DDR3A_A2	P3	A2	DQ2	F2	DDR3A_DQ2
DDR3A_A3	N2	A3	DQ3	F8	DDR3A_DQ3
DDR3A_A4	P8	A4	DQ4	H3	DDR3A_DQ4
DDR3A_A5	P2	A5	DQ5	H8	DDR3A_DQ5
DDR3A_A6	R8	A6	DQ6	G2	DDR3A_DQ6
DDR3A_A7	R2	A7	DQ7	H7	DDR3A_DQ7
DDR3A_A8	T8	A8	DQ8	D7	DDR3A_DQ8
DDR3A_A9	R3	A9	DQ9	C3	DDR3A_DQ9
DDR3A_A10	L7	A10/AP	DQ10	C8	DDR3A_DQ10
DDR3A_A11	R7	A11	DQ11	C2	DDR3A_DQ11
DDR3A_A12	N7	A12/BCn	DQ12	A7	DDR3A_DQ12
DDR3A_A13	T3	A13	DQ13	A2	DDR3A_DQ13
			DQ14	B8	DDR3A_DQ14
4 DDR3A_CKE	K9	CKE	DQ15	A3	DDR3A_DQ15
4 DDR3A_CLK_P	J7	CK_P	DQS_P0	F3	DDR3A_DQS_P0
4 DDR3A_CLK_N	K7	CK_N	DQS_N0	G3	DDR3A_DQS_N0
DDR3A_DM0	E7	DM0	DQS_P1	C7	DDR3A_DQS_P1
DDR3A_DM1	D3	DM1	DQS_N1	B7	DDR3A_DQS_N1
4 DDR3A_CSn	L2	CS			
4 DDR3A_WEn	L3	WE	NC1	J1	
4 DDR3A_RASn	J3	RAS	NC2	J9	
4 DDR3A_CASn	K3	CAS	NC3	L1	
			NC4	L9	
DDR3A_BA0	M2	BA0	NC5	M7	
DDR3A_BA1	N8	BA1	NC6	T7	
DDR3A_BA2	M3	BA2			
4 DDR3A_RESETn	T2	RESETn			
4 DDR3A_ODT	K1	ODT			
DDR3A_ZQ01	L8	ZQ			
VREF_DDR3A	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
			VSS	A9	
1.5V_DDR3	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

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Place These Caps Near DDR3 (U26, U27, and U28)

1.5V_DDR3

C487	C472	C500	C473	C437	C482	C436	C531	C470	C494	C471	C484	C497	C501	C498	C495	C483	C511	C485	C454
2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	3.3nF	3.3nF	4.7nF	4.7nF	4.7nF	0.01uF	0.01uF	0.01uF	0.01uF

1.5V_DDR3

C455	C509	C450	C510	C452	C512	C481	C486	C456	C513	C532	C457	C458	C530	C453	C451				
0.01uF	0.01uF	0.01uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.47uF	0.47uF	0.47uF	0.47uF	0.47uF	0.47uF				

Title	Cyclone V GT FPGA Development Kit Board	
Size B	Document Number 150-0321004-B1 (6XX-44179R)	Rev B
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DDR3B (x64 Soft Memory Controller)

DDR3B INTERFACE

DDR3B_BA[2:0] 5
DDR3B_DM[7:0] 5,9
DDR3B_DQS_P[7:0] 5
DDR3B_DQS_N[7:0] 5
DDR3B_DQ[63:0] 5,9
DDR3B_A[13:0] 5,9

V8 DDR3B_CLK_P 200 R323 DDR3B_CLK_N V9
DDR3B_CLK_P 200 R222 DDR3B_CLK_N

Place one termination resistor at the end of each branch.

VTT_DDR3B CN1 0.1uF
VTT_DDR3B CN2 0.1uF
VTT_DDR3B CN3 0.1uF

1.5V_DDR3
V33 DDR3B_RESETn R275 51
V7 DDR3B_CKE R265 4.70K, 1%

VTT_DDR3B

V30	DDR3B_A9	RN2A	1	16 51
V16	DDR3B_A11	RN2D	4	13 51
V17	DDR3B_A8	RN2G	7	10 51
V25	DDR3B_BA0	RN3B	2	15 51
V26	DDR3B_A0	RN3E	5	12 51
V31	DDR3B_A7	RN3H	8	9 51
V22	DDR3B_WEn	RN1C	3	14 51
V21	DDR3B_CASn	RN1F	6	11 51

VTT_DDR3B

V32	DDR3B_A13	RN2B	2	15 51
V13	DDR3B_A4	RN2E	5	12 51
		RN2H	8	9 51
V24	DDR3B_BA2	RN3C	3	14 51
V29	DDR3B_A5	RN3F	6	11 51
V14	DDR3B_A1	RN1A	1	16 51
V10	DDR3B_A10	RN1D	4	13 51
		RN1G	7	10 51

VTT_DDR3B

V12	DDR3B_A12	RN2C	3	14 51
V15	DDR3B_A6	RN2F	6	11 51
V23	DDR3B_CSn	RN3A	1	16 51
V27	DDR3B_A3	RN3D	4	13 51
V28	DDR3B_A2	RN3G	7	10 51
V11	DDR3B_BA1	RN1B	2	15 51
V32	DDR3B_ODT	RN1E	5	12 51
V20	DDR3B_RASn	RN1H	8	9 51

U30 DDR3 Device — MT41K128M16JT

DDR3B_A0	N3	A0	DQ0	E3	DDR3B_DQ0
DDR3B_A1	P7	A1	DQ1	F7	DDR3B_DQ1
DDR3B_A2	P3	A2	DQ2	F2	DDR3B_DQ2
DDR3B_A3	N2	A3	DQ3	F8	DDR3B_DQ3
DDR3B_A4	P8	A4	DQ4	H3	DDR3B_DQ4
DDR3B_A5	P2	A5	DQ5	H8	DDR3B_DQ5
DDR3B_A6	R8	A6	DQ6	G2	DDR3B_DQ6
DDR3B_A7	R2	A7	DQ7	H7	DDR3B_DQ7
DDR3B_A8	T8	A8	DQ8	D7	DDR3B_DQ8
DDR3B_A9	R3	A9	DQ9	C3	DDR3B_DQ9
DDR3B_A10	L7	A10/AP	DQ10	C8	DDR3B_DQ10
DDR3B_A11	R7	A11	DQ11	C2	DDR3B_DQ11
DDR3B_A12	N7	A12/BCn	DQ12	A7	DDR3B_DQ12
DDR3B_A13	T3	A13	DQ13	A2	DDR3B_DQ13
			DQ14	B8	DDR3B_DQ14
DDR3B_CKE	K9	CKE	DQ15	A3	DDR3B_DQ15
DDR3B_CLK_P	J7	CK_P		F3	DDR3B_DQS_P0
DDR3B_CLK_N	K7	CK_N	DQS_P0	G3	DDR3B_DQS_N0
			DQS_N0	C7	DDR3B_DQS_P1
DDR3B_DM0	E7	DM0	DQS_P1	B7	DDR3B_DQS_N1
DDR3B_DM1	D3	DM1	DQS_N1		
DDR3B_CSn	L2	CS		J1	
DDR3B_WEn	L3	WE	NC1	J9	
DDR3B_RASn	J3	RAS	NC2	L1	
DDR3B_CASn	K3	CAS	NC3	L9	
			NC4	M7	
DDR3B_BA0	M2	BA0	NC5	T7	
DDR3B_BA1	N8	BA1	NC6		
DDR3B_BA2	M3	BA2			
DDR3B_RESETn	T2	RESETn			
DDR3B_ODT	K1	ODT			
DDR3B_ZQ1	L8	ZQ			
VREF_DDR3B		VREFDQ	VSSQ	B1	
	H1	VREFCA	VSSQ	B9	
	M8		VSSQ	D1	
			VSSQ	D8	
	B2	VDD	VSSQ	E2	
	D9	VDD	VSSQ	E8	
	G7	VDD	VSSQ	F9	
	K2	VDD	VSSQ	G1	
	K8	VDD	VSSQ	G9	
	N1	VDD			
	N9	VDD	VSS	J2	
	R1	VDD	VSS	J8	
	R9	VDD	VSS	A9	
		VDD	VSS	M1	
			VSS	M9	
	A1	VDDQ	VSS	B3	
	A8	VDDQ	VSS	P1	
	C1	VDDQ	VSS	P9	
	C9	VDDQ	VSS	E1	
	D2	VDDQ	VSS	T1	
	E9	VDDQ	VSS	T9	
	F1	VDDQ	VSS	G8	
	H2	VDDQ	VSS		
	H9	VDDQ			

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U22 DDR3 Device — MT41K128M16JT

DDR3B_A0	N3	A0	DQ0	E3	DDR3B_DQ16
DDR3B_A1	P7	A1	DQ1	F7	DDR3B_DQ17
DDR3B_A2	P3	A2	DQ2	F2	DDR3B_DQ18
DDR3B_A3	N2	A3	DQ3	F8	DDR3B_DQ19
DDR3B_A4	P8	A4	DQ4	H3	DDR3B_DQ20
DDR3B_A5	P2	A5	DQ5	H8	DDR3B_DQ21
DDR3B_A6	R8	A6	DQ6	G2	DDR3B_DQ22
DDR3B_A7	R2	A7	DQ7	H7	DDR3B_DQ23
DDR3B_A8	T8	A8	DQ8	D7	DDR3B_DQ24
DDR3B_A9	R3	A9	DQ9	C3	DDR3B_DQ25
DDR3B_A10	L7	A10/AP	DQ10	C8	DDR3B_DQ26
DDR3B_A11	R7	A11	DQ11	C2	DDR3B_DQ27
DDR3B_A12	N7	A12/BCn	DQ12	A7	DDR3B_DQ28
DDR3B_A13	T3	A13	DQ13	A2	DDR3B_DQ29
			DQ14	B8	DDR3B_DQ30
DDR3B_CKE	K9	CKE	DQ15	A3	DDR3B_DQ31
DDR3B_CLK_P	J7	CK_P		F3	DDR3B_DQS_P2
DDR3B_CLK_N	K7	CK_N	DQS_P0	G3	DDR3B_DQS_N2
			DQS_N0	C7	DDR3B_DQS_P3
DDR3B_DM2	E7	DM0	DQS_P1	B7	DDR3B_DQS_N3
DDR3B_DM3	D3	DM1	DQS_N1		
DDR3B_CSn	L2	CS		J1	
DDR3B_WEn	L3	WE	NC1	J9	
DDR3B_RASn	J3	RAS	NC2	L1	
DDR3B_CASn	K3	CAS	NC3	L9	
			NC4	M7	
DDR3B_BA0	M2	BA0	NC5	T7	
DDR3B_BA1	N8	BA1	NC6		
DDR3B_BA2	M3	BA2			
DDR3B_RESETn	T2	RESETn			
DDR3B_ODT	K1	ODT			
DDR3B_ZQ2	L8	ZQ			
VREF_DDR3B		VREFDQ	VSSQ	B1	
	H1	VREFCA	VSSQ	B9	
	M8		VSSQ	D1	
			VSSQ	D8	
	B2	VDD	VSSQ	E2	
	D9	VDD	VSSQ	E8	
	G7	VDD	VSSQ	F9	
	K2	VDD	VSSQ	G1	
	K8	VDD	VSSQ	G9	
	N1	VDD			
	N9	VDD	VSS	J2	
	R1	VDD	VSS	J8	
	R9	VDD	VSS	A9	
		VDD	VSS	M1	
			VSS	M9	
	A1	VDDQ	VSS	B3	
	A8	VDDQ	VSS	P1	
	C1	VDDQ	VSS	P9	
	C9	VDDQ	VSS	E1	
	D2	VDDQ	VSS	T1	
	E9	VDDQ	VSS	T9	
	F1	VDDQ	VSS	G8	
	H2	VDDQ	VSS		
	H9	VDDQ			

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U8 DDR3 Device — MT41K128M16JT

DDR3B_A0	N3	A0	DQ0	E3	DDR3B_DQ32
DDR3B_A1	P7	A1	DQ1	F7	DDR3B_DQ33
DDR3B_A2	P3	A2	DQ2	F2	DDR3B_DQ34
DDR3B_A3	N2	A3	DQ3	F8	DDR3B_DQ35
DDR3B_A4	P8	A4	DQ4	H3	DDR3B_DQ36
DDR3B_A5	P2	A5	DQ5	H8	DDR3B_DQ37
DDR3B_A6	R8	A6	DQ6	G2	DDR3B_DQ38
DDR3B_A7	R2	A7	DQ7	H7	DDR3B_DQ39
DDR3B_A8	T8	A8	DQ8	D7	DDR3B_DQ40
DDR3B_A9	R3	A9	DQ9	C3	DDR3B_DQ41
DDR3B_A10	L7	A10/AP	DQ10	C8	DDR3B_DQ42
DDR3B_A11	R7	A11	DQ11	C2	DDR3B_DQ43
DDR3B_A12	N7	A12/BCn	DQ12	A7	DDR3B_DQ44
DDR3B_A13	T3	A13	DQ13	A2	DDR3B_DQ45
			DQ14	B8	DDR3B_DQ46
DDR3B_CKE	K9	CKE	DQ15	A3	DDR3B_DQ47
DDR3B_CLK_P	J7	CK_P		F3	DDR3B_DQS_P4
DDR3B_CLK_N	K7	CK_N	DQS_P0	G3	DDR3B_DQS_N4
			DQS_N0	C7	DDR3B_DQS_P5
DDR3B_DM4	E7	DM0	DQS_P1	B7	DDR3B_DQS_N5
DDR3B_DM5	D3	DM1	DQS_N1		
DDR3B_CSn	L2	CS		J1	
DDR3B_WEn	L3	WE	NC1	J9	
DDR3B_RASn	J3	RAS	NC2	L1	
DDR3B_CASn	K3	CAS	NC3	L9	
			NC4	M7	
DDR3B_BA0	M2	BA0	NC5	T7	
DDR3B_BA1	N8	BA1	NC6		
DDR3B_BA2	M3	BA2			
DDR3B_RESETn	T2	RESETn			
DDR3B_ODT	K1	ODT			
DDR3B_ZQ3	L8	ZQ			
VREF_DDR3B		VREFDQ	VSSQ	B1	
	H1	VREFCA	VSSQ	B9	
	M8		VSSQ	D1	
			VSSQ	D8	
	B2	VDD	VSSQ	E2	
	D9	VDD	VSSQ	E8	
	G7	VDD	VSSQ	F9	
	K2	VDD	VSSQ	G1	
	K8	VDD	VSSQ	G9	
	N1	VDD			
	N9	VDD	VSS	J2	
	R1	VDD	VSS	J8	
	R9	VDD	VSS	A9	
		VDD	VSS	M1	
			VSS	M9	
	A1	VDDQ	VSS	B3	
	A8	VDDQ	VSS	P1	
	C1	VDDQ	VSS	P9	
	C9	VDDQ	VSS	E1	
	D2	VDDQ	VSS	T1	
	E9	VDDQ	VSS	T9	
	F1	VDDQ	VSS	G8	
	H2	VDDQ	VSS		
	H9	VDDQ			

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U15 DDR3 Device — MT41K128M16JT

DDR3B_A0	N3	A0	DQ0	E3	DDR3B_DQ48
DDR3B_A1	P7	A1	DQ1	F7	DDR3B_DQ49
DDR3B_A2	P3	A2	DQ2	F2	DDR3B_DQ50
DDR3B_A3	N2	A3	DQ3	F8	DDR3B_DQ51
DDR3B_A4	P8	A4	DQ4	H3	DDR3B_DQ52
DDR3B_A5	P2	A5	DQ5	H8	DDR3B_DQ53
DDR3B_A6	R8	A6	DQ6	G2	DDR3B_DQ54
DDR3B_A7	R2	A7	DQ7	H7	DDR3B_DQ55
DDR3B_A8	T8	A8	DQ8	D7	DDR3B_DQ56
DDR3B_A9	R3	A9	DQ9	C3	DDR3B_DQ57
DDR3B_A10	L7	A10/AP	DQ10	C8	DDR3B_DQ58
DDR3B_A11	R7	A11	DQ11	C2	DDR3B_DQ59
DDR3B_A12	N7	A12/BCn	DQ12	A7	DDR3B_DQ60
DDR3B_A13	T3	A13	DQ13	A2	DDR3B_DQ61
			DQ14	B8	DDR3B_DQ62
DDR3B_CKE	K9	CKE	DQ15	A3	DDR3B_DQ63
DDR3B_CLK_P	J7	CK_P		F3	DDR3B_DQS_P6
DDR3B_CLK_N	K7	CK_N	DQS_P0	G3	DDR3B_DQS_N6
			DQS_N0	C7	DDR3B_DQS_P7
DDR3B_DM6	E7	DM0	DQS_P1	B7	DDR3B_DQS_N7
DDR3B_DM7	D3	DM1	DQS_N1		
DDR3B_CSn	L2	CS		J1	
DDR3B_WEn	L3	WE	NC1	J9	
DDR3B_RASn	J3	RAS	NC2	L1	
DDR3B_CASn	K3	CAS	NC3	L9	
			NC4	M7	
DDR3B_BA0	M2	BA0	NC5	T7	
DDR3B_BA1	N8	BA1	NC6		
DDR3B_BA2	M3	BA2			
DDR3B_RESETn	T2	RESETn			
DDR3B_ODT	K1	ODT			
DDR3B_ZQ4	L8	ZQ			
VREF_DDR3B		VREFDQ	VSSQ	B1	
	H1	VREFCA	VSSQ	B9	
	M8		VSSQ	D1	
			VSSQ	D8	
	B2	VDD	VSSQ	E2	
	D9	VDD	VSSQ	E8	
	G7	VDD	VSSQ	F9	
	K2	VDD	VSSQ	G1	
	K8	VDD	VSSQ	G9	
	N1	VDD			
	N9	VDD	VSS	J2	
	R1	VDD	VSS	J8	
	R9	VDD	VSS	A9	
		VDD	VSS	M1	
			VSS	M9	
	A1	VDDQ	VSS	B3	
	A8	VDDQ	VSS	P1	
	C1	VDDQ	VSS	P9	
	C9	VDDQ	VSS	E1	
	D2	VDDQ	VSS	T1	
	E9	VDDQ	VSS	T9	
	F1	VDDQ	VSS	G8	
	H2	VDDQ	VSS		
	H9	VDDQ			

R244 240, C297 0.1uF

Place These Caps Near DDR3 (U8, U15, U22 and U30)

1.5V_DDR3
C234 2.2nF, C217 2.2nF, C222 2.2nF, C266 2.2nF, C272 2.2nF, C389 2.2nF, C394 2.2nF, C443 2.2nF, C449 2.2nF, C267 3.3nF, C269 4.7nF, C364 4.7nF, C219 0.01uF, C268 0.01uF, C336 0.01uF, C524 0.01uF

1.5V_DDR3
C466 0.01uF, C250 0.1uF, C220 0.1uF, C270 0.1uF, C299 0.1uF, C392 0.1uF, C221 0.1uF, C271 0.47uF, C448 0.47uF, C393 0.47uF

1.5V_DDR3
C298 0.01uF, C490 0.1uF, C526 0.1uF, C467 0.1uF, C365 0.1uF, C447 0.1uF, C362 0.47uF, C300 0.47uF, C468 0.47uF, C523 0.47uF

1.5V_DDR3
C527 2.2nF, C464 2.2nF, C469 2.2nF, C522 2.2nF, C528 2.2nF, C366 2.2nF, C361 2.2nF, C296 2.2nF, C301 2.2nF, C444 3.3nF, C446 4.7nF, C525 4.7nF, C363 0.01uF, C426 0.01uF, C445 0.01uF, C391 0.01uF

Title: Cyclone V GT FPGA Development Kit Board

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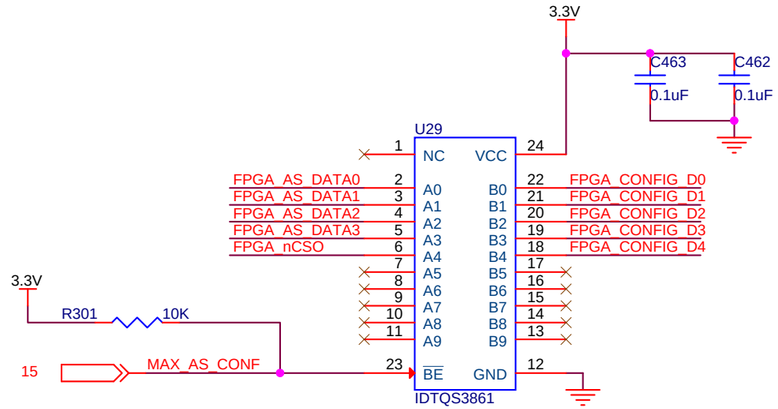
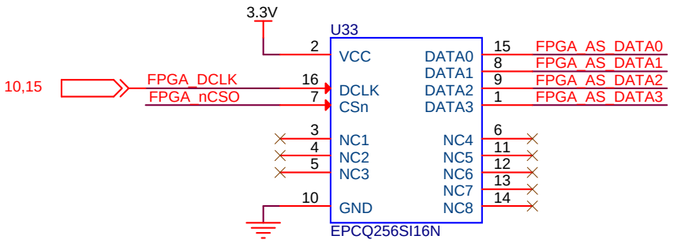
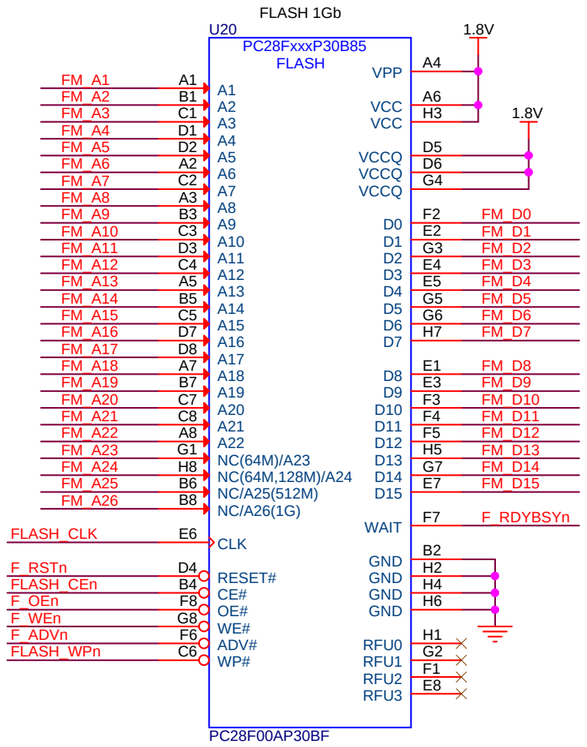
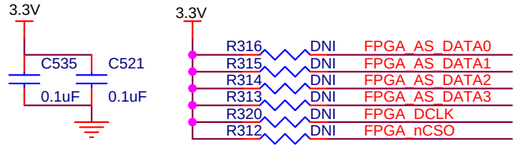
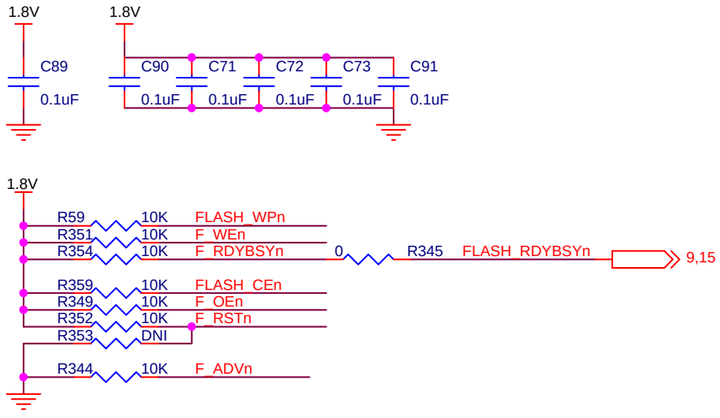
FLASH

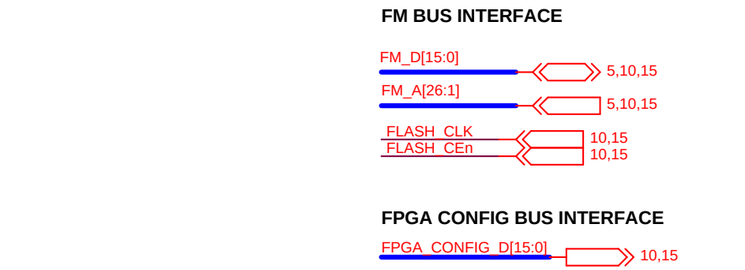


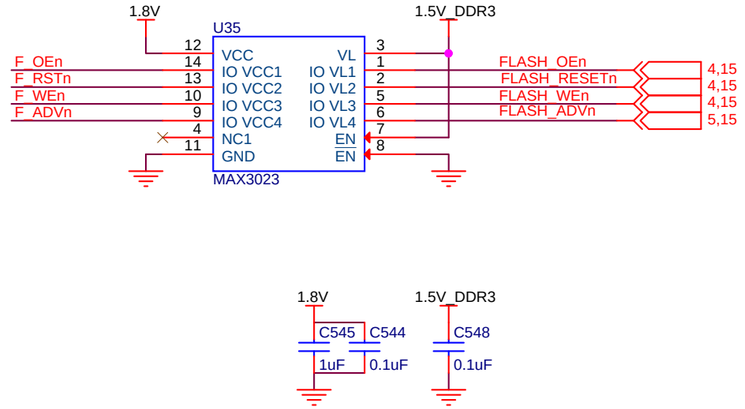












Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone V GT FPGA Development Kit Board**

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5M2210 System Controller

U32A — MAX V BANK1 — 5M2210ZF256

FPGA_CONFIG_D0	D3	DIFFIO_L1P	DIFFIO_L13P	J4	FPGA_nSTATUS
FPGA_CONFIG_D1	C2	DIFFIO_L1N	DIFFIO_L13N	K1	FPGA_CONF_DONE
FPGA_CONFIG_D2	C3	DIFFIO_L2P	DIFFIO_L14P	J3	FPGA_DCLK
FPGA_CONFIG_D3	E3	DIFFIO_L2N	DIFFIO_L14N	K2	
FPGA_CONFIG_D4	D2	DIFFIO_L3P	DIFFIO_L15P	K5	FPGA_CEn
FPGA_CONFIG_D5	E4	DIFFIO_L3N	DIFFIO_L15N	L1	
FPGA_CONFIG_D6	D1	DIFFIO_L4P	DIFFIO_L16P	L2	ASSP_CPLD_MRn
FPGA_CONFIG_D7	E5	DIFFIO_L4N	DIFFIO_L16N	K3	
FPGA_CONFIG_D8	F3	DIFFIO_L5P	DIFFIO_L17P	M1	EXTRA_SIG0
FPGA_CONFIG_D9	E1	DIFFIO_L5N	DIFFIO_L17N	M2	
FPGA_CONFIG_D10	F4	DIFFIO_L6P	DIFFIO_L18P	L4	
FPGA_CONFIG_D11	F2	DIFFIO_L6N	DIFFIO_L18N	L3	
FPGA_CONFIG_D12	F1	DIFFIO_L7P	DIFFIO_L19P	N1	FPGA_nCONFIG
FPGA_CONFIG_D13	F6	DIFFIO_L7N	DIFFIO_L19N	M4	
FPGA_CONFIG_D14	G2	DIFFIO_L8P	DIFFIO_L20P	N2	
FPGA_CONFIG_D15	G3	DIFFIO_L8N	DIFFIO_L20N	M3	
	G1	DIFFIO_L9P	DIFFIO_L21P	N3	FPGA_CvP_CONFDONE
	G4	DIFFIO_L9N	DIFFIO_L21N	P2	FPGA_PR_ERROR
MAX_AS_CONF	H2	DIFFIO_L10P			
	G5	DIFFIO_L10N	IOB1_1	E2	FPGA_PR_READY
	H3	DIFFIO_L11P	IOB1_2	F5	FPGA_PR_REQUEST
	J1	DIFFIO_L11N	IOB1_3	H1	FPGA_PR_DONE
	H4	DIFFIO_L12P	IOB1_4	K4	
	J2	DIFFIO_L12N	IOB1_5	L5	
USB_CLK	H5	IOB1/CLK0	TCK	P3	JTAG_TCK
CLK_CONFIG	J5	IOB1/CLK1	TDI	L6	JTAG_EPM2210_TDI
			TDO	M5	JTAG_BLASTER_TDI
			TMS	N4	JTAG_TMS

U32B — MAX V BANK2 — 5M2210ZF256

SI571_EN	D4	DIFFIO_T1P	DIFFIO_T13P	E10	
	B1	DIFFIO_T1N	DIFFIO_T13N	A11	
	C5	DIFFIO_T2P	DIFFIO_T14P	B11	
	C4	DIFFIO_T2N	DIFFIO_T14N	A12	
	B4	DIFFIO_T3P	DIFFIO_T15P	E11	MAX_CONF_DONE
	D6	DIFFIO_T3N	DIFFIO_T15N	B12	
	E6	DIFFIO_T4P	DIFFIO_T16P	C11	
	B5	DIFFIO_T4N	DIFFIO_T16N	B13	PGM_SEL
SENSE_SCK	A5	DIFFIO_T5P	DIFFIO_T17P	D12	PGM_CONFIG
SENSE_SDI	D7	DIFFIO_T5N	DIFFIO_T17N	B14	PGM_LED0
SENSE_SDO	B6	DIFFIO_T6P	DIFFIO_T18P	C13	PGM_LED1
SENSE_CSn	E7	DIFFIO_T6N	DIFFIO_T18N	B16	PGM_LED2
	C8	DIFFIO_T7P			
OVERTEMP	B7	DIFFIO_T7N			
	D8	DIFFIO_T8P	IOB2_6	A13	CLK_SEL
	A7	DIFFIO_T8N	IOB2_7	A15	CLK_ENABLE
HSMA_PRSNTn	B8	DIFFIO_T9P	IOB2_8	A2	FACTORY_USER
HSMB_PRSNTn	A8	DIFFIO_T9N	IOB2_9	A4	MAX_ERROR
	A9	DIFFIO_T10P	IOB2_10	A6	MAX_LOAD
CLK50_EN	E9	DIFFIO_T10N	IOB2_11	B10	FPGA_MSEL0
CLK125_EN	B9	DIFFIO_T11P	IOB2_12	B3	FPGA_MSEL1
CLOCK_SDA	D9	DIFFIO_T11N	IOB2_13	C10	FPGA_MSEL2
SI570_EN	A10	DIFFIO_T12P	IOB2_14	C12	FPGA_MSEL3
CLOCK_SCL	C9	DIFFIO_T12N	IOB2_15	C6	FPGA_MSEL4
				C7	
			IOB2_16	D10	CPU_RESETn
			IOB2_17	D11	SDI_A_TX_EN
			IOB2_18	D5	SDI_A_RX_BYPASS
			IOB2_19	E8	SDI_A_RX_EN
			IOB2_20		

JTAG_EPM2210_TDI — R340 — DNI — JTAG_BLASTER_TDI

INSTALL R340 ONLY WHEN MAX V IS NOT POPULATED.

U32C — MAX V BANK3 — 5M2210ZF256

	E14	DIFFIO_R1P	DIFFIO_R13P	J14	FM_D0
FM_A1	C14	DIFFIO_R1N	DIFFIO_R13N	J15	FM_D1
FM_A2	C15	DIFFIO_R2P	DIFFIO_R14P	K16	FM_D2
FM_A3	E13	DIFFIO_R2N	DIFFIO_R14N	K13	FM_D3
FM_A4	E12	DIFFIO_R3P	DIFFIO_R15P	K15	FM_D4
FM_A5	D15	DIFFIO_R3N	DIFFIO_R15N	K14	FM_D5
FM_A6	F14	DIFFIO_R4P	DIFFIO_R16P	L16	FM_D6
FM_A7	D16	DIFFIO_R4N	DIFFIO_R16N	L11	FM_D7
FM_A8	F13	DIFFIO_R5P	DIFFIO_R17P	L15	FM_D8
FM_A9	E15	DIFFIO_R5N	DIFFIO_R17N	L12	FM_D9
FM_A10	E16	DIFFIO_R6P	DIFFIO_R18P	M16	FM_D10
FM_A11	F15	DIFFIO_R6N	DIFFIO_R18N	L13	FM_D11
FM_A12	G14	DIFFIO_R7P	DIFFIO_R19P	M15	FM_D12
FM_A13	F16	DIFFIO_R7N	DIFFIO_R19N	L14	FM_D13
FM_A14	G13	DIFFIO_R8P	DIFFIO_R20P	N16	FM_D14
FM_A15	G15	DIFFIO_R8N	DIFFIO_R20N	M13	FM_D15
FM_A16	G12	DIFFIO_R9P	DIFFIO_R21P	N15	FORCE_FAN
FM_A17	G16	DIFFIO_R9N	DIFFIO_R21N	N14	
FM_A18	H14	DIFFIO_R10P	DIFFIO_R22P	P15	
FM_A19	H15	DIFFIO_R10N	DIFFIO_R22N	P14	
FM_A20	H13	DIFFIO_R11P			
FM_A21	H16	DIFFIO_R11N	IOB3_21	D13	
FM_A22	J13	DIFFIO_R12P	IOB3_22	D14	
	J16	DIFFIO_R12N	IOB3_23	F11	
			IOB3_24	F12	
			IOB3_25	K12	
CLKIN_MAX_50	J12	IOB3/CLK2	IOB3_26	M14	
	H12	IOB3/CLK3	IOB3_27	N13	

U32D — MAX V BANK4 — 5M2210ZF256

	R1	DIFFIO_B1P	DIFFIO_B14P	M10	MAX_OEn
FM_A26	P4	DIFFIO_B1N	DIFFIO_B14N	R10	MAX_CSn
FM_A25	T2	DIFFIO_B2P	DIFFIO_B15P	N10	MAX_WEn
FM_A24	P5	DIFFIO_B2N	DIFFIO_B15N	T11	MAX_CLK
FM_A23	R3	DIFFIO_B3P	DIFFIO_B16P	P10	
	N5	DIFFIO_B3N	DIFFIO_B16N	R11	
	P6	DIFFIO_B4P	DIFFIO_B17P	T12	
FLASH_WEn	N6	DIFFIO_B4N	DIFFIO_B17N	N11	
FLASH_CEn	R5	DIFFIO_B5P	DIFFIO_B19P	T13	EXTRA_SIG1
FLASH_OEn	M6	DIFFIO_B5N	DIFFIO_B19N	R13	
FLASH_RDYBSYn	T5	DIFFIO_B6P	DIFFIO_B18P	R12	ASSP_MODE
FLASH_RESETn	P7	DIFFIO_B6N	DIFFIO_B18N	P11	M570_CLOCK
FLASH_CLK	R6	DIFFIO_B7P	DIFFIO_B20P	N12	FACTORY_STATUS
FLASH_ADVn	N7	DIFFIO_B7N	DIFFIO_B20N	R14	FACTORY_REQUEST
	M7	DIFFIO_B8P	DIFFIO_B21P	P12	M570_PCIE_JTAG_EN
	R7	DIFFIO_B8N	DIFFIO_B21N	T15	EXTRA_SIG2
USB_CFG2	P8	DIFFIO_B9P	DIFFIO_B22P	R16	
USB_CFG3	T7	DIFFIO_B9N	DIFFIO_B22N	P13	
USB_CFG4	N8	DIFFIO_B10P	IOB4_28	M11	
USB_CFG5	R8	DIFFIO_B10N	IOB4_29	M12	
USB_CFG6	T8	DIFFIO_B11P	IOB4_30	N9	
USB_CFG7	T9	DIFFIO_B11N	IOB4_31	R4	USB_CFG0
USB_CFG8	R9	DIFFIO_B12P	IOB4_32	T10	USB_CFG11
USB_CFG9	P9	DIFFIO_B12N	IOB4_33	T4	USB_CFG1
MAX_RESETn	M9	DIFFIO_B13N/DEV_CLRn			
USB_CFG10	M8	DIFFIO_B13P/DEV_OE			

U32E — MAX V Power — 5M2210ZF256

	F7	GNDINT	VCCINT	F10	1.8V
	G6	GNDINT	VCCINT	G11	
	H7	GNDINT	VCCINT	H10	
	H9	GNDINT	VCCINT	H8	
	J10	GNDINT	VCCINT	J7	
	J8	GNDINT	VCCINT	J9	
	K11	GNDINT	VCCINT	K6	
	L10	GNDINT	VCCINT	L7	
	A1	GNDIO	VCCIO1	C1	2.5V
	A16	GNDIO	VCCIO1	H6	
	B15	GNDIO	VCCIO1	J6	
	B2	GNDIO	VCCIO1	P1	
	G10	GNDIO			
	G7	GNDIO	VCCIO2	A14	
	G8	GNDIO	VCCIO2	A3	
	G9	GNDIO	VCCIO2	F8	
	K10	GNDIO	VCCIO2	F9	
	K7	GNDIO			1.8V
	K8	GNDIO	VCCIO3	C16	
	K9	GNDIO	VCCIO3	H11	
	R15	GNDIO	VCCIO3	J11	
	R2	GNDIO	VCCIO3	P16	
	T1	GNDIO			
	T16	GNDIO	VCCIO4	L8	
	T6	GNDIO	VCCIO4	L9	
			VCCIO4	T14	
			VCCIO4	T3	

2.5V — X2 (EN, VCC, GND, OUT) 100MHz — 2.5V — CLK_CONFIG

C478 2.2uF — C477 0.1uF

VCCINT (1.8V): C514 C546 C502 C536 C519 C533 C534 C520 — 0.1uF

2.5V VCCIO (2.5V): C537 C476 C475 C505 C504 C503 — 0.1uF

1.8V VCCIO (1.8V): C474 C547 C518 C515 C516 C517 — 0.1uF

FPGA CONFIG INTERFACE

FPGA_CONFIG_D[15:0]	10,14
FPGA_nSTATUS	10
FPGA_CONF_DONE	10
FPGA_DCLK	10,14
FPGA_nCONFIG	10
FPGA_PR_DONE	10
FPGA_PR_REQUEST	10
FPGA_PR_READY	10
FPGA_PR_ERROR	10
FPGA_CvP_CONFDONE	10
FPGA_MSEL0	10
FPGA_MSEL1	10
FPGA_MSEL2	10
FPGA_MSEL3	10
FPGA_MSEL4	10
FPGA_CEn	10
OVERTEMP	29
SENSE_SDO	29
SENSE_CSn	29
SENSE_SDI	29
SENSE_SCK	29

JTAG INTERFACE

JTAG_BLASTER_TDI	11,19
JTAG_TCK	10,11,18,19
JTAG_EPM2210_TDI	11
JTAG_TMS	10,11,19
MAX_AS_CONF	14
ASSP_MODE	20
ASSP_CPLD_MRn	21

FLASH INTERFACE

FM_D[15:0]	5,10,14
FM_A[26:1]	5,10,14
FLASH_WEn	4,14
FLASH_CEn	10,14
FLASH_OEn	4,14
FLASH_RDYBSYn	9,14
FLASH_ADVn	5,14
FLASH_RESETn	4,14
FLASH_CLK	10,14

ON-BOARD USB BLASTER II

USB_CFG[11:0]	19
EXTRA_SIG[2:0]	19
USB_CLK	9,19
M570_PCIE_JTAG_EN	19
M570_CLOCK	19
FACTORY_STATUS	19
FACTORY_REQUEST	19

CLOCK INTERFACES

CLKIN_MAX_50	8
CLK125_EN	8
CLK50_EN	8
SI570_EN	8
SI571_EN	8
CLOCK_SDA	8
CLOCK_SCL	8

MAX CTL INTERFACE

MAX_OEn	5
MAX_CSn	5
MAX_WEn	5
MAX_CLK	9

SDI INTERFACE

SDI_A_TX_EN	4,16
SDI_A_RX_BYPASS	4,16
SDI_A_RX_EN	4,16

DIPSWITCH INTERFACE

CLK_SEL	8,20
CLK_ENABLE	20
FACTORY_USER	20
FORCE_FAN	10

PUSH BUTTON INTERFACE

PGM_SEL	20
PGM_CONFIG	20
CPU_RESETn	10,20

LED INTERFACE

PGM_LED[2:0]	20
MAX_RESETn	20
MAX_ERROR	20
MAX_LOAD	20
MAX_CONF_DONE	20
HSMA_PRSNTn	6,18,20
HSMB_PRSNTn	6,18,20

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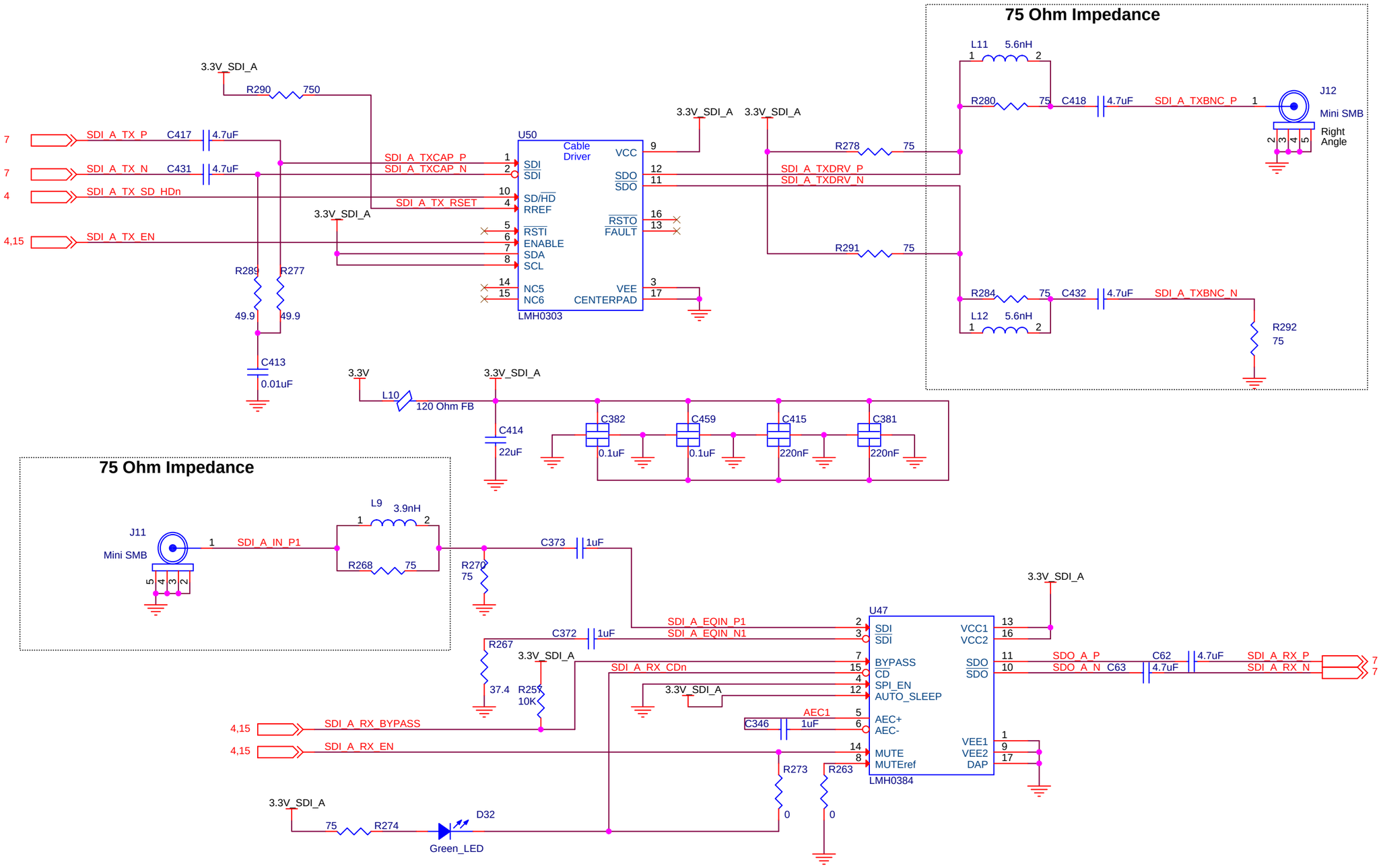
SDI Cable Driver, Equalizer, and SMB



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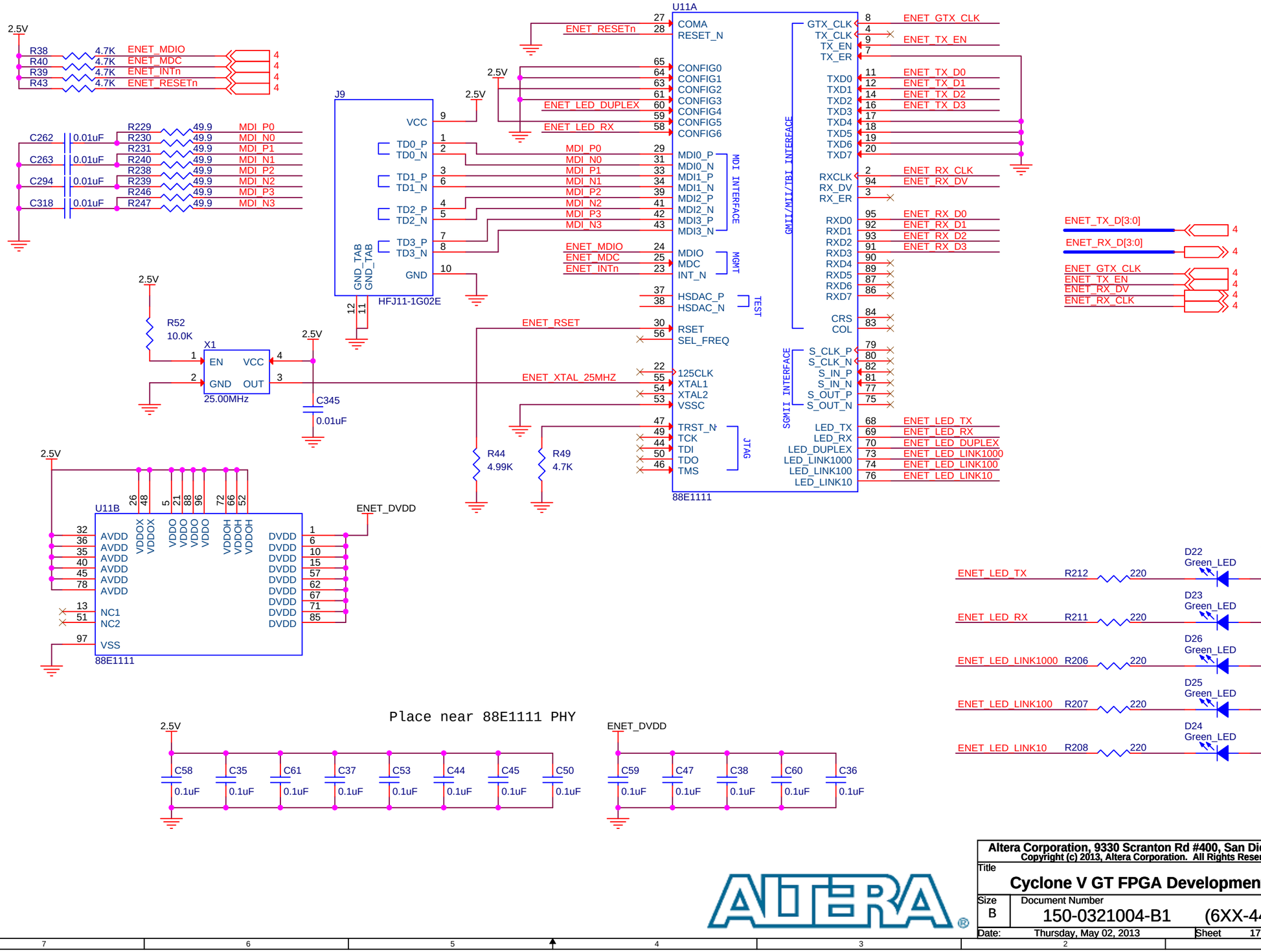
10/100/1000 Ethernet

RGMII Mode (default)



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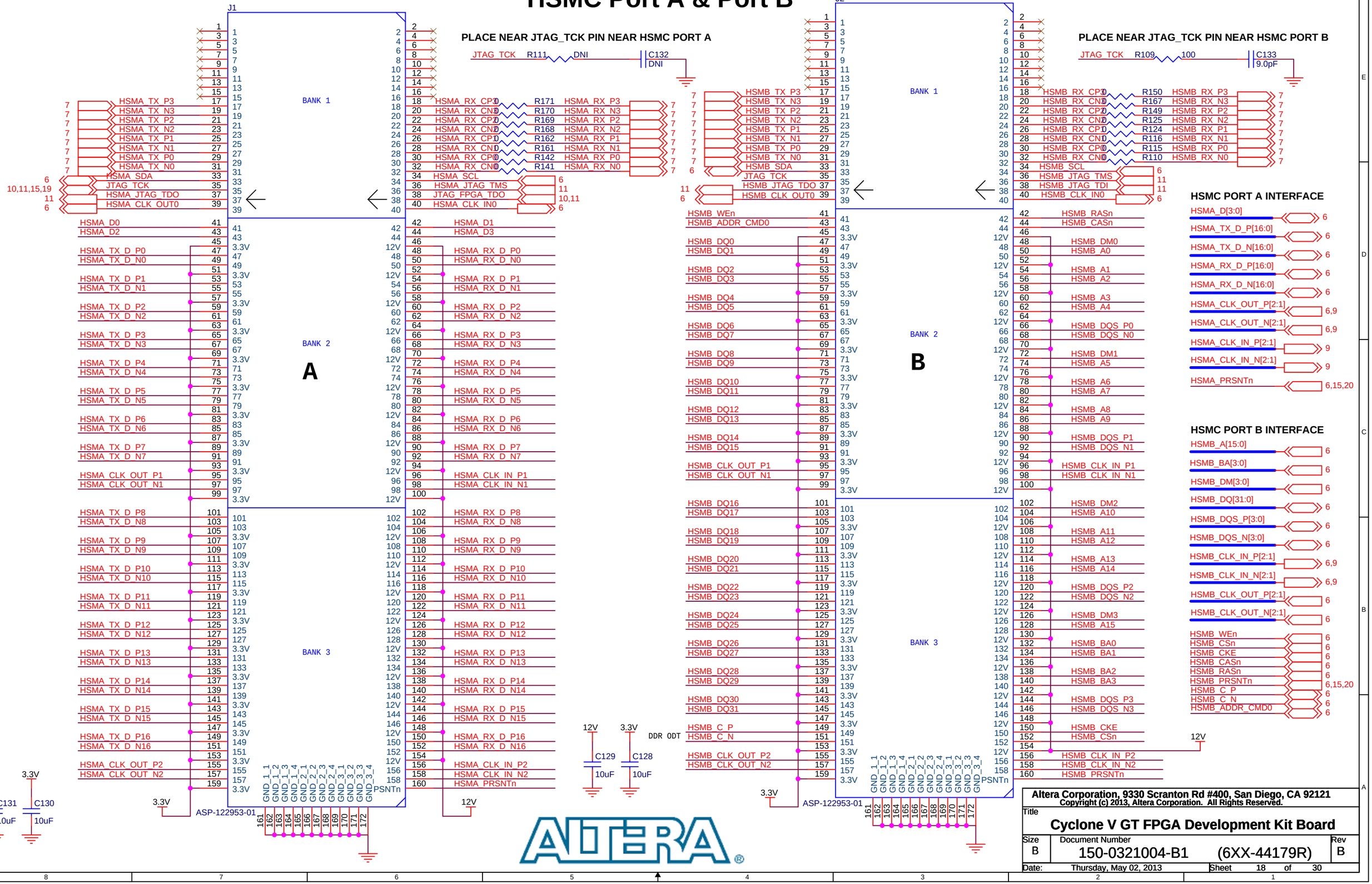
HSMC Port A & Port B



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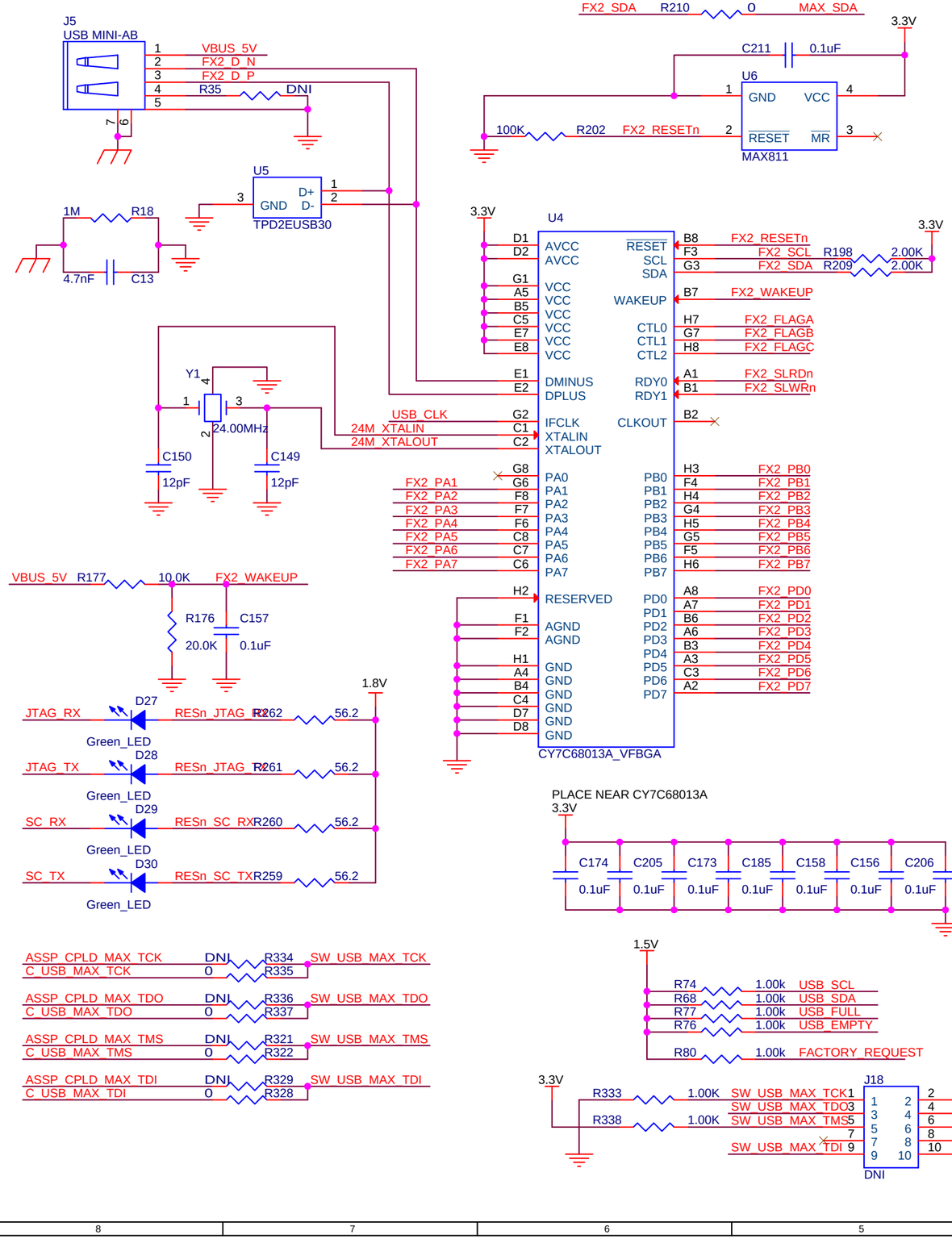
On-Board USB Blaster II



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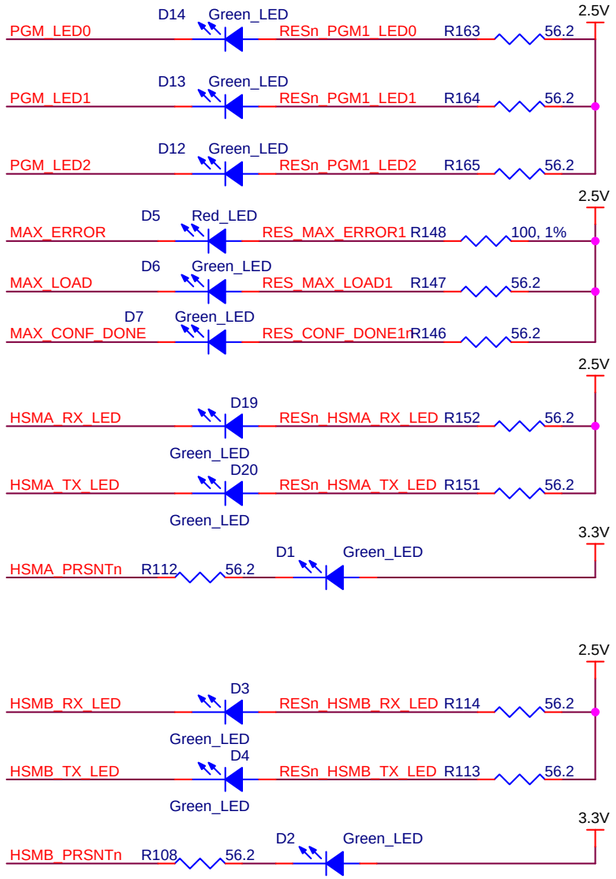
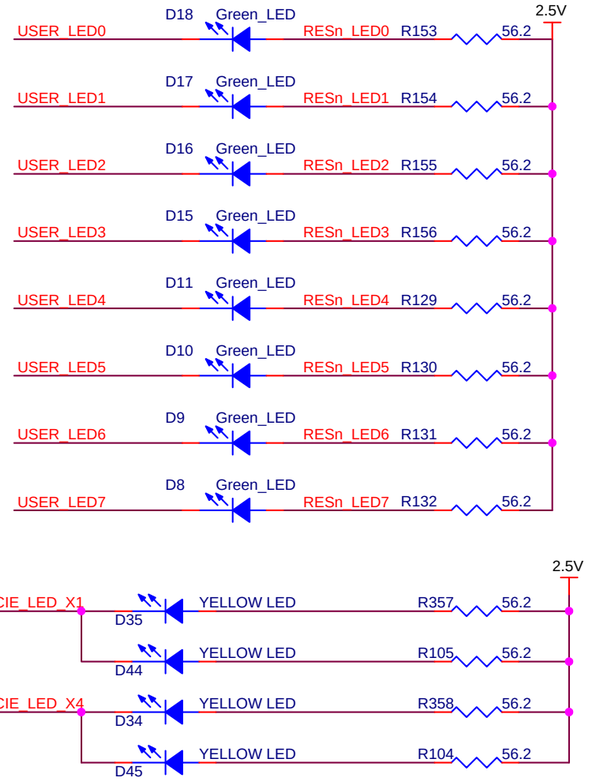
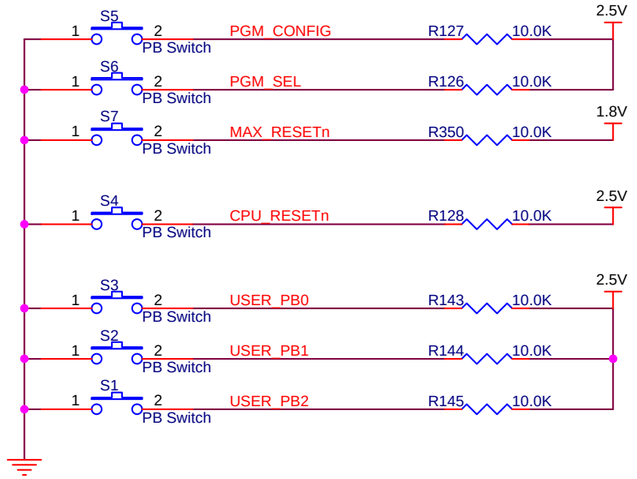
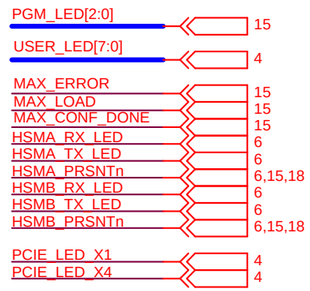
User I/O



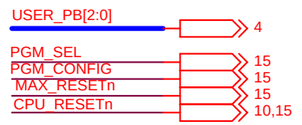




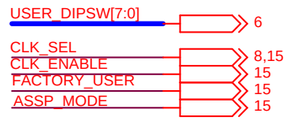
LED INTERFACE

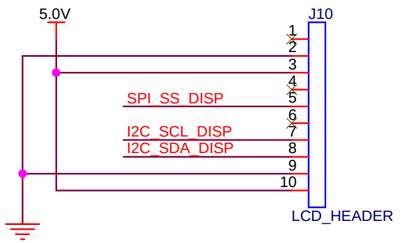


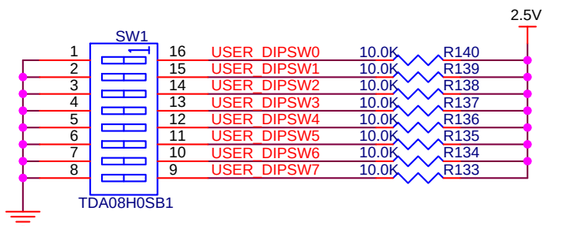
PUSH BUTTON INTERFACE

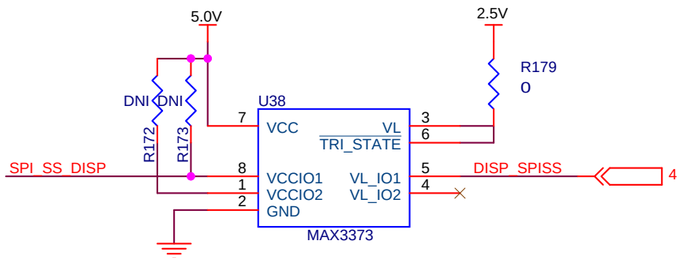


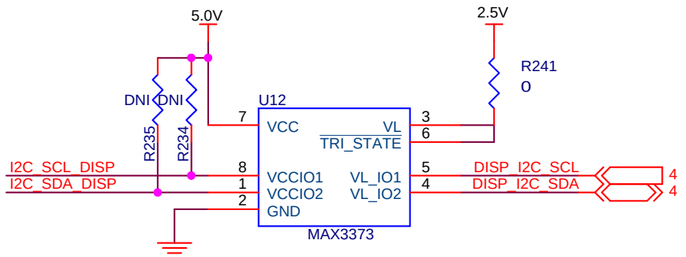
DIP SWITCH INTERFACE











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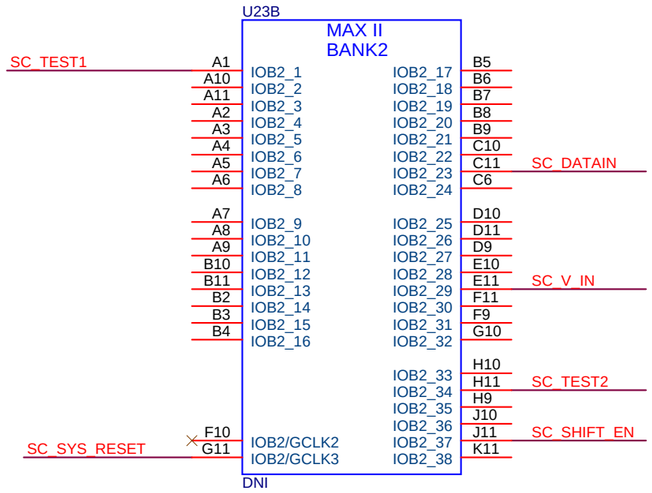
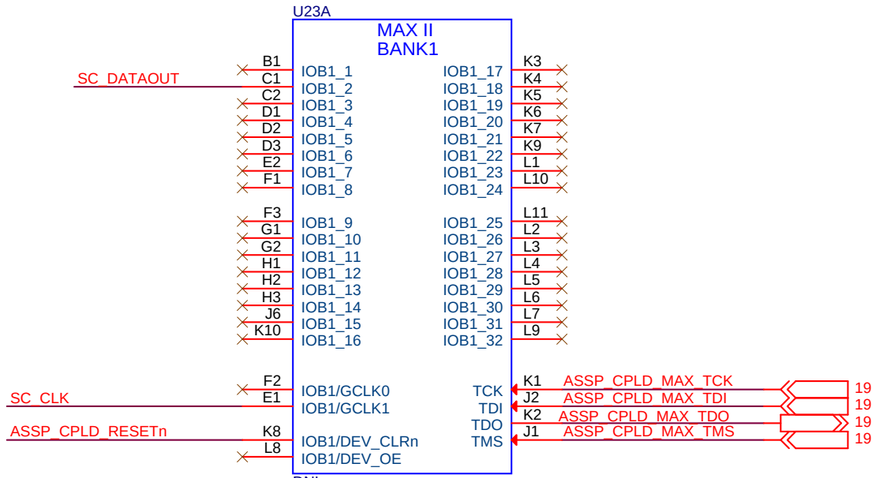
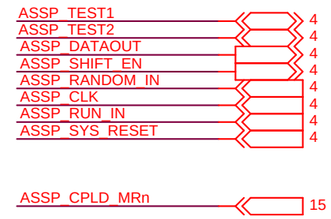
ASSP CPLD

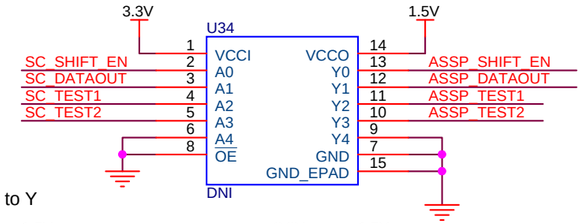


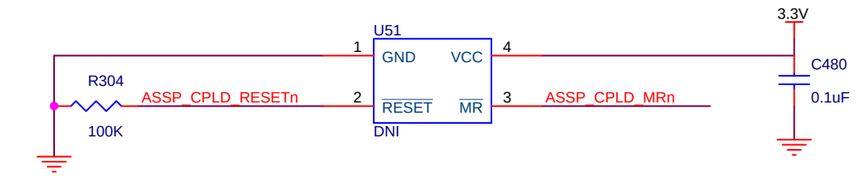


MVE ASSP Core Interface

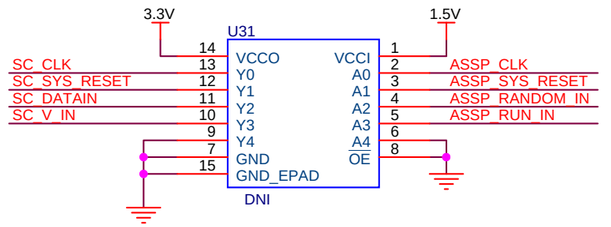


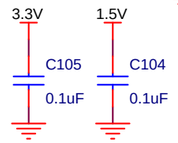
DATA FLOWS FROM A to Y



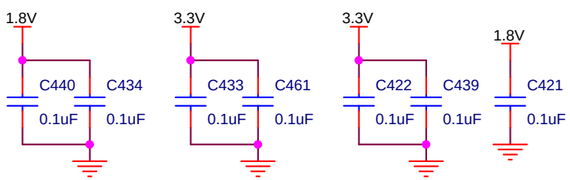


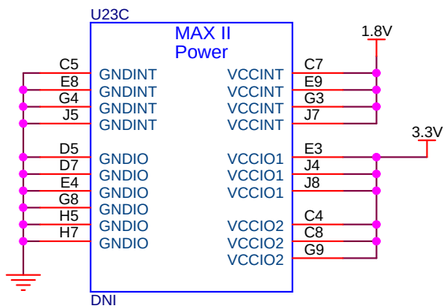
DATA FLOWS FROM A to Y

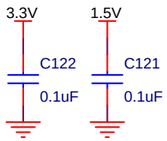




PLACE NEAR MAX II EPM570







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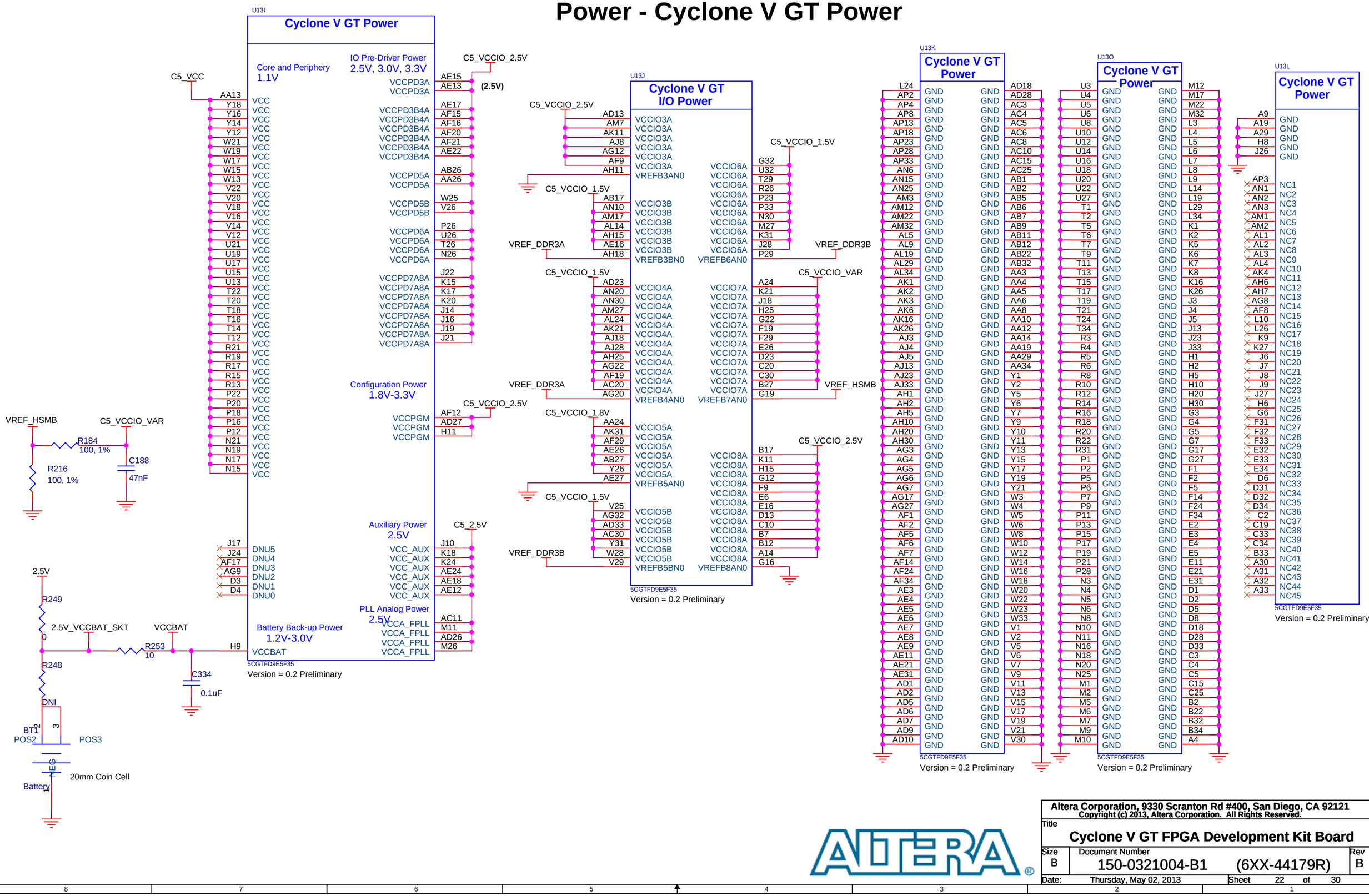
Power - Cyclone V GT Power



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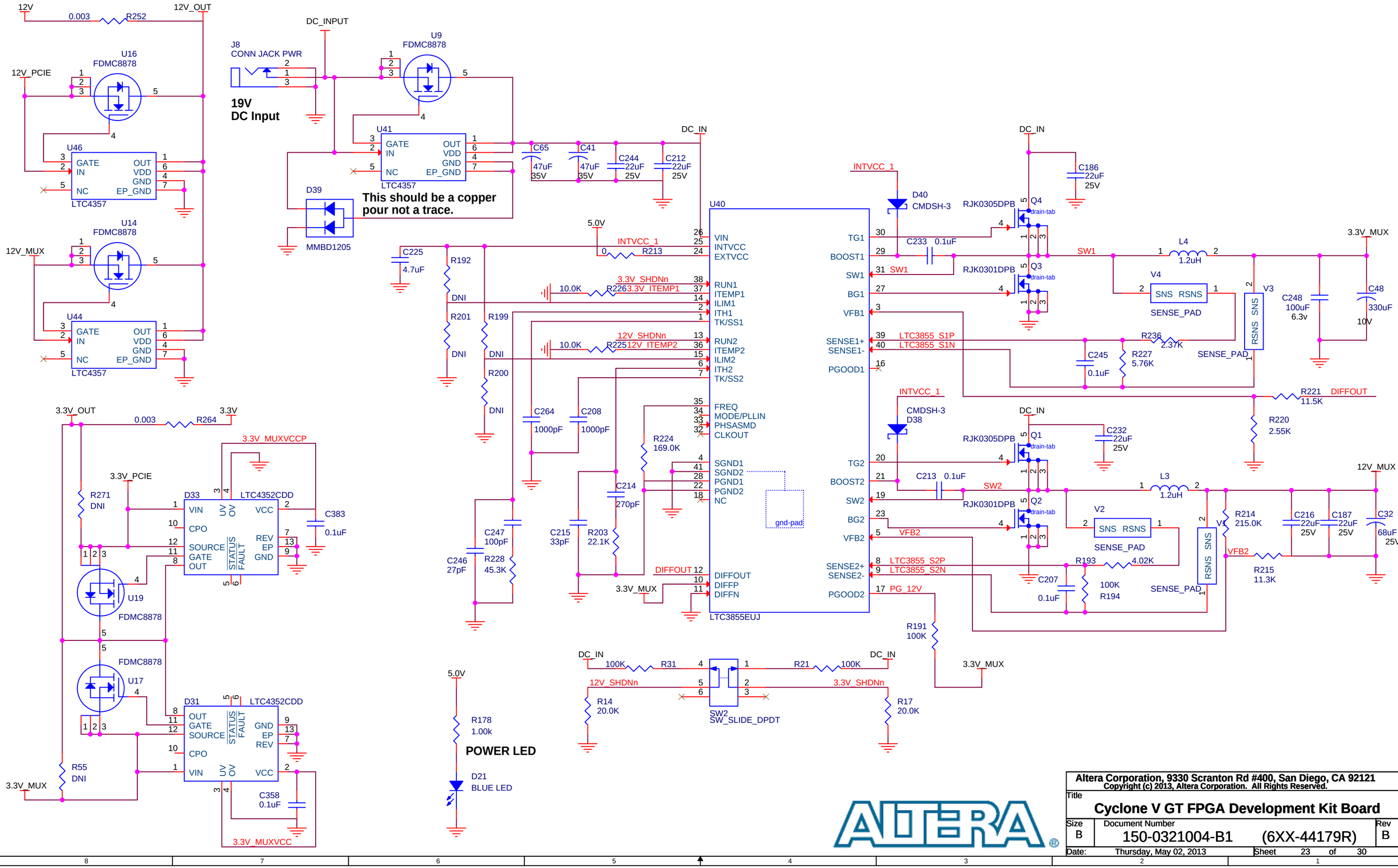
Power 1 - DC Input & 12V, 3.3V Output



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Power 2 - 1.1V (C5_VCC)

PGOOD_C5_VCC → 25,26,27,28

12V
C114 22uF 25V 1210
C508 22uF 25V 1210

CAD Note:
Regulator input caps
Place near regulator controller

U24B
LTC3613EWKH_6
PVIN2 PVIN3 PVIN4 PVIN5 PVIN6 PVIN7 PVIN8 PVIN9 PVIN10 PVIN11 PVIN12 PVIN13 PVIN14
SGND2 SGND3 SGND4 SGND5 SGND6 SGND7
SW2 SW3 SW4 SW5 SW6 SW7 SW8 SW9 NC
PGND2 PGND3 PGND4 PGND5 PGND6 PGND7 PGND8 PGND9
C5_VCC_SW

U24A
LTC3613EWKH_6
PGOOD SNS+ SNS- VOUT VOSNS- VOSNS+ TRACK/SS ITH VRNG RT SGND
BOOST SW1 SW2 PGND1 INTVCC1 INTVCC2 PVIN1 SVIN1 MODE/PLLIN EXTVCC NC RUN

PGOOD_C5_VCC R303 0 PGD_C5_VCC
C5_VCC_INTVCC R294 100K
C5_VCC_SNS_P R311 10 C479 1.0nF
C5_VCC_SNS_N R310 10
1.1V_REG_VCC
R102 13.7K 1%
R101 16.5K 1%
C5_VCC_REF
C5_VCC_TRACK
C106 0.01uF
47pF C101
R99 21K (1%)
270pF C438
C5_VCC_INTVCC R279 DNI
R88 0
R87 115K (1%)
FSW = 350kHz

C5_VCC_BOOST C110 0.1uF
D42 CMDSH-3
L7 0.47uH Isat = 20A
C5_VCC_SW1
C5_VCC_VOUT
744314047 Wurth Elektronik
C416 4.7uF
C5_VCC_INTVCC
C420 0.1uF
C489 22uF 25V 1210
C116 22uF 25V 1210
12V
C5_VCC_MODE 10.0K R282 DNI R283
C419 DNI
RUN_C5_VCC 10.0K R86
3.3V

C5_VCC_SNS_P
C5_VCC_SNS_N
V35 V36 RSNS SNS SENSE_PAD
R78 0.001
1.1V_REG_VCC
R70 0.001
C88 100UF 6.3V
C87 100UF 6.3V
C69 330uF 6.3V
C5_VCC

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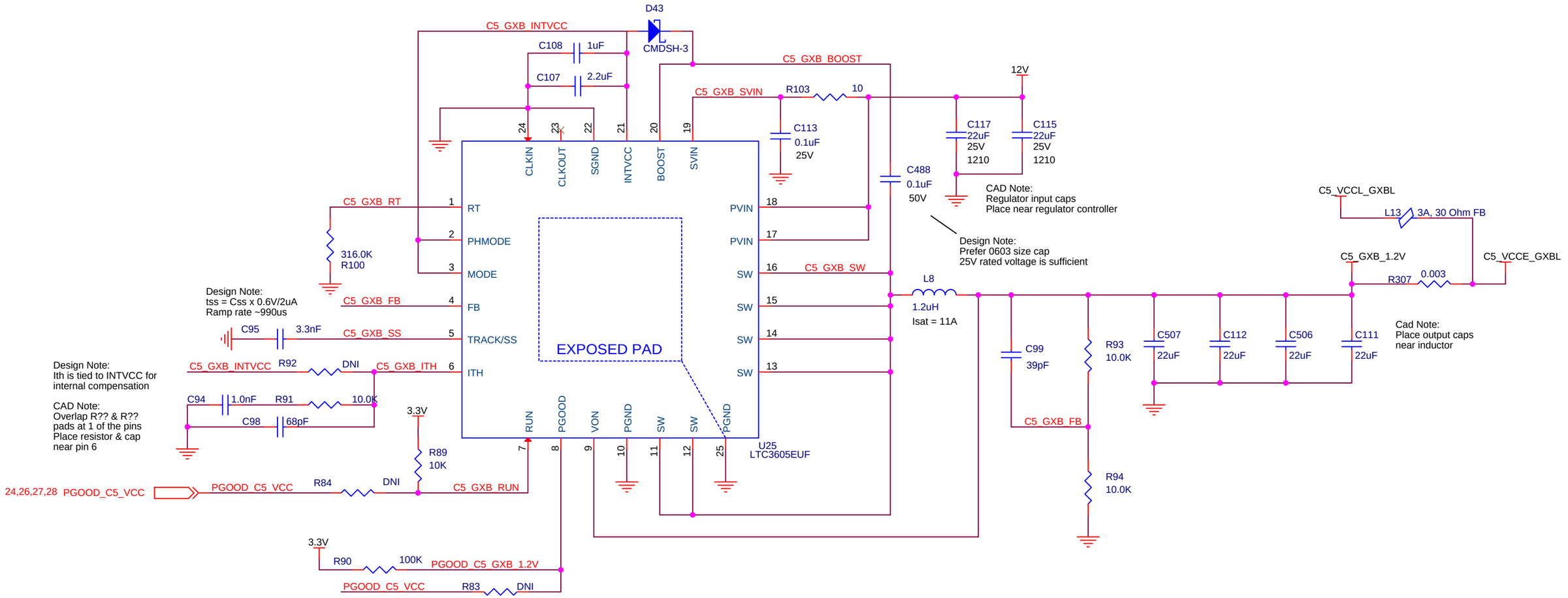
Power 3 - 1.2V (C5 GTB)



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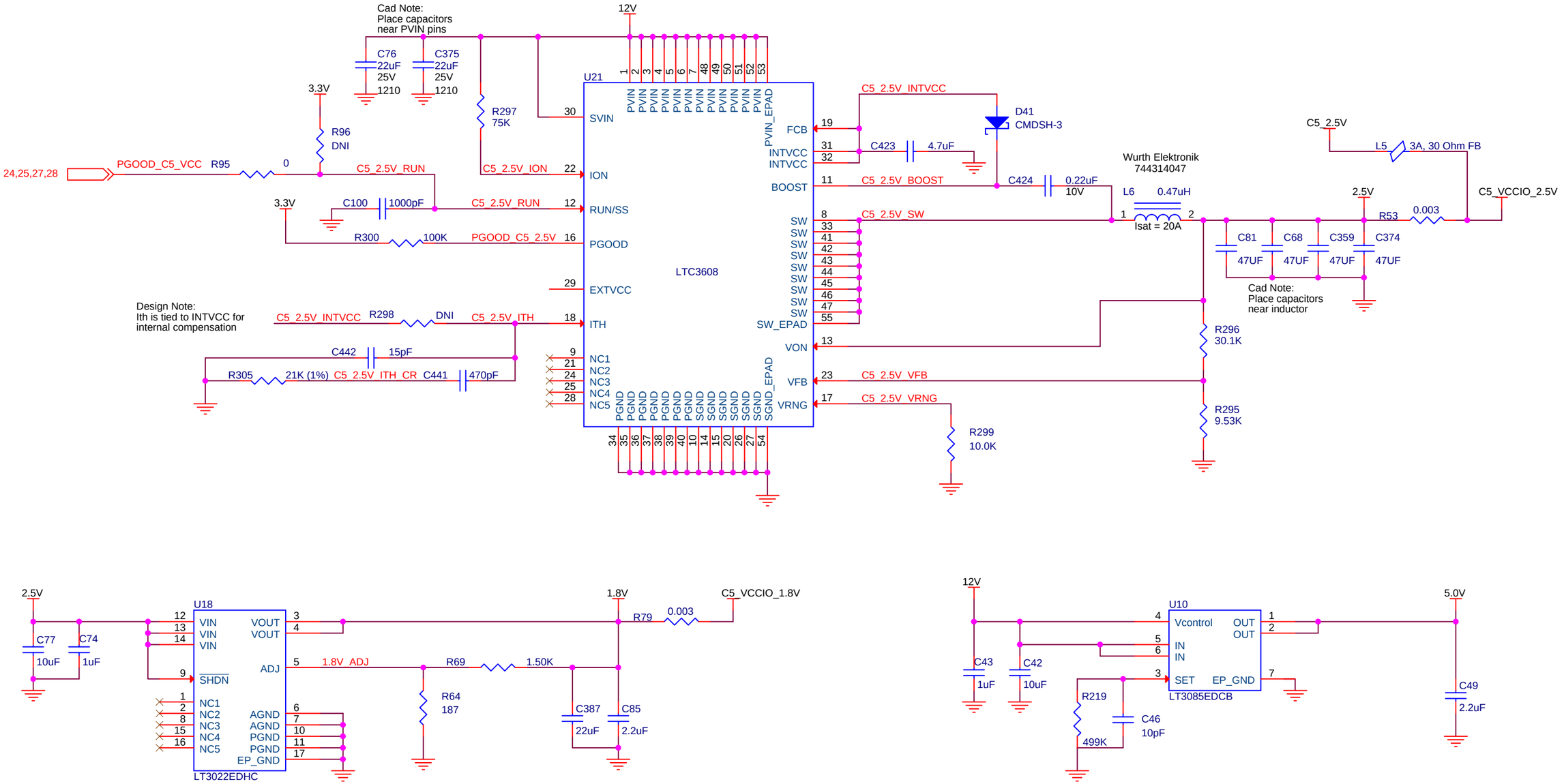
Power 4 - 2.5V (C5 2.5V), 1.8V & 5.0V



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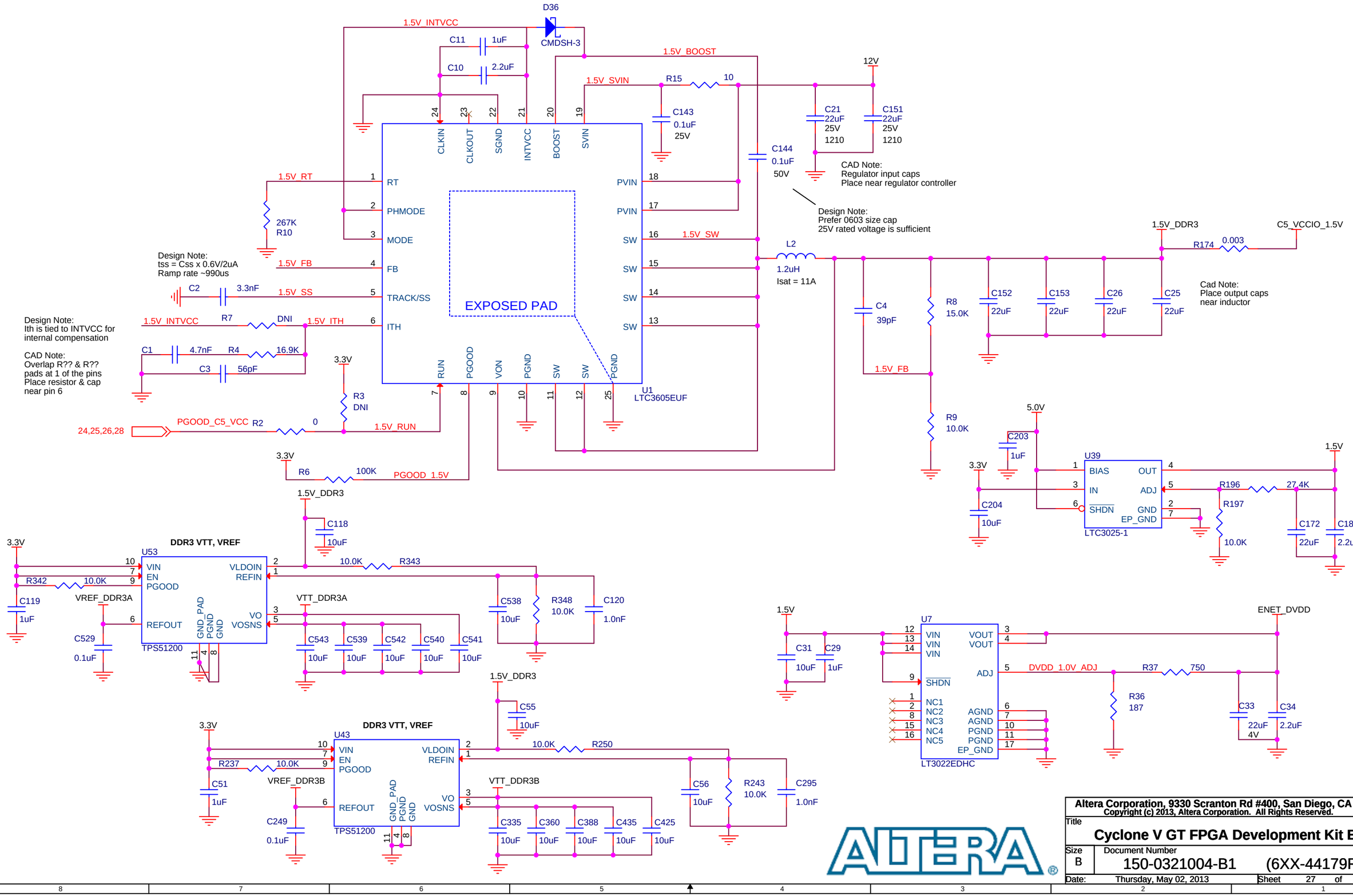
Power 5 - 1.5V, VTT_DDR3, VREF_DDR3, ENET_DVDD



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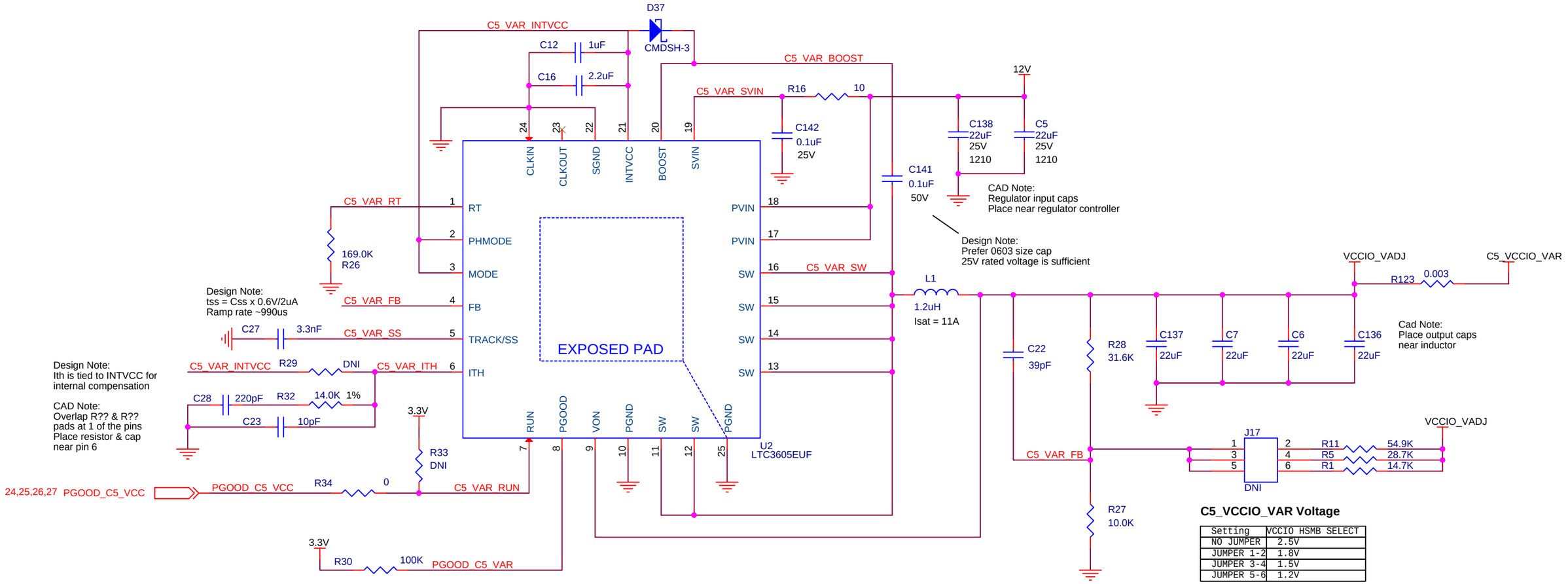
Power 6 - LTC3605 VAR



C5_VCCIO_VAR Voltage

Setting	VCCIO HSMB SELECT
NO JUMPER	2.5V
JUMPER 1-2	1.8V
JUMPER 3-4	1.5V
JUMPER 5-6	1.2V

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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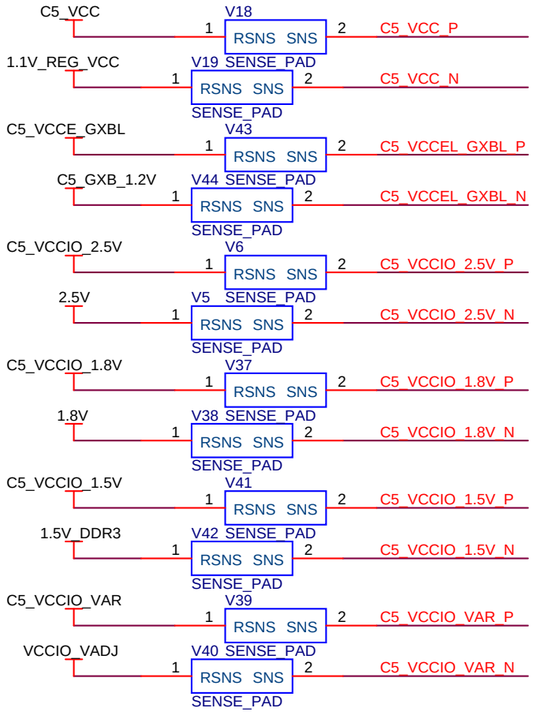
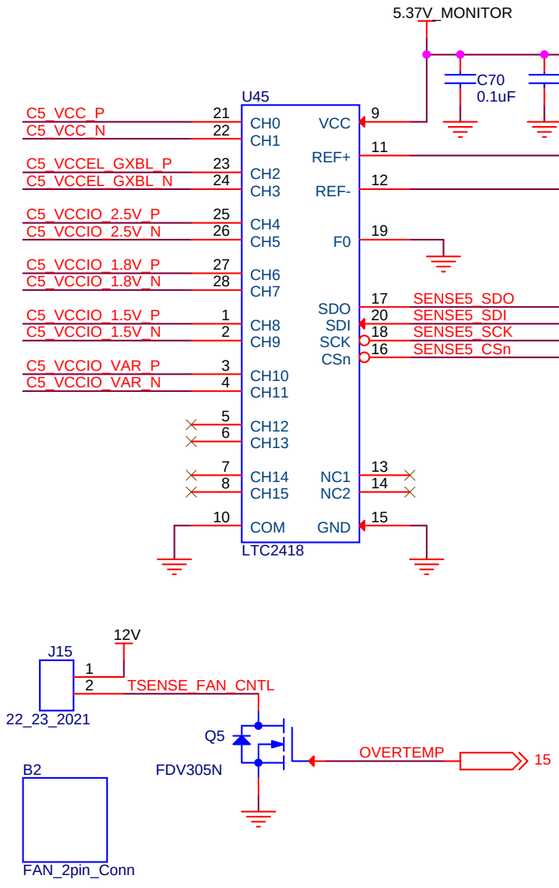
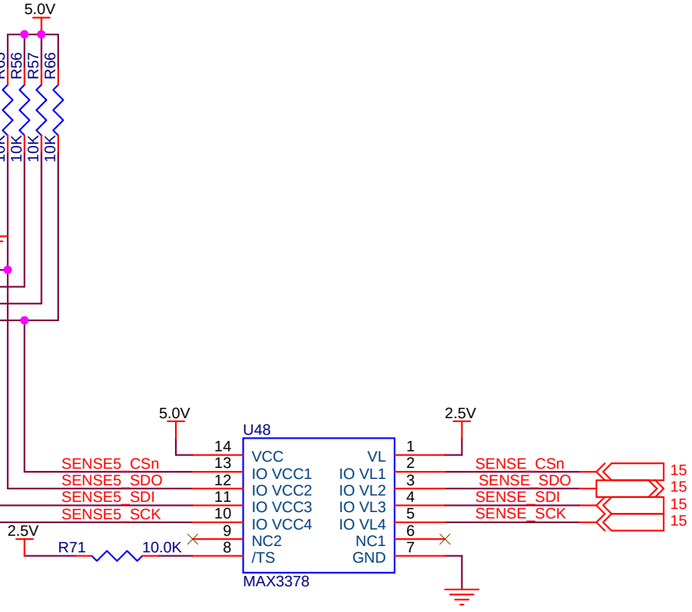
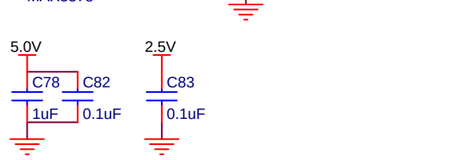
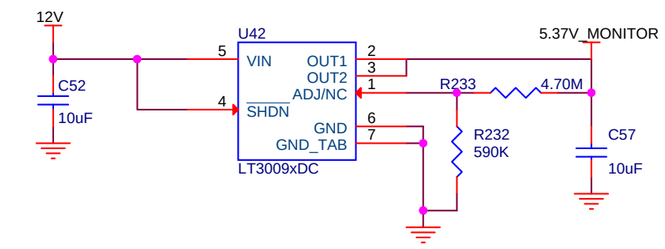
Power 6 - Power Monitor











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Cyclone V GT Decoupling

C5_VCC

C384	C347	C337	C273	C235	C223	C39	C93	C54	C75	C283	C281	C279	C277	C322	C256	C323	C306	C308	C310	C312	C313
100uF	100uF	100uF	100uF	100uF	100uF	220uF	220uF	220uF	220uF	47nF	47nF	47nF	47nF	47nF	47nF	47nF	47nF	47nF	47nF	47nF	47nF

C284	C327	C325	C309	C253	C305	C280	C282	C255	C254	C324	C326	C278	C311	C285	C307
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.22uF	0.22uF	0.22uF	0.22uF	0.22uF	0.47uF	0.47uF	1uF	1uF	2.2uF	4.7uF

C5_VCCIO_1.8V

C349	C396
0.1uF	4.7uF

C5_VCCL_GXBL

C289	C331
0.1uF	4.7uF

VREF_DDR3A

C403	C401	C405	C369
0.1uF	0.1uF	0.1uF	0.1uF

VREF_DDR3B

C321	C251	C303	C275
0.1uF	0.1uF	0.1uF	0.1uF

C5_VCCIO_1.5V

C428	C226	C92	C395	C397	C410	C380	C402	C302	C274	C276	C367	C320	C338	C377	C408	C406
100uF	330uF 4V	330uF 4V	22nF	22nF	22nF	22nF	22nF	22nF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	47nF	47nF	47nF

C385	C368	C379	C236	C228	C378	C399	C227
0.1uF	0.1uF	0.1uF	0.22uF	0.47uF	1uF	1uF	4.7uF

C5_VCCE_GXBL

C64	C102	C292	C242	C243	C333	C341	C344	C330	C342	C343	C291	C258	C293	C316	C317
220uF	330uF 10V	22nF	22nF	22nF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF

C357	C332	C290	C286	C287	C315	C329	C260	C314	C261
0.01uF	0.01uF	47nF	47nF	47nF	0.1uF	0.22uF	0.47uF	1uF	4.7uF

C5_VCCIO_2.5V

C429	C40	C24	C353	C356	C354	C201	C371	C386	C230	C252	C241	C238	C240	C352	C197	C199
100uF	330uF 10V	330uF 10V	22nF	22nF	22nF	22nF	22nF	22nF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	47nF	47nF	47nF

C351	C348	C304	C193	C231	C370	C355	C224
0.1uF	0.1uF	0.1uF	0.22uF	0.47uF	1uF	1uF	4.7uF

C5_2.5V

C430	C427	C259	C288	C202	C170	C411	C376	C398	C400	C404	C409	C257	C237	C407
100uF	100uF	22nF	22nF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF

C200	C412	C339	C239	C183	C328	C340	C196	C198	C182	C195	C350	C194
4.7uF	4.7uF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	47nF	47nF	0.1uF	0.22uF	0.47uF	1uF

C5_VCCIO_VAR

C14	C17	C30	C163	C175	C190	C162	C192	C191	C171	C165	C189	C176	C164	C166	C167	C168
100uF	330uF 4V	330uF 4V	22nF	22nF	22nF	22nF	22nF	22nF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	47nF	47nF	47nF

C229	C169	C181	C209	C177	C179	C180	C178
0.1uF	0.1uF	0.1uF	0.22uF	0.47uF	1uF	1uF	4.7uF

PCB1	SCREW1	SCREW2	STANDOFF1
	SCREW3	SCREW4	STANDOFF2
		SCREW5	STANDOFF3
		SCREW6	STANDOFF4

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