External Memory Interfaces in Cyclone V Devices

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The Cyclone® V devices provide an efficient architecture that allows you to fit wide external memory interfaces to support a high level of system bandwidth within the small modular I/O bank structure. The I/Os are designed to provide high-performance support for existing and emerging external memory standards.

Table 6-1: Supported External Memory Standards in Cyclone V Devices

Memory Standard	Hard Memory Controller	Soft Memory Controller
DDR3 SDRAM	Full rate	Half rate
DDR2 SDRAM	Full rate	Half rate
LPDDR2 SDRAM	Full rate	Half rate

Related Information

- **External Memory Interface Spec Estimator**
  For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.
- **External Memory Interface Handbook**
  Provides more information about the memory types supported, board design guidelines, timing analysis, simulation, and debugging information.
- **Cyclone V Device Handbook: Known Issues**
  Lists the planned updates to the *Cyclone V Device Handbook* chapters.

External Memory Performance

Table 6-2: External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

Related Information

- **External Memory Interface Spec Estimator**
  For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.
- **Cyclone V Device Datasheet**

HPS External Memory Performance

Table 6-3: HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Altera's External Memory Interface Spec Estimator tool.

Memory Interface Pin Support in Cyclone V Devices

In the Cyclone V devices, the memory interface circuitry is available in every I/O bank that does not support transceivers. The devices offer differential input buffers for differential read-data strobe and clock operations.

The memory clock pins are generated with double data rate input/output (DDRIO) registers.

Related Information

Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
Provides more information about which pins to use for memory clock pins and pin location requirements.

Guideline: Using DQ/DQS Pins

The following list provides guidelines on using the DQ/DQS pins:

- The devices support DQ and DQS signals with DQ bus modes of x8 or x16. Cyclone V devices do not support the x4 bus mode.
- You can use the DQSn pins that are not used for clocking as DQ pins.
- If you do not use the DQ/DQS pins for memory interfacing, you can use these pins as user I/Os. However, unused HPS DQ/DQS pins on the Cyclone V SX and ST devices cannot be used as user I/Os.
- Some specific DQ pins can also be used as RZQ pins. If you need extra RZQ pins, you can use these the DQ pins as RZQ pins instead.

Note: For the x8 or x16 DQ/DQS groups whose members are used as RZQ pins, Altera recommends that you assign the DQ and DQS pins manually. Otherwise, the Quartus II software might not be able to place the DQ and DQS pins, resulting in a "no-fit" error.

Reading the Pin Table

For the maximum number of DQ pins and the exact number per group for a particular Cyclone V device, refer to the relevant device pin table.

In the pin tables, the DQS and DQSn pins denote the differential data strobe/clock pin pairs. The DQS and DQSn pins are listed respectively in the Cyclone V pin tables as `DQS`*XY* and `DQSn`*XY*. *X* indicates the DQ/DQS grouping number and *Y* indicates whether the group is located on the top (T), bottom (B), left (L), or right (R) side of the device.

Note: The F484 package of the Cyclone V E A9, GX C9, and GT D9 devices can only support a 24 bit hard memory controller on the top side using the `T_DQ_0` to `T_DQ_23` pin assignments. Even though the F484 package pin tables of these devices list `T_DQ_32` to `T_DQ_39` in the "HMC Pin Assignment" columns, you cannot use these pin assignments for the hard memory controller.

Related Information

- **Hard Memory Controller Width for Cyclone V E** on page 6-35
- **Hard Memory Controller Width for Cyclone V GX** on page 6-36
- **Hard Memory Controller Width for Cyclone V GT** on page 6-37
- **Cyclone V Device Pin-Out Files**
  Download the relevant pin tables from this web page.

DQ/DQS Bus Mode Pins for Cyclone V Devices

The following table lists the pin support per DQ/DQS bus mode, including the DQS and DQSn pin pairs. The maximum number of data pins per group listed in the table may vary according to the following conditions:

- Single-ended DQS signaling—the maximum number of DQ pins includes data mask connected to the DQS bus network.

- Differential or complementary DQS signaling—the maximum number of data pins per group decreases by one.
- DDR3 and DDR2 interfaces—each x8 group of pins require one DQS pin. You may also require one DQSn pin and one DM pin. This further reduces the total number of data pins available.

Table 6-4: DQ/DQS Bus Mode Pins for Cyclone V Devices

Mode	DQSn Support	Data Mask (Optional)	Maximum Data Pins per Group
x8	Yes	Yes	11
x16	Yes	Yes	23

DQ/DQS Groups in Cyclone V E

Table 6-5: Number of DQ/DQS Groups Per Side in Cyclone V E Devices

This table lists the DQ/DQS groups for the soft memory controller. For the hard memory controller, you can get the DQ/DQS groups from the pin table of the specific device. The numbers are preliminary before the devices are available.

Member Code	Package	Side	x8	x16
A2 A4	256-pin FineLine BGA	Top	2	0
		Left	1	0
		Right	2	0
		Bottom	3	0
	324-pin Ultra FineLine BGA	Top	3	0
		Left	2	0
		Right	2	0
		Bottom	4	0
	383-pin Micro FineLine BGA	Top	4	0
		Left	2	0
		Right	1	0
		Bottom	4	0
	484-pin Ultra FineLine BGA	Top	5	1
		Left	1	0
		Right	2	0
		Bottom	6	1
	484-pin FineLine BGA	Top	5	1
		Left	1	0
		Right	2	0
		Bottom	6	1
A5	383-pin Micro FineLine BGA	Top	4	0
		Right	1	0
		Bottom	4	0
	484-pin Ultra FineLine BGA	Top	5	1
		Right	3	0
		Bottom	6	1
	484-pin FineLine BGA	Top	7	2
		Right	2	0
		Bottom	6	1

Member Code	Package	Side	x8	x16
A7	484-pin Micro FineLine BGA	Top	5	1
		Right	4	0
		Bottom	6	1
	484-pin Ultra FineLine BGA	Top	5	1
		Right	4	1
		Bottom	6	1
	484-pin FineLine BGA	Top	7	2
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	0
		Bottom	8	2
	896-pin FineLine BGA	Top	10	3
		Right	10	3
		Bottom	10	3
A9	484-pin Ultra FineLine BGA	Top	5	1
		Right	4	0
		Bottom	6	1
	484-pin FineLine BGA	Top	5	1
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	0
		Bottom	8	2
	896-pin FineLine BGA	Top	10	3
		Right	10	3
		Bottom	10	3

Related Information

Cyclone V Device Pin-Out Files

Download the relevant pin tables from this web page.

DQ/DQS Groups in Cyclone V GX

Table 6-6: Number of DQ/DQS Groups Per Side in Cyclone V GX Devices

This table lists the DQ/DQS groups for the soft memory controller. For the hard memory controller, you can get the DQ/DQS groups from the pin table of the specific device. The numbers are preliminary before the devices are available.

Member Code	Package	Side	x8	x16
C3	324-pin Ultra FineLine BGA	Top	3	0
		Right	2	0
		Bottom	4	0
	484-pin Ultra FineLine BGA	Top	5	1
		Right	2	0
		Bottom	6	1
	484-pin FineLine BGA	Top	5	1
		Right	2	0
		Bottom	6	1
C4 C5	301-pin Micro FineLine BGA	Top	TBD	TBD
		Left	TBD	TBD
		Right	TBD	TBD
		Bottom	TBD	TBD
	383-pin Micro FineLine BGA	Top	4	0
		Right	1	0
		Bottom	4	0
	484-pin Ultra FineLine BGA	Top	5	1
		Right	3	0
		Bottom	6	1
	484-pin FineLine BGA	Top	7	2
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	2
		Bottom	8	2

Member Code	Package	Side	x8	x16
C7	484-pin Micro FineLine BGA	Top	5	1
		Right	4	0
		Bottom	6	1
	484-pin Ultra FineLine BGA	Top	5	1
		Right	4	1
		Bottom	6	1
	484-pin FineLine BGA	Top	7	2
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	0
		Bottom	8	2
	896-pin FineLine BGA	Top	10	3
		Right	10	3
		Bottom	10	3
C9	484-pin Ultra FineLine BGA	Top	5	1
		Right	4	0
		Bottom	6	1
	484-pin FineLine BGA	Top	5	1
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	0
		Bottom	8	2
	896-pin FineLine BGA	Top	10	3
		Right	10	3
		Bottom	10	3
	1152-pin FineLine BGA	Top	12	4
		Right	11	4
		Bottom	12	4

Related Information

Cyclone V Device Pin-Out Files
Download the relevant pin tables from this web page.

DQ/DQS Groups in Cyclone V GT

Table 6-7: Number of DQ/DQS Groups Per Side in Cyclone V GT Devices

This table lists the DQ/DQS groups for the soft memory controller. For the hard memory controller, you can get the DQ/DQS groups from the pin table of the specific device. The numbers are preliminary before the devices are available.

Member Code	Package	Side	x8	x16
D5	301-pin Micro FineLine BGA	Top	TBD	TBD
		Left	TBD	TBD
		Right	TBD	TBD
		Bottom	TBD	TBD
	383-pin Micro FineLine BGA	Top	4	0
		Right	1	0
		Bottom	4	0
	484-pin Ultra FineLine BGA	Top	5	1
		Right	3	0
		Bottom	6	1
	484-pin FineLine BGA	Top	7	2
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	2
		Bottom	8	2

Member Code	Package	Side	x8	x16
D7	484-pin Micro FineLine BGA	Top	5	1
		Right	4	0
		Bottom	6	1
	484-pin Ultra FineLine BGA	Top	5	1
		Right	4	1
		Bottom	6	1
	484-pin FineLine BGA	Top	7	2
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	0
		Bottom	8	2
	896-pin FineLine BGA	Top	10	3
		Right	10	3
		Bottom	10	3
D9	484-pin Ultra FineLine BGA	Top	5	1
		Right	4	0
		Bottom	6	1
	484-pin FineLine BGA	Top	5	1
		Right	2	0
		Bottom	6	1
	672-pin FineLine BGA	Top	7	2
		Right	6	0
		Bottom	8	2
	896-pin FineLine BGA	Top	10	3
		Right	10	3
		Bottom	10	3
	1152-pin FineLine BGA	Top	12	4
		Right	11	4
		Bottom	12	4

Related Information

Cyclone V Device Pin-Out Files
Download the relevant pin tables from this web page.

DQ/DQS Groups in Cyclone V SE

Table 6-8: Number of DQ/DQS Groups Per Side in Cyclone V SE Devices

This table lists the DQ/DQS groups for the soft memory controller. For the hard memory controller, you can get the DQ/DQS groups from the pin table of the specific device. The numbers are preliminary before the devices are available.

Member Code	Package	Side	x8	x16
A2 A4	484-pin Ultra FineLine BGA	Right	1	0
		Bottom	2	0
	672-pin Ultra FineLine BGA	Right	1	0
		Bottom	8	2
A5 A6	484-pin Ultra FineLine BGA	Right	1	0
		Bottom	2	0
	672-pin Ultra FineLine BGA	Right	1	0
		Bottom	8	2
	896-pin FineLine BGA	Top	5	2
		Right	3	0
		Bottom	10	3

DQ/DQS Groups in Cyclone V SX

Table 6-9: Number of DQ/DQS Groups Per Side in Cyclone V SX Devices

This table lists the DQ/DQS groups for the soft memory controller. For the hard memory controller, you can get the DQ/DQS groups from the pin table of the specific device. The numbers are preliminary before the devices are available.

Member Code	Package	Side	x8	x16
C2 C4	672-pin Ultra FineLine BGA	Right	1	0
		Bottom	8	2
C5 C6	672-pin Ultra FineLine BGA	Right	1	0
		Bottom	8	2
	896-pin FineLine BGA	Top	5	2
		Right	3	0
		Bottom	10	3

Related Information

Cyclone V Device Pin-Out Files
Download the relevant pin tables from this web page.

DQ/DQS Groups in Cyclone V ST

Table 6-10: Number of DQ/DQS Groups Per Side in Cyclone V ST Devices

This table lists the DQ/DQS groups for the soft memory controller. For the hard memory controller, you can get the DQ/DQS groups from the pin table of the specific device. The numbers are preliminary before the devices are available.

Member Code	Package	Side	x8	x16
D5 D6	896-pin FineLine BGA	Top	5	2
		Right	3	0
		Bottom	10	3

Related Information

Cyclone V Device Pin-Out Files
Download the relevant pin tables from this web page.

External Memory Interface Features in Cyclone V Devices

The Cyclone V I/O elements (IOE) provide built-in functionality required for a rapid and robust implementation of external memory interfacing.

The following device features are available for external memory interfaces:

- DQS phase-shift circuitry
- PHY Clock (PHYCLK) networks
- DQS logic block
- Dynamic on-chip termination (OCT) control
- IOE registers
- Delay chains
- Hard memory controllers

UniPHY IP

The high-performance memory interface solution includes the self-calibrating UniPHY IP that is optimized to take advantage of the Cyclone V I/O structure and the Quartus II software TimeQuest Timing Analyzer. The UniPHY IP helps set up the physical interface (PHY) best suited for your system. This provides the total solution for the highest reliable frequency of operation across process, voltage, and temperature (PVT) variations.

The UniPHY IP instantiates a PLL to generate related clocks for the memory interface. The UniPHY IP can also dynamically choose the number of delay chains that are required for the system. The amount of delay is equal to the sum of the intrinsic delay of the delay element and the product of the number of delay steps and the value of the delay steps.

The UniPHY IP and the Altera memory controller MegaCore® functions can run at half the I/O interface frequency of the memory devices, allowing better timing management in high-speed memory interfaces. The Cyclone V devices contain built-in circuitry in the IOE to convert data from full rate (the I/O frequency) to half rate (the controller frequency) and vice versa.

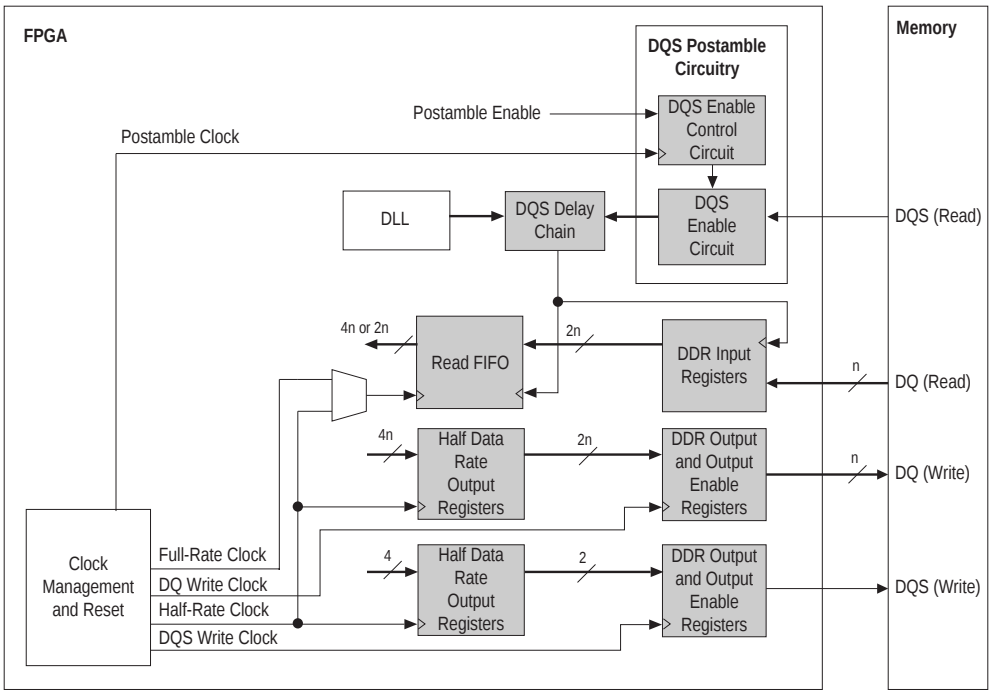
Related Information

Reference Material volume, External Memory Interface Handbook
Provides more information about the UniPHY IP.

External Memory Interface Datapath

The following figure shows an overview of the memory interface datapath that uses the Cyclone V I/O elements. In the figure, the DQ/DQS read and write signals may be bidirectional or unidirectional, depending on the memory standard. If the signal is bidirectional, it is active during read and write operations. You can bypass each register block.

Figure 6-1: External Memory Interface Datapath Overview for Cyclone V Devices



Note: There are slight block differences for different memory interface standards. The shaded blocks are part of the I/O elements.

DQS Phase-Shift Circuitry

The Cyclone V DLL provides phase shift to the DQS pins on read transactions if the DQS pins are acting as input clocks or strobes to the FPGA.

The following figures show how the DLLs are connected to the DQS pins in the various Cyclone V variants. The reference clock for each DLL may come from adjacent PLLs.

Note: The following figures show all possible connections for each device. For available pins and connections in each device package, refer to the device pin-out files.

Figure 6-2: DQS Pins and DLLs in Cyclone V E (A2 and A4) Devices

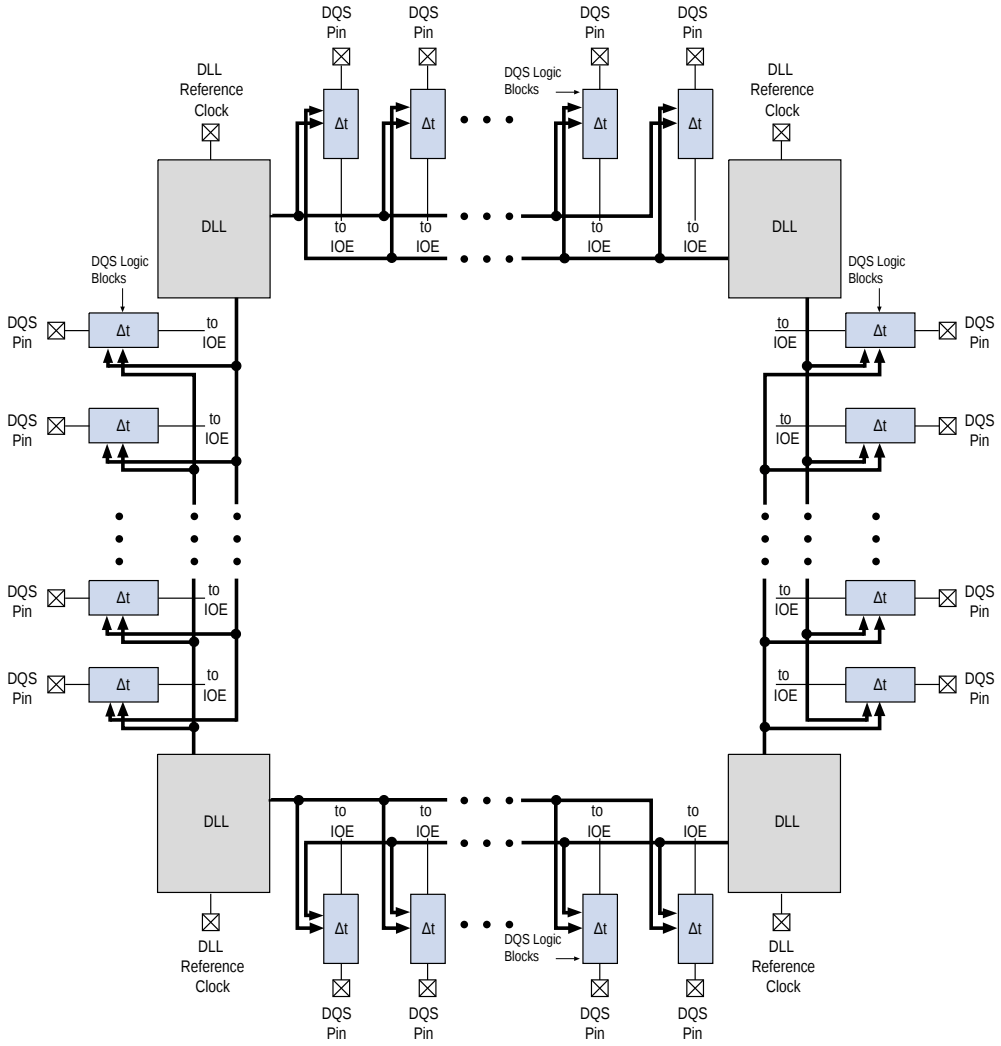


Figure 6-3: DQS Pins and DLLs in Cyclone V GX (C3) Devices

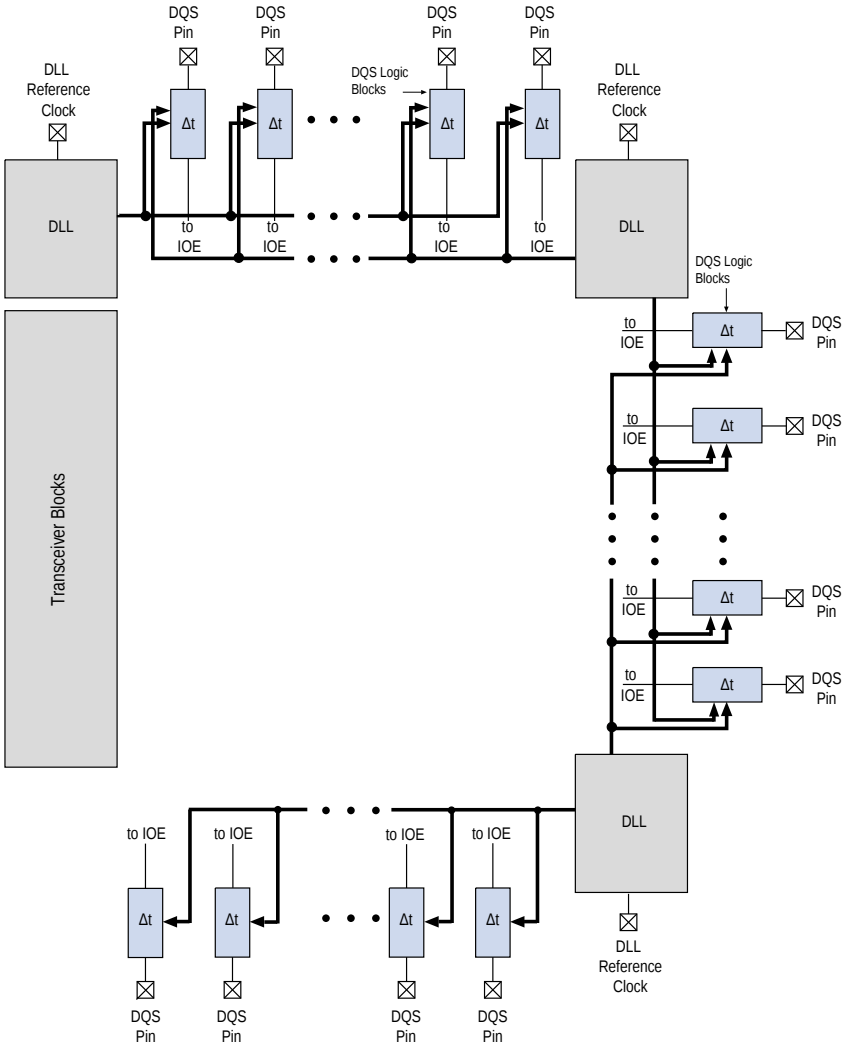


Figure 6-4: DQS Pins and DLLs in Cyclone V E (A5, A7, and A9), GX (C4, C5, C7, and C9), GT (D5, D7, and D9) Devices

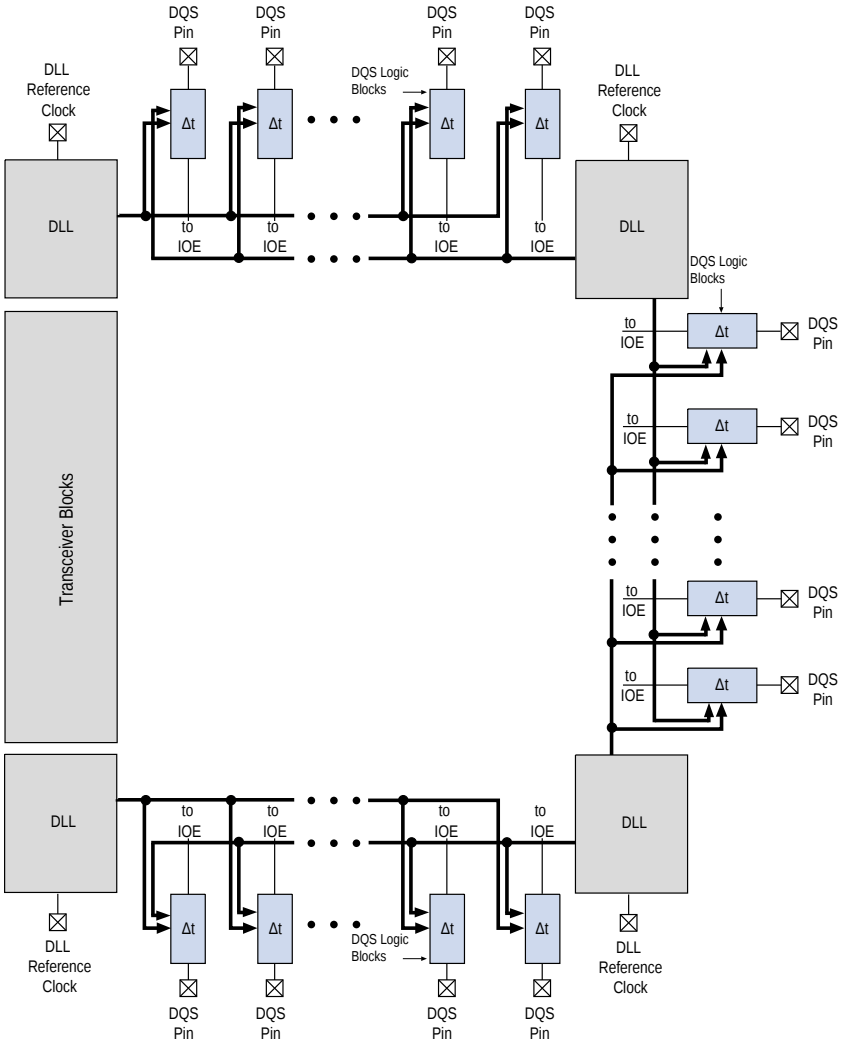


Figure 6-5: DQS Pins and DLLs in Cyclone V SE (A2, A4, A5, and A6) Devices

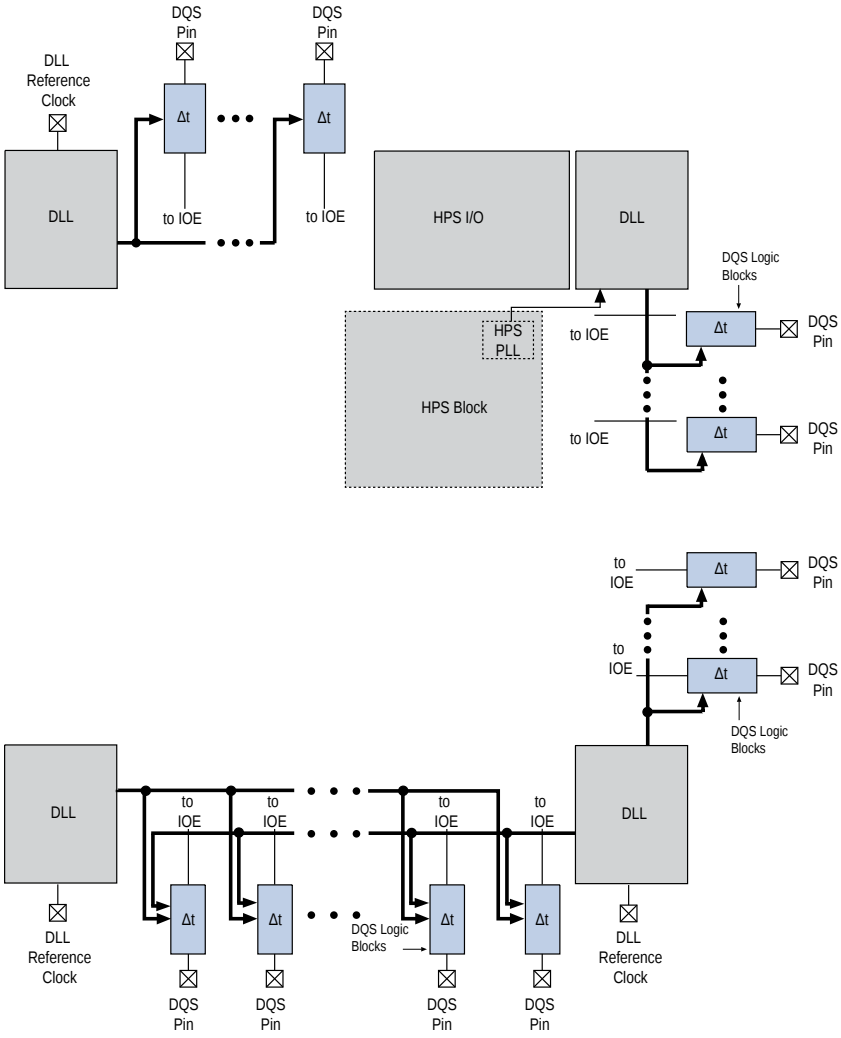
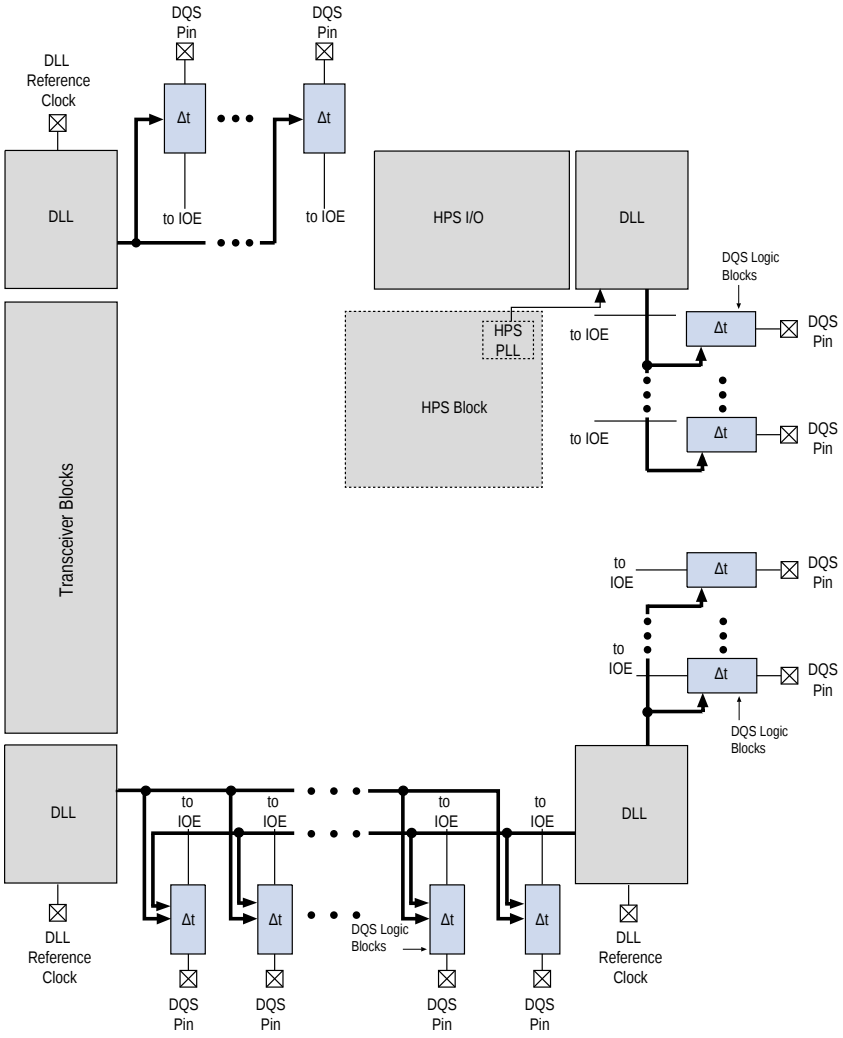


Figure 6-6: DQS Pins and DLLs in Cyclone V SX (C2, C4, C5, and C6) and ST (D5 and D6) Devices



Related Information

Cyclone V Device Pin-Out Files
Download the relevant pin tables from this web page.

Delay-Locked Loop

The delay-locked loop (DLL) uses a frequency reference to dynamically generate control signals for the delay chains in each of the DQS pins, allowing the delay to compensate for process, voltage, and temperature (PVT) variations. The DQS delay settings are gray-coded to reduce jitter if the DLL updates the settings.

There are a maximum of four DLLs, located in each corner of the Cyclone V devices. You can clock each DLL using different frequencies.

The DLLs can access the two adjacent sides from its location in the device. You can have two different interfaces with the same frequency on the two sides adjacent to a DLL, where the DLL controls the DQS delay settings for both interfaces.

I/O banks between two DLLs have the flexibility to create multiple frequencies and multiple-type interfaces. These banks can use settings from either or both adjacent DLLs. For example, DQS1R can get its phase-shift settings from DLL_TR, while DQS2R can get its phase-shift settings from DLL_BR.

The reference clock for each DLL may come from the PLL output clocks or clock input pins.

Note: If you have a dedicated PLL that only generates the DLL input reference clock, set the PLL mode to **Direct Compensation** to achieve better performance (or the Quartus II software automatically changes it). Because the PLL does not use any other outputs, it does not have to compensate for any clock paths.

DLL Reference Clock Input for Cyclone V Devices

Table 6-11: DLL Reference Clock Input from PLLs for Cyclone V E (A2, A4, A5, A7, and A9), GX (C4, C5, C7, and C9), and GT (D5, D7, and D9) Devices—Preliminary

DLL	PLL			
	Top Left	Top Right	Bottom Left	Bottom Right
DLL_TL	pllout	—	—	—
DLL_TR	—	pllout	—	—
DLL_BL	—	—	pllout	—
DLL_BR	—	—	—	pllout

Table 6-12: DLL Reference Clock Input from PLLs for Cyclone V GX (C3) Device—Preliminary

DLL	PLL			
	Top Left	Top Right	Bottom Left	Bottom Right
DLL_TL	pllout	—	—	—
DLL_TR	—	pllout	—	—
DLL_BL	—	—	—	—
DLL_BR	—	—	—	pllout

Table 6-13: DLL Reference Clock Input from PLLs for Cyclone V SE A2, A4, A5, and A6 Devices, Cyclone V SX C2, C4, C5, and C6 Devices, and Cyclone V ST D5 and D6 Devices—Preliminary

DLL	PLL			
	Top Left	Top Right	Bottom Left	Bottom Right
DLL_TL	pllout	—	—	—
DLL_TR	—	—	—	—
DLL_BL	—	—	pllout	—

DLL	PLL			
	Top Left	Top Right	Bottom Left	Bottom Right
DLL_BR	—	—	—	pllout

DLL Phase-Shift

The DLL can shift the incoming DQS signals by 0° or 90°. The shifted DQS signal is then used as the clock for the DQ IOE input registers, depending on the number of DQS delay chains used.

All DQS pins referenced to the same DLL, can have their input signal phase shifted by a different degree amount but all must be referenced at one particular frequency. However, not all phase-shift combinations are supported. The phase shifts on the DQS pins referenced by the same DLL must all be a multiple of 90°.

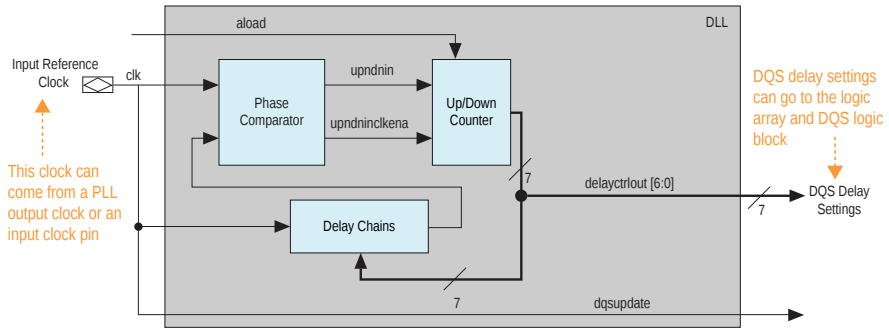
The 7-bit DQS delay settings from the DLL vary with PVT to implement the phase-shift delay. For example, with a 0° shift, the DQS signal bypasses both the DLL and DQS logic blocks. The Quartus II software automatically sets the DQ input delay chains, so that the skew between the DQ and DQS pins at the DQ IOE registers is negligible if a 0° shift is implemented. You can feed the DQS delay settings to the DQS logic block and logic array.

The shifted DQS signal goes to the DQS bus to clock the IOE input registers of the DQ pins. The signal can also go into the logic array for resynchronization if you are not using IOE read FIFO for resynchronization.

For Cyclone V SoC devices, you can feed the hard processor system (HPS) DQS delay settings to the HPS DQS logic block only.

Figure 6-7: Simplified Diagram of the DQS Phase-Shift Circuitry

This figure shows a simple block diagram of the DLL. All features of the DQS phase-shift circuitry are accessible from the UniPHY megafunction in the Quartus II software.



The input reference clock goes into the DLL to a chain of up to eight delay elements. The phase comparator compares the signal coming out of the end of the delay chain block to the input reference clock. The phase comparator then issues the upndn signal to the Gray-code counter. This signal increments or decrements a 7-bit delay setting (DQS delay settings) that increases or decreases the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

The DLL can be reset from either the logic array or a user I/O pin. Each time the DLL is reset, you must wait for 2,560 clock cycles for the DLL to lock before you can capture the data properly. The DLL phase comparator requires 2,560 clock cycles to lock and calculate the correct input clock period.

For the frequency range of each DLL frequency mode, refer to the device datasheet.

Related Information

Cyclone V Device Datasheet

PHY Clock (PHYCLK) Networks

The PHYCLK network is a dedicated high-speed, low-skew balanced clock tree designed for a high-performance external memory interface.

The top and bottom sides of the Cyclone V devices have up to four PHYCLK networks each. There are up to two PHYCLK networks on the left and right side I/O banks. Each PHYCLK network spans across one I/O bank and is driven by one of the PLLs located adjacent to the I/O bank.

The following figures show the PHYCLK networks available in the Cyclone V devices.

Figure 6-8: PHYCLK Networks in Cyclone V E A2 and A4 Devices

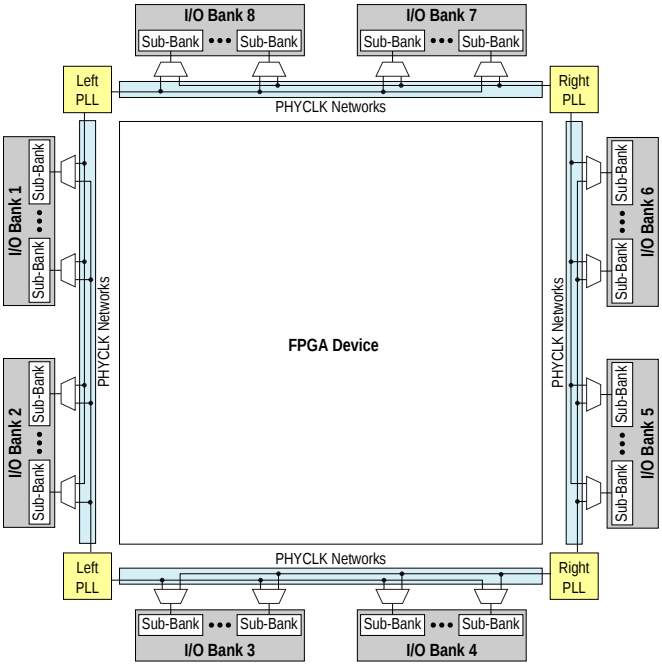


Figure 6-9: PHYCLK Networks in Cyclone V GX C3 Devices

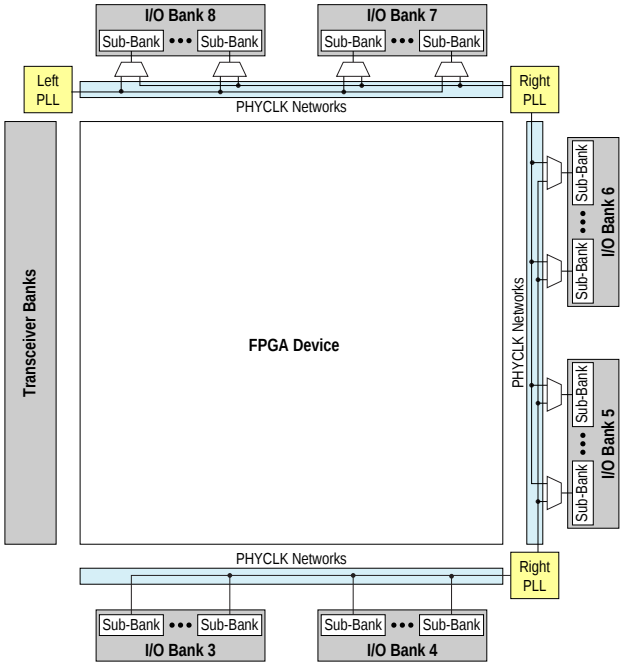


Figure 6-10: PHYCLK Networks in Cyclone V E A7, A5, and A9 Devices, Cyclone V GX C4, C5, C7, and C9 Devices, and Cyclone V GT D5, D7, and D9 Devices

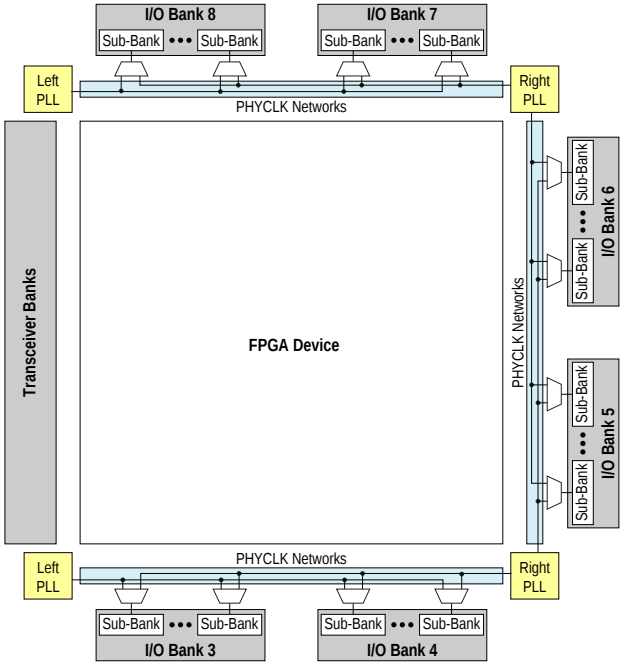


Figure 6-11: PHYCLK Networks in Cyclone V SE A2, A4, A5, and A6 Devices

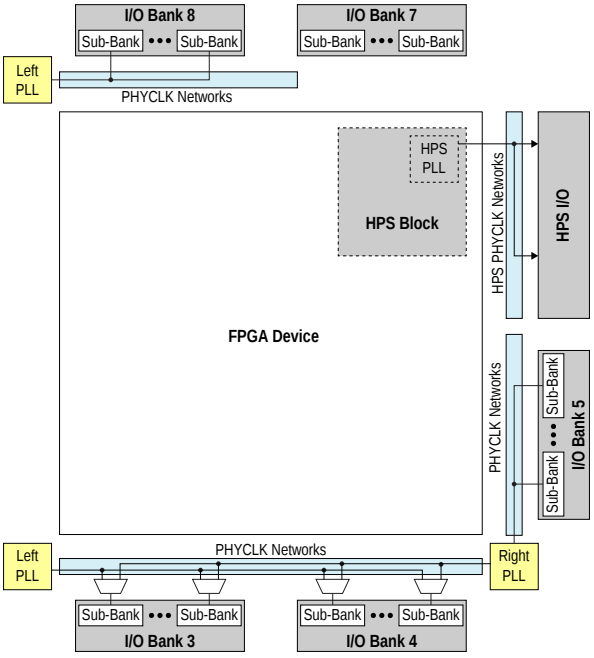
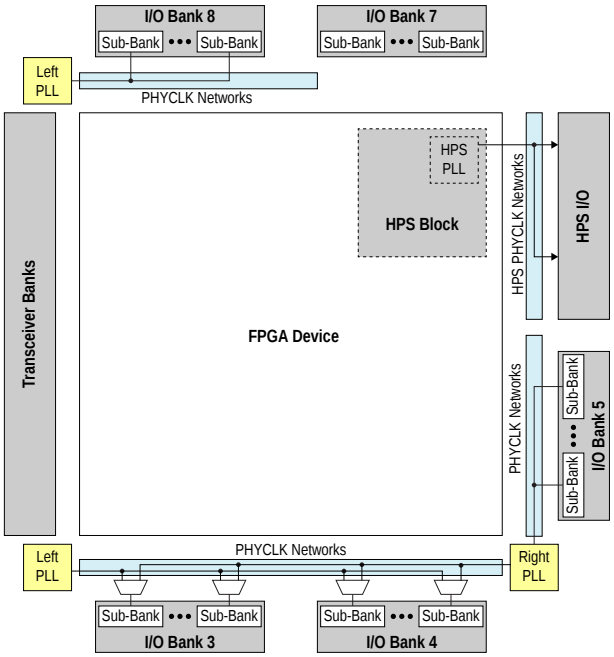


Figure 6-12: PHYCLK Networks in Cyclone V SX C2, C4, C5, and C6 Devices, and Cyclone V ST D5 and D6 Devices

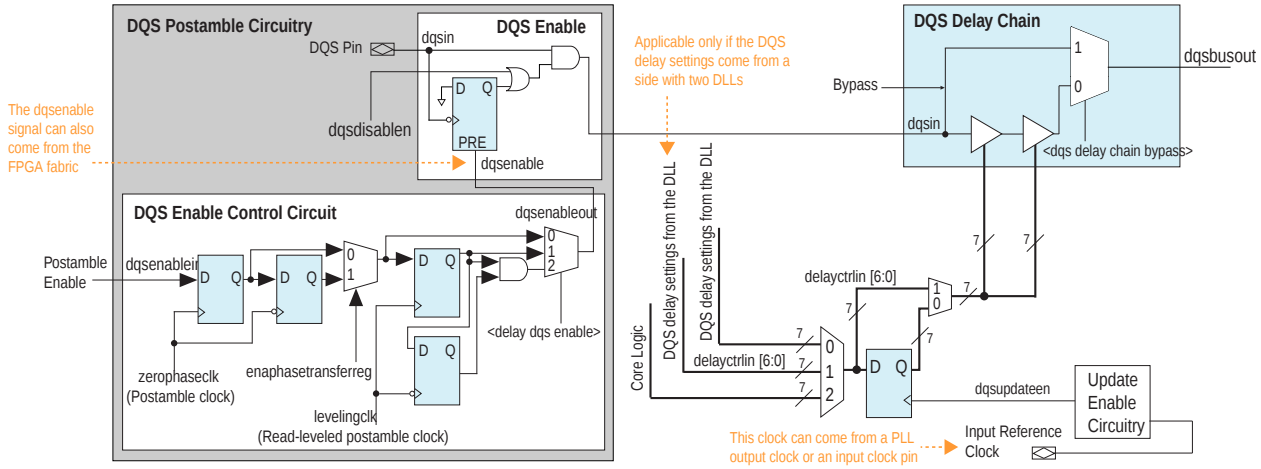


DQS Logic Block

Each DQS/CQ/CQn/QK# pin is connected to a separate DQS logic block, which consists of the update enable circuitry, DQS delay chains, and DQS postamble circuitry.

The following figure shows the DQS logic block.

Figure 6-13: DQS Logic Block in Cyclone V Devices



Update Enable Circuitry

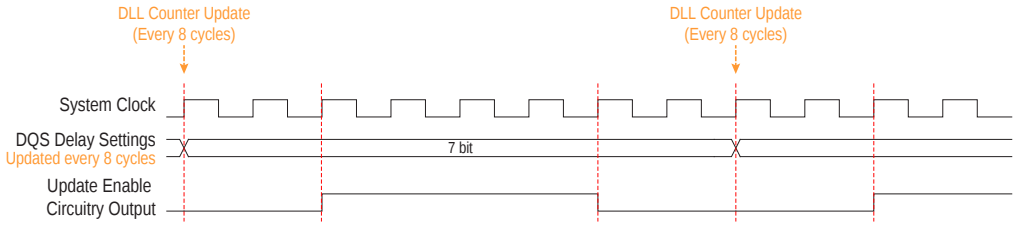
The update enable circuitry enables the registers to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry or core logic to all the DQS logic blocks before the next change.

Both the DQS delay settings and the phase-offset settings pass through a register before going into the DQS delay chains. The registers are controlled by the update enable circuitry to allow enough time for any changes in the DQS delay setting bits to arrive at all the delay elements, which allows them to be adjusted at the same time.

The circuitry uses the input reference clock or a user clock from the core to generate the update enable output. The UniPHY intellectual property (IP) uses this circuit by default.

Figure 6-14: DQS Update Enable Waveform

This figure shows an example waveform of the update enable circuitry output.



DQS Delay Chain

DQS delay chains consist of a set of variable delay elements to allow the input DQS signals to be shifted by the amount specified by the DQS phase-shift circuitry or the logic array.

There are two delay elements in the DQS delay chain that have the same characteristics:

- Delay elements in the DQS logic block
- Delay elements in the DLL

The DQS pin is shifted by the DQS delay settings.

The number of delay chains required is transparent because the UniPHY IP automatically sets it when you choose the operating frequency.

In the Cyclone V SE, SX, and ST devices, the DQS delay chain is controlled by the DQS phase-shift circuitry only.

Related Information

- **ALTDQ_DQS2 Megafunction User Guide**
  Provides more information about programming the delay chains.
- **Delay Chains** on page 6-28

DQS Postamble Circuitry

There are preamble and postamble specifications for both read and write operations in DDR3 and DDR2 SDRAM. The DQS postamble circuitry ensures that data is not lost if there is noise on the DQS line during the end of a read operation that occurs while DQS is in a postamble state.

The Cyclone V devices contain dedicated postamble registers that you can control to ground the shifted DQS signal that is used to clock the DQ input registers at the end of a read operation. This function ensures that any glitches on the DQS input signal during the end of a read operation and occurring while DQS is in a postamble state do not affect the DQ IOE registers.

- For preamble state, the DQS is low, just after a high-impedance state.
- For postamble state, the DQS is low, just before it returns to a high-impedance state.

For external memory interfaces that use a bidirectional read strobe (DDR3 and DDR2 SDRAM), the DQS signal is low before going to or coming from a high-impedance state.

Half Data Rate Block

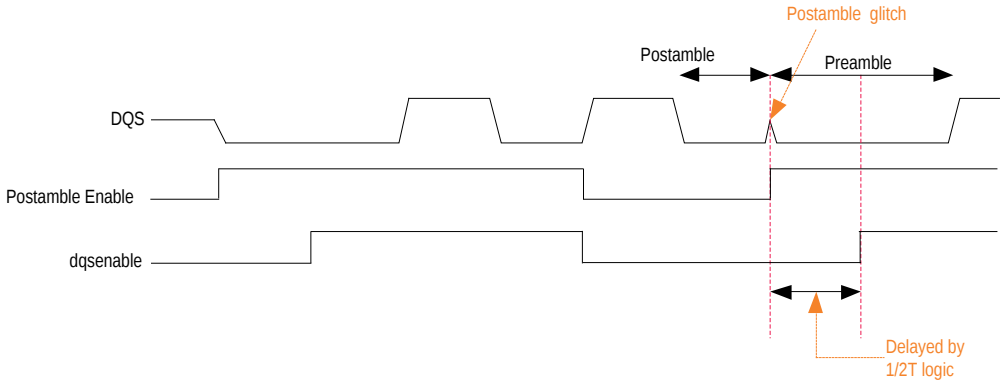
The Cyclone V devices contain a half data rate (HDR) block in the postamble enable circuitry.

The HDR block is clocked by the half-rate resynchronization clock, which is the output of the I/O clock divider circuit. There is an AND gate after the postamble register outputs to avoid postamble glitches from a previous read burst on a non-consecutive read burst. This scheme allows half-a-clock cycle latency for `dqsenable` assertion and zero latency for `dqsenable` deassertion.

Using the HDR block as the first stage capture register in the postamble enable circuitry block is optional. Altera recommends using these registers if the controller is running at half the frequency of the I/Os.

Figure 6-15: Avoiding Glitch on a Non-Consecutive Read Burst Waveform

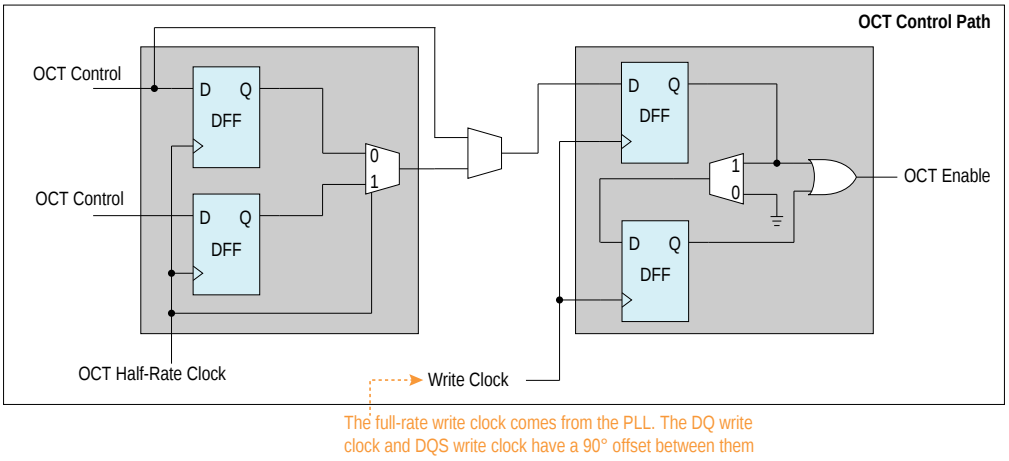
This figure shows how to avoid postamble glitches using the HDR block.



Dynamic OCT Control

The dynamic OCT control block includes all the registers that are required to dynamically turn the on-chip parallel termination (R_T OCT) on during a read and turn R_T OCT off during a write.

Figure 6-16: Dynamic OCT Control Block for Cyclone V Devices



Related Information

I/O Features in Cyclone V Devices
Provides more information about dynamic OCT control.

IOE Registers

The IOE registers are expanded to allow source-synchronous systems to have faster register-to-FIFO transfers and resynchronization. All top, bottom, and right IOEs have the same capability.

Input Registers

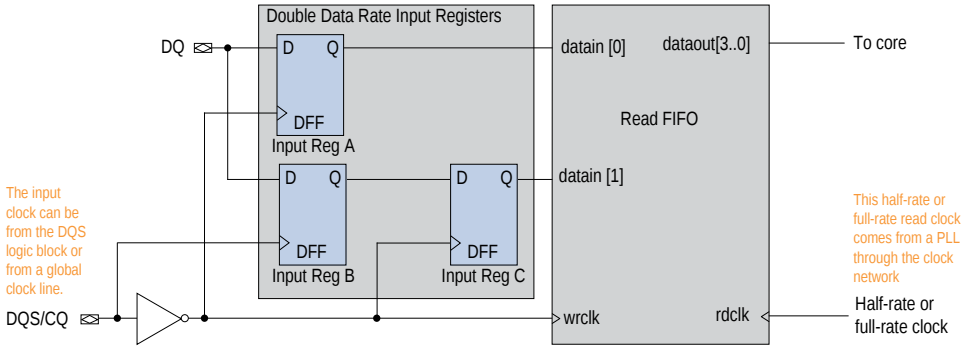
The input path consists of the DDR input registers and the read FIFO block. You can bypass each block of the input path.

There are three registers in the DDR input registers block. Registers A and B capture data on the positive and negative edges of the clock while register C aligns the captured data. Register C uses the same clock as Register A.

The read FIFO block resynchronizes the data to the system clock domain and lowers the data rate to half rate.

The following figure shows the registers available in the Cyclone V input path. For DDR3 and DDR2 SDRAM interfaces, the DQS and DQSn signals must be inverted. If you use Altera's memory interface IPs, the DQS and DQSn signals are automatically inverted.

Figure 6-17: IOE Input Registers for Cyclone V Devices



Output Registers

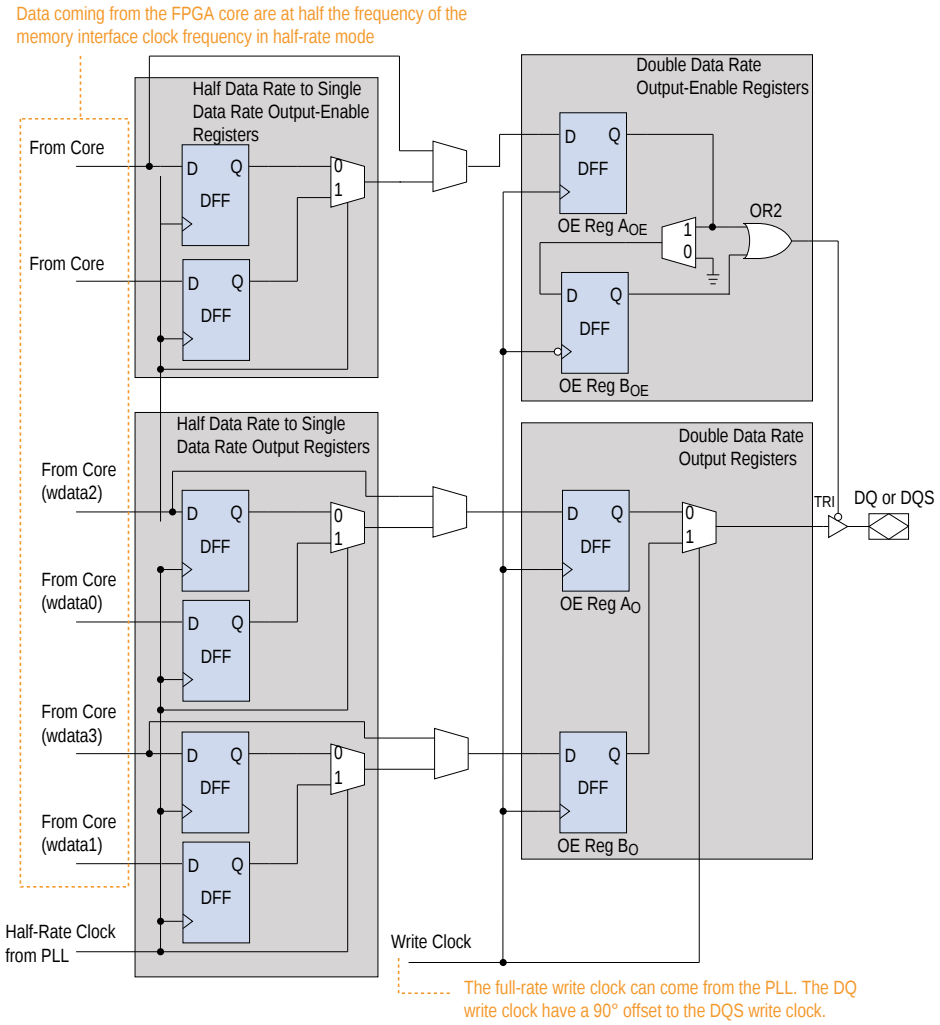
The Cyclone V output and output-enable path is divided into the HDR block, and output and output-enable registers. The device can bypass each block of the output and output-enable path.

The output path is designed to route combinatorial or registered single data rate (SDR) outputs and full-rate or half-rate DDR outputs from the FPGA core. Half-rate data is converted to full-rate with the HDR block, clocked by the half-rate clock from the PLL.

The output-enable path has a structure similar to the output path—ensuring that the output-enable path goes through the same delay and latency as the output path.

Figure 6-18: IOE Output and Output-Enable Path Registers for Cyclone V Devices

The following figure shows the registers available in the Cyclone V output and output-enable paths.



Delay Chains

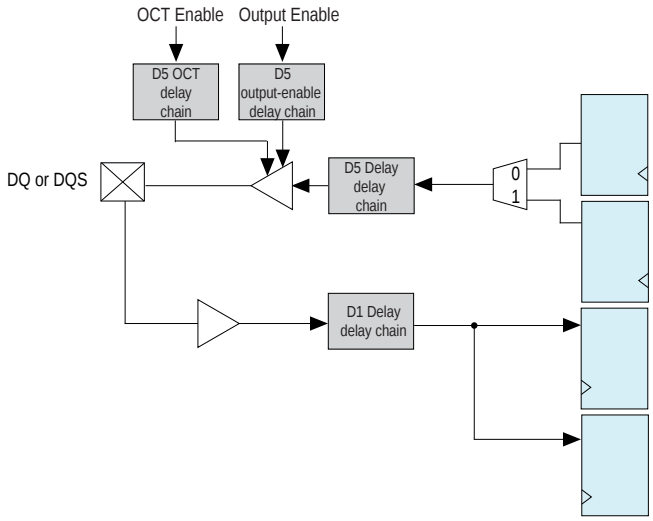
The Cyclone V devices contain run-time adjustable delay chains in the I/O blocks and the DQS logic blocks. You can control the delay chain setting through the I/O or the DQS configuration block output.

Every I/O block contains a delay chain between the following elements:

- The output registers and output buffer
- The input buffer and input register
- The output enable and output buffer
- The R_T OCT enable-control register and output buffer

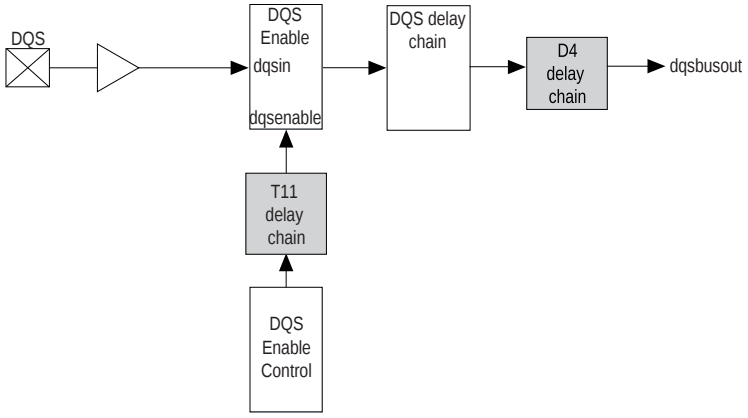
You can bypass the DQS delay chain to achieve a 0° phase shift.

Figure 6-19: Delay Chains in an I/O Block



Each DQS logic block contains a delay chain after the `dqsbusout` output and another delay chain before the `dqsenable` input.

Figure 6-20: Delay Chains in the DQS Input Path



Related Information

- **ALTDQ_DQS2 Megafunction User Guide**
  Provides more information about programming the delay chains.
- **DQS Delay Chain** on page 6-25

I/O and DQS Configuration Blocks

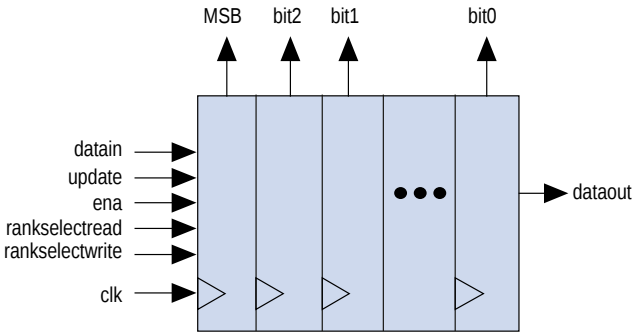
The I/O and DQS configuration blocks are shift registers that you can use to dynamically change the settings of various device configuration bits.

- The shift registers power-up low.

- Every I/O pin contains one I/O configuration register.
- Every DQS pin contains one DQS configuration block in addition to the I/O configuration register.

Figure 6-21: Configuration Block (I/O and DQS)

This figure shows the I/O configuration block and the DQS configuration block circuitry.



Related Information

ALTDQ_DQS2 Megafunction User Guide
Provides details about the I/O and DQS configuration block bit sequence.

Hard Memory Controller

The Cyclone V devices feature dedicated hard memory controllers. You can use the hard memory controllers for LPDDR2, DDR2, and DDR3 SDRAM interfaces. Compared to the memory controllers implemented using core logic, the hard memory controllers allow support for higher memory interface frequencies with shorter latency cycles.

The hard memory controllers use dedicated I/O pins as data, address, command, control, clock, and ground pins for the SDRAM interface. If you do not use the hard memory controllers, you can use these dedicated pins as regular I/O pins.

Related Information

- **Functional Description—HPC II Controller chapter, External Memory Interface Handbook**
  The hard memory controller is functionally similar to the High-Performance Controller II (HPC II).
- **Functional Description—Hard Memory Interface chapter, External Memory Interface Handbook**
  Provides detailed information about application of the hard memory interface.

Features of the Hard Memory Controller

Table 6-14: Features of the Cyclone V Hard Memory Controller

Feature	Description
Memory Interface Data Width	• 8, 16, and 32 bit data • 16 bit data + 8 bit ECC • 32 bit data + 8bit ECC

Feature	Description
Memory Density	The controller supports up to four gigabits density parts and two chip selects.
Memory Burst Length	• DDR3—Burst length of 8 and burst chop of 4 • DDR2—Burst lengths of 4 and 8 • LPDDR2—Burst lengths of 2, 4, 8, and 16
Command and Data Reordering	The controller increases efficiency through the support for out-of-order execution of DRAM commands—with address collision detection-and in-order return of results.
Starvation Control	A starvation counter ensures that all requests are served after a predefined time-out period. This function ensures that data with low priority access are not left behind when reordering data for efficiency.
User-Configurable Priority Support	When the controller detects a high priority request, it allows the request to bypass the current queuing request. This request is processed immediately and thus reduces latency.
Avalon®-MM Data Slave Local Interface	By default, the controller supports the Avalon Memory-Mapped protocol.
Bank Management	By default, the controller provides closed-page bank management on every access. The controller intelligently keeps a row open based on incoming traffic. This feature improves the efficiency of the controller especially for random traffic.
Streaming Reads and Writes	The controller can issue reads or writes continuously to sequential addresses every clock cycle if the bank is open. This function allows for very high efficiencies with large amounts of data.
Bank Interleaving	The controller can issue reads or writes continuously to 'random' addresses.
Predictive Bank Management	The controller can issue bank management commands early so that the correct row is open when the read or write occurs. This increases efficiency.
Multiport Interface	The interface allows you to connect up to six data masters to access the memory controller through the local interface. You can update the multiport scheduling configuration without interrupting traffic on a port.
Built-in Burst Adaptor	The controller can accept bursts of arbitrary sizes on its local interface and map these bursts to efficient memory commands.
Run-time Configuration of the Controller	This feature provides support for updates to the timing parameters without requiring reconfiguration of the FPGA, apart from the standard compile-time setting of the timing parameters.
On-Die Termination	The controller controls the on-die termination (ODT) in the memory, which improves signal integrity and simplifies your board design.
User-Controlled Refresh Timing	You can optionally control when refreshes occur—allowing the refreshes to avoid clashing of important reads or writes with the refresh lock-out time.

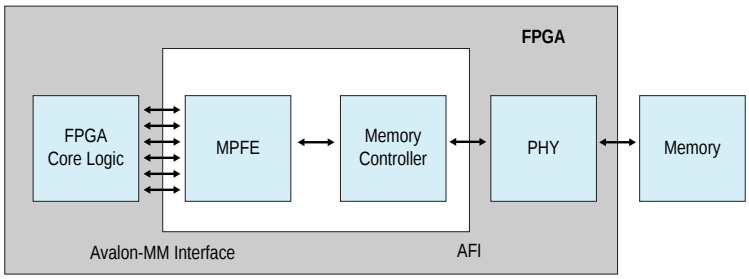
Feature	Description
Low Power Modes	You can optionally request the controller to put the memory into the self-refresh or deep power-down modes.
Partial Array Self-Refresh	You can select the region of memory to refresh during self-refresh through the mode register to save power.
ECC	Standard Hamming single error correction, double error detection (SECDED) error correction code (ECC) support: • 32 bit data + 8 bit ECC • 16 bit data + 8 bit ECC
Additive Latency	With additive latency, the controller can issue a READ/WRITE command after the ACTIVATE command to the bank prior to t_{RCD} to increase the command efficiency.
Write Acknowledgment	The controller supports write acknowledgment on the local interface.
User Control of Memory Controller Initialization	The controller supports initialization of the memory controller under the control of user logic—for example, through the software control in the user system if a processor is present.
Controller Bonding Support	You can bond two controllers to achieve wider data width for higher bandwidth applications.

Multi-Port Front End

The multi-port front end (MPFE) and its associated fabric interface provide up to six command ports, four read-data ports and four write-data ports, through which user logic can access the hard memory controller.

Figure 6-22: Simplified Diagram of the Cyclone V Hard Memory Interface

This figure shows a simplified diagram of the Cyclone V hard memory interface with the MPFE.



Numbers of MPFE Ports Per Device

Table 6-15: Numbers of MPFE Command, Write-Data, and Read-Data Ports for Each Cyclone V Device

Variant	Member Code	MPFE Ports		
		Command	Write-data	Read-data
Cyclone V E	A2	4	2	2
	A4	4	2	2
	A5	6	4	4
	A7	6	4	4
	A9	6	4	4
Cyclone V GX	C3	4	2	2
	C4	6	4	4
	C5	6	4	4
	C7	6	4	4
	C9	6	4	4
Cyclone V GT	D5	6	4	4
	D7	6	4	4
	D9	6	4	4

Bonding Support

Note: Bonding is supported only for hard memory controllers configured with one port. Do not use the bonding configuration when there is more than one port in each hard memory controller.

You can bond two hard memory controllers to support wider data widths.

If you bond two hard memory controllers, the data going out of the controllers to the user logic is synchronized. However, the data going out of the controllers to the memory is not synchronized.

The bonding controllers are not synchronized and remain independent with two separate address buses and two independent command buses. These buses are calibrated separately.

If you require ECC support for a bonded interface, you must implement the ECC logic external to the hard memory controllers.

Note: A memory interface that uses the bonding feature has higher average latency. Bonding through the core fabric will also cause a higher latency.

Figure 6-23: Hard Memory Controllers Bonding Support in Cyclone V E A7, A5, and A9 Devices, Cyclone V GX C4, C5, C7, and C9 Devices, and Cyclone V GT D5, D7, and D9 Devices

This figure shows the bonding of two opposite hard memory controllers through the core fabric.

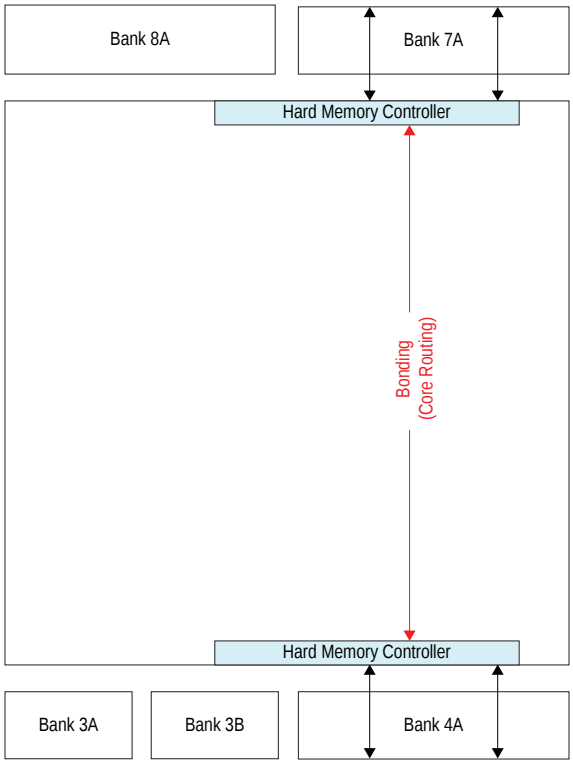
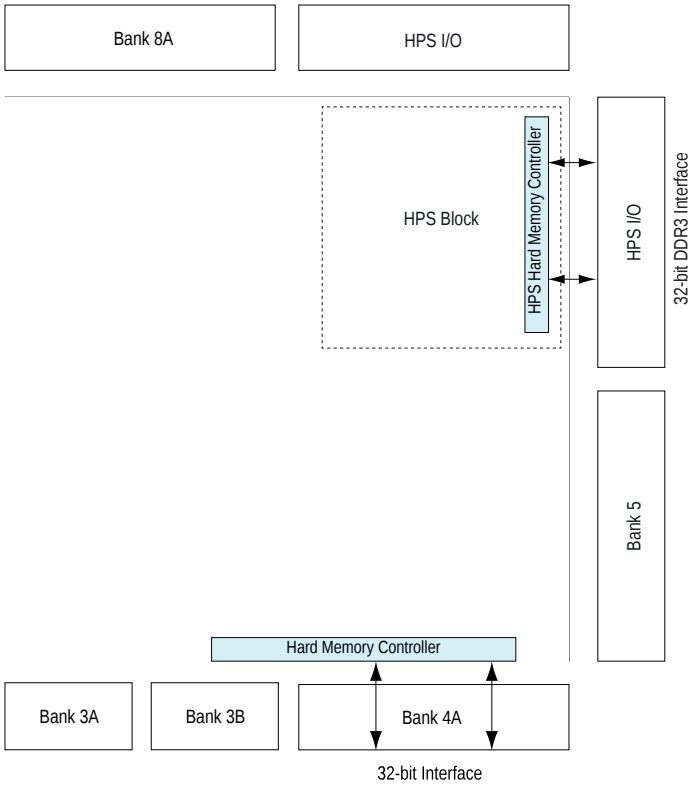


Figure 6-24: Hard Memory Controllers in Cyclone V SX C2, C4, C5, and C6 Devices, and Cyclone V ST D5 and D6 Devices

This figure shows hard memory controllers in the SoC devices. There is no bonding support.



Related Information

- **Bonding Does Not Work for Multiple MPFE Ports in Hard Memory Controller**
- **Cyclone V Device Family Pin Connection Guidelines**
  Provides more information about the dedicated pins.

Hard Memory Controller Width for Cyclone V E

Table 6-16: Hard Memory Controller Width Per Side in Cyclone V E Devices—Preliminary

Package	Member Code									
	A2		A4		A5		A7		A9	
	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom
M383	≤ 24	0	≤ 24	0	≤ 24	0	—	—	—	—
M484	—	—	—	—	—	—	24	24	—	—
F256	0	0	0	0	—	—	—	—	—	—
U324	0	0	0	0	—	—	—	—	—	—

Package	Member Code									
	A2		A4		A5		A7		A9	
	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom
U484	24	0	24	0	24	24	24	24	—	—
F484	24	0	24	0	40	24	40	24	24	24
F672	—	—	—	—	—	—	40	40	40	40
F896	—	—	—	—	—	—	40	40	40	40

Related Information

Guideline: Using DQ/DQS Pins on page 6-3
Important information about usable pin assignments for the hard memory controller in the F484 package of this device.

Hard Memory Controller Width for Cyclone V GX

Table 6-17: Hard Memory Controller Width Per Side in Cyclone V GX Devices—Preliminary

Package	Member Code									
	C3		C4		C5		C7		C9	
	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom
M301	—	—	0	0	0	0	—	—	—	—
M383	—	—	≤ 24	0	≤ 24	0	—	—	—	—
M484	—	—	—	—	—	—	24	24	—	—
U324	0	0	—	—	—	—	—	—	—	—
U484	24	0	24	24	24	24	24	24	24	24
F484	24	0	40	24	40	24	40	24	24	24
F672	—	—	40	40	40	40	40	40	40	40
F896	—	—	—	—	—	—	40	40	40	40
F1152	—	—	—	—	—	—	—	—	40	40

Related Information

Guideline: Using DQ/DQS Pins on page 6-3
Important information about usable pin assignments for the hard memory controller in the F484 package of this device.

Hard Memory Controller Width for Cyclone V GT

Table 6-18: Hard Memory Controller Width Per Side in Cyclone V GT Devices—Preliminary

Package	Member Code					
	D5		D7		D9	
	Top	Bottom	Top	Bottom	Top	Bottom
M301	0	0	—	—	—	—
M383	≤ 24	0	—	—	—	—
M484	—	—	24	24	—	—
U484	24	24	24	24	24	24
F484	40	24	40	24	24	24
F672	40	40	40	40	40	40
F896	—	—	40	40	40	40
F1152	—	—	—	—	40	40

Related Information

Guideline: Using DQ/DQS Pins on page 6-3
Important information about usable pin assignments for the hard memory controller in the F484 package of this device.

Hard Memory Controller Width for Cyclone V SE

Table 6-19: Hard Memory Controller Width Per Side in Cyclone V SE Devices—Preliminary

Package	Member Code							
	A2		A4		A5		A6	
	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom
U484	0	0	0	0	0	0	0	0
U672	0	40	0	40	0	40	0	40
F896	—	—	—	—	0	40	0	40

Table 6-20: HPS Hard Memory Controller Width in Cyclone V SE Devices—Preliminary

Package	Member Code			
	A2	A4	A5	A6
U484	32	32	32	32
U672	40	40	40	40
F896	—	—	40	40

Hard Memory Controller Width for Cyclone V SX

Table 6-21: Hard Memory Controller Width Per Side in Cyclone V SX Devices—Preliminary

Package	Member Code							
	C2		C4		C5		C6	
	Top	Bottom	Top	Bottom	Top	Bottom	Top	Bottom
U672	0	40	0	40	0	40	0	40
F896	—	—	—	—	0	40	0	40

Table 6-22: HPS Hard Memory Controller Width in Cyclone V SX Devices—Preliminary

Package	Member Code			
	C2	C4	C5	C6
U672	40	40	40	40
F896	—	—	40	40

Hard Memory Controller Width for Cyclone V ST

Table 6-23: Hard Memory Controller Width Per Side in Cyclone V ST Devices—Preliminary

Package	Member Code			
	D5		D6	
	Top	Bottom	Top	Bottom
F896	0	40	0	40

Table 6-24: HPS Hard Memory Controller Width in Cyclone V ST Devices—Preliminary

Package	Member Code	
	D5	D6
F896	40	40

Document Revision History

Date	Version	Changes
January 2014	2014.01.10	• Added Cyclone V SE DLL reference clock input information. • Added the DQ/DQS groups table for Cyclone V SE. • Added the DQS pins and DLLs figure for Cyclone V SE. • Added the PHYCLK networks figure for Cyclone V SE. • Updated the DQ/DQS numbers for the M383 package of Cyclone V E, GX, and GT variants. • Removed the statement about the bottom hard memory controller restrictions in the figure that shows the Cyclone V GX C5 hard memory controller bonding. • Added information about the hard memory controller interface widths for the Cyclone V SE. • Added the HPS hard memory controller widths for Cyclone V SE, SX, and ST. • Added related information link to **ALTDQ_DQS2 Megafunction User Guide** for more information about using the delay chains. • Changed all "SoC FPGA" to "SoC". • Added links to Altera's **External Memory Spec Estimator** tool to the topics listing the external memory interface performance. • Updated the topic about using DQ/DQS pins to specify that only some specific DQ pins can also be used as RZQ pins. • Updated the topic about DQS delay chain to remove statements about using `delayctrlin[6..0]` signals in UniPHY IP to input your own gray-coded 7 bit settings. This mode is not recommended with the UniPHY controllers. • Updated topic about hard memory controller bonding support to specify that bonding is supported only for hard memory controllers configured with one port.

Date	Version	Changes
May 2013	2013.05.06	• Moved all links to the Related Information section of respective topics for easy reference. • Added link to the known document issues in the Knowledge Base. • Added the supported minimum operating frequencies for the supported memory interface standards. • Added packages and updated the DQ/DQS groups of Cyclone V E, GX, GT, and SX devices. • Added the number of MPFE command, write-data, and read-data ports for each Cyclone V E, GX, and GT device. • Added a note about the usable hard memory controller pin assignments for the F484 package of the Cyclone V E A9, GX C9, and GT D9 devices. • Updated the M386 package to M383. • Removed the F672 package from the Cyclone V E A5 device in the table listing Cyclone V E hard memory controller widths. • Added the U484 package for the Cyclone V GX C9 device in the table listing Cyclone V GX hard memory controller widths. • Updated the hard memory controller widths of Cyclone V E, GX, SX, and ST. • Removed the restrictions on using the bottom hard memory controller of the Cyclone V GX C5 device if the configuration is 3.3/3.0 V. • Added note to clarify that the DQS phase-shift circuitry figures show all possible connections and the device pin-out files have per package information.
December 2012	2012.11.28	• Reorganized content and updated template. • Added a list of supported external memory interface standards using the hard memory controller and soft memory controller. • Added performance information for external memory interfaces and the HPS external memory interfaces. • Separated the DQ/DQS groups tables into separate topics for each device variant for easy reference. • Updated the DQ/DQS numbers and device packages for the Cyclone V E, GX, GT, SX, and ST variants. • Moved the PHYCLK networks pin placement guideline to the **Planning Pin and FPGA Resources** chapter of the *External Memory Interface Handbook*. • Moved information from the "Design Considerations" section into relevant topics. • Removed the "DDR2 SDRAM Interface" and "DDR3 SDRAM DIMM" sections. Refer to the relevant sections in the **External Memory Interface Handbook** for the information. • Added the I/O and DQS configuration blocks topic. • Updated the term "Multiport logic" to "multi-port front end" (MPFE). • Added information about the hard memory controller interface widths for the Cyclone V E, GX, GT, SX, and ST variants.

Date	Version	Changes
June 2012	2.0	Updated for the Quartus II software v12.0 release: • Restructured chapter. • Updated "Design Considerations", "DQS Postamble Circuitry", and "IOE Registers"sections. • Added SoC devices information. • Added Figure 6–5, Figure 6–10, and Figure 6–21.
February 2012	1.2	• Updated Figure 6–20. • Minor text edits.
November 2011	1.1	• Updated Table 6–2. • Added Figure 6–2.
October 2011	1.0	Initial release.